OKI Semiconductor

MSM6962/6963

Single Chip CODEC

GENERAL DESCRIPTION

The MSM6962 and MSM6963 are a single-channel CODEC CMOS ICs containing filters for A/D and D/A converting of the voice signal ranging from 300 Hz to 3400 Hz.

FEATURES

- Compliance with ITU-T companding Law
     MSM6962 : μ-law
     MSM6963 : A-law
- Enable independent operation of transmission and reception
- Transmission clock : 512, 1024, 1536, 1544, 2048 kHz
- Built-in an Auto compensation circuit for off set voltage, so long steady operation is held
- Built-in reference voltage source
- Low Power Dissipation
     Operating   (55 mW Typ.)
     Standby   (6 mW Typ.)
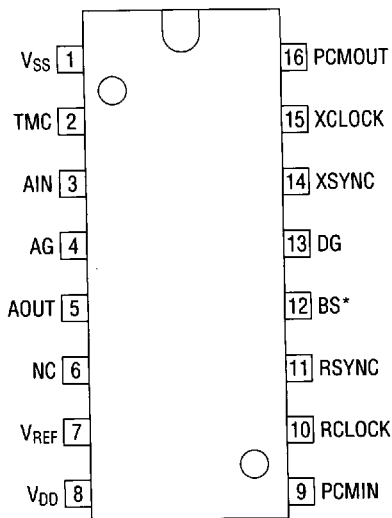- Package :
  16-pin plastic DIP   (DIP16-P-300)

Note: The product names are indicated in PIN CONFIGURATION.

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BLOCK DIAGRAM
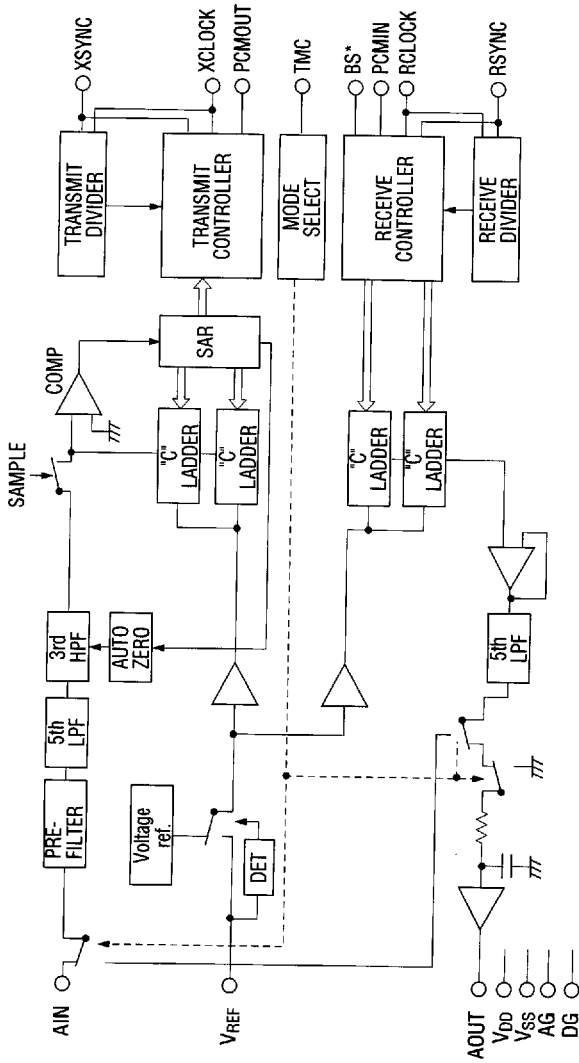
* Only the MSM6962. The pin is not connected in the MSM6963.

: ■ 6724240 0021287 T65 ■

PIN CONFIGURATION (TOP VIEW)

```
              ┌─────────┐
    Vss   1   │         │  16  PCMOUT
              │  ◯      │
    TMC   2   │         │  15  XCLOCK
              │         │
    AIN   3   │         │  14  XSYNC
              │         │
    AG    4   │         │  13  DG
              │         │
   AOUT   5   │         │  12  BS*
              │         │
    NC    6   │         │  11  RSYNC
              │         │
   VREF   7   │      ◯  │  10  RCLOCK
              │         │
    VDD   8   │         │   9  PCMIN
              └─────────┘
```

16-Pin Plastic DIP
MSM6962RS/MSM6963RS

Notes: Indication of product depends on abbreviation type, M6962 or M6963.
            BS is only for the MSM6962, and is not connected in the MSM6963.
   NC : No connect pin

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PIN AND FUNCTIONAL DESCRIPTIONS

V$_{SS}$ pin1

Negative voltage power supply.
The range of power supply voltage is –5 V ±5%.

TMC pin2

Control signal input for mode selection.
The normal operating mode or analog loop-back mode can be selected.

"TMC"	Mode	"AIN"	"AOUT"
> 2.0 V	Normal Operation	Transmit signal input	Receive signal output Connected to RCV$_{FIL}$ output "AOUT"
< 0.8 V	Analog Loop-back	Disconnected	0 V

⟶ Signal flow in normal operating mode
---► Signal flow in analog loop-back mode
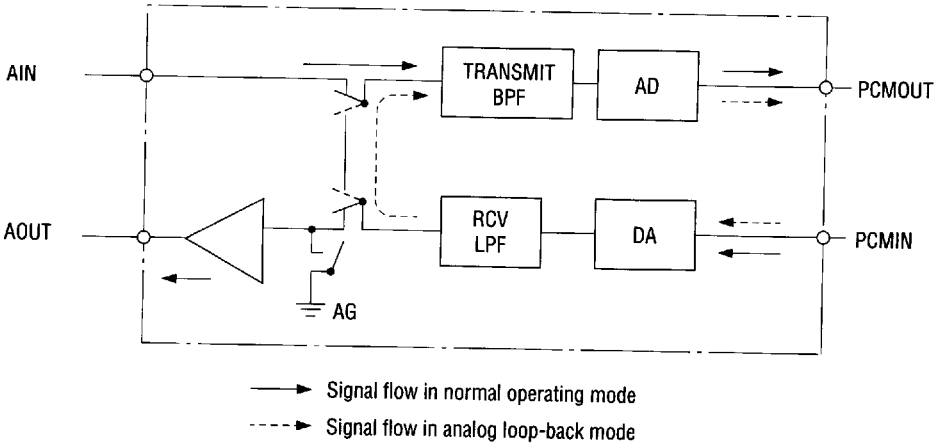
Since the TMC input signal is monitored on each frame by internal XSYNC pulse, the control for mode selection by TMC signal is not executed in the no-signal state of XSYNC and XCLOCK.

AIN pin 3

AIN is an analog signal input and is normally connected to the transmit filter input.
The input analog signal is bandwidth-limited to (300 Hz to 3400 Hz) and is converted to the 8-bit PCM signal.
The input signal amplitude range is 5 V_{P-P}. In analog loop-back mode, the state of this pin is left open.
Since this pin is high impedance input, a resister of 20 kΩ or less should be connected between this pin and AG pin, in the case of AC connection circuit to this pin. (Where DC current is cut off to this pin by external condenser.)

AG pin 4

Analog signal ground.

AOUT pin 5

Analog signal output.
AOUT is connected to an output of the receive filter. The output signal amplitude range is 5 V_{P-P}.
The signal level is 0 V at analog loop-back mode. This output signal is able to drive a resister load of 10 kΩ or more, but it is recommendable to drive as higher resister as possible.
A level of this pin is fixed to 0 V , when powered down.

NC pin 6

Non-connected.

V_{REF} pin 7

Input of the external reference voltage source.
When a state of this pin is open or less than 2 V, the internal reference voltage source is applied. When the internal reference voltage source is used, the pin should be connected to the AG pin.
When an external reference voltage source is used, the power dissipation of this device is reduced by 20%, and the external reference voltage should be +2.5 V ±5%.

V_{DD} pin 8

Positive voltage power supply.
The range of supply voltage is +5 V ±5%.

PCMIN pin 9

PCM signal input.

The serial input PCM signal is converted from digital to analog, synchronizing with the synchronous signal RSYNC and clock signal RCLOCK.

The data rate of PCM signal is one of 512, 1024, 1536, 1544, and 2048 kbps.

The PCM signal is read at the falling edge of the clock signal and latched into the internal register when finished to read eight bits data.

The top of the PCM data is specified by RSYNC pulse timing.

RCLOCK pin 10

Receive clock pulse input.

The frequency of this clock pulse should be identified with the data rate of PCM input signal at the PCMIN pin.

This clock pulse needs to be continious signal, and is used for the clock signal in SCF filter and timing signal in D/A converter by directly dividing this frequency count.

The frequency deviation must be in ±50 ppm or less, to guarantee frequency characteristics of the filter. But where the frequency characteristics of an applied system is not specified exactly, the RCLOCK clock pulse count's between pules of RSYNC are allowed within the range of table shown below, for the normal operation mode.

But the electrical characteristics of this device can not be guaranteed.

PCMIN Data Rate	Clock Pulse Count between RSYNC Pulses		
	Ave.	Min.	Max.
512 kbps	64	64	65
1024 kbps	128	127	130
1536 kbps	192	190	195
1544 kbps	193	190	195
2048 kbps	256	253	257

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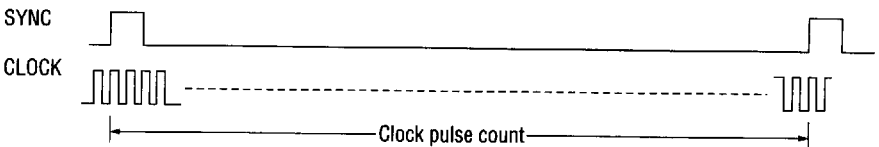
RSYNC pin 11

Receive synchronizing signal input.
Eight required bits are selected from serial PCM signals on the PCMIN pin by the receive synchronizing signal.
The whole timing signal in the receive section are synchronized by this synchronizing signal.
This signal must be synchronize in phase with RCLOCK.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics of receive section.
However, same as the RCLOCK frequency, this device can operate in the range of 8 kHz ±4 kHz, with no guarantee of adherence to the electrical characteristics in this specification as a catalogue value.
Fixing this signal to logic "1" or "0", the receive circuit is driver in a power down state.

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BS pin 12

Control signal input for decoding seven bits signal.
The PCM signal from first bit through seventh bit in a frame including the transition point of a signal to this pin, is decoded. The least significant bit is invalid.
Normally, this pin is fixed level "H" or "L".
The MSM6963 does not include this function.

DG pin 13

Ground for digital signal.
This pin is not connected to the AG pin.

XSYNC pin 14

Transmit synchronizing signal input.
The PCM output signal from PCMOUT pin is output in synchronization with this transmit synchronizing signal.
All transmit timing signals are triggered to synchronize with this signal. This signal should be synchronized in phase with XCLOCK pulse.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics of transmit section.
In the frequency range of 8 kHz ±4 kHz, even if the device circuit operates, same as on XCLOCK, the specification for the electrical characteristics is not guaranteed.
Fixing this signal to logic "1" or "0", the transmit circuit is driver in a power down state.

XCLOCK pin 15

Transmit clock input.

The PCM output data rate from the PCMOUT pin is set by this clock frequency.

The usable clock frequency is one of 512, 1024, 1536, 1544, and 2048 kHz.

This clock pulse must to be a continuous signal since the clock pulse is used as the clock pulse of SCF filter and the timing signal of A/D convertion.

To guarantee the frequency characteristics of the filter, the frequency deviation of the clock signal must be ±50 ppm or less.

However when the frequency characteristic of an applicate system is not specified exactly, if the XCLOCK clock counts in between the pulses of signal XSYNC are allowed in the range of table shown below, the device operates but the specified electrical characteristics is not guaranteed.

Clock Frequency	Clock Pulse Count between XSYNC Pulse Period		
	Ave.	Min.	Max.
512 kHz	64	64	65
1024 kHz	128	127	130
1536 kHz	192	190	195
1544 kHz	193	190	195
2048 kHz	256	253	257
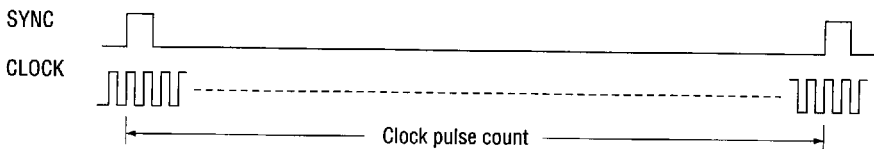
PCMOUT pin 16

PCM signal output.

The PCM output signal is output in synchronization with the rising edge of XCLOCK pulse orderly from MSB first. (The first bit of the PCM signal may output at the rising edge of XSYNC pulse, according to mutual timing of XSYNC and XCLOCK pulse.). During the PCMOUT signal output except the 8 bit-pulses, the pin is in an open state, therefore, multiple connections by wired-OR are easily possible at this pin.

The code companding law and output code format depend on ITU-T Recommendation G. 711, and for the MSM6963 (A-law) the output PCM signals are obtained by inverting the even bits of signals.

Input/Output	PCMIN/PCMOUT														
Level	MSM6962 (μ-law)								MSM6963 (A-law)							
+Full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
+0	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
-0	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
-Full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
	V_{SS}	—	−7 to 0	V
Reference Voltage	V_{REF}	—	0 to V_{DD}	V
Analog Input Voltage	V_{AIN}	—	V_{DD} −0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{op}	—	−10 to 80	°C
Storage Temperature	T_{STG}	—	−55 to 150	°C

RECOMMENDED OPERATING CONDITIONS
(Ta = 0°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.75	5	5.25	V
	V_{SS}	—	−5.25	−5	−4.75	V
Reference Voltage	V_{REF}	When using external V_{REF}	2.475	2.5	2.525	V
Analog Input Voltage	V_{AIN}	—	—	—	5	V_{P-P}
Input High Voltage	V_{IH}	XSYNC, XCLOCK, PCMIN,	2.0	2.4	V_{DD}	V
Input Low Voltage	V_{IL}	RSYNC, RCLOCK, TMC, BS	0	0	0.8	V
Clock Frequency	f_C	XCLOCK, RCLOCK	—	512, 1024 1536, 1544, 2048	—	kHz
Sync Pulse Frequency	f_S	XSYNC, RSYNC	—	8	—	kHz
Clock Duty Ratio	D_L	XCLOCK, RCLOCK	40	50	60	%
Digital Input Rise Time	t_{Ir}	XSYNC, XCLOCK, PCMIN,	—	—	50	ns
Digital Input Fall Time	t_{If}	RSYNC, RCLOCK (Fig. 1)	—	—	50	ns
Transmit Sync Timing	t_{XS}	XCLOCK→XSYNC (Fig. 2)	50	—	—	ns
	t_{SX}	XSYNC→XCLOCK (Fig. 2)	100	—	—	ns
Receive Sync Timing	t_{RS}	RCLOCK→RSYNC (Fig. 2)	50	—	—	ns
	t_{SR}	RSYNC→RCLOCK (Fig. 2)	100	—	—	ns
Transmit Sync Pulse Width	t_{WX}	—	1/fc	—	117	μs
Receive Sync Pulse Width	t_{WR}	—	1/fc	—	117	μs
PCMIN Set-up Time	t_{DS}	—	100	—	—	ns
PCMIN Hold Time	t_{DH}	—	100	—	—	ns
BS Set-up Time *	t_{BS}	—	200	—	—	ns
BS Hold Time *	t_{BH}	—	200	—	—	ns
Analog Output Load	R_{AL}	AOUT	10	20	—	kΩ
	C_{AL}		—	—	100	pF
Digital Output Load	R_{DL}	PCMOUT	1	—	—	kΩ
	C_{DL}		—	—	100	pF
Allowable Analog Input Offset Voltage	V_{IO}	—	−200	—	200	mV

* : The value for the MSM6962

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

$(V_{DD} = +5\text{ V} \pm 5\%, V_{SS} = -5\text{ V} \pm 5\%, Ta = 0°C\text{ to }70°C)$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	XCLOCK, RCLOCK	—	5.5	11	mA
(Operating)	I_{SS1}	2048 kHz	—	5.0	11	
Power Supply Current	I_{DD2}	—	—	0.8	3.0	mA
(Stand-by)	I_{SS2}		—	0.3	1.5	
Reference Current	I_{REF}	When external V_{REF} input.	—	5	100	µA
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input Leakage Current	I_{IH}		—	< 0.5	2.0	µA
	I_{IL}	—	—	< 0.2	0.5	
Output Low Voltage	V_{OL}		—	0.1	0.4	V
Output Leakage Current	I_{OH}		—	< 5	10	µA
Analog Output Offset Voltage	V_{OFF}		−150	0	150	mV
Input Capacitance	C_{IN}	Except for AIN	—	5	—	pF
		AIN	—	5	—	
Analog Input Resistance	R_{IN}	$f_{IN} < 3.4$ kHz	—	1	—	MΩ

AC Characteristics

$(V_{DD} = +5 \text{ V} \pm 5\%, V_{SS} = -5 \text{ V} \pm 5\%, Ta = 0°C \text{ to } 70°C)$

Parameter	Symbol	Condition Freq. (Hz)	Condition Level (dBmO)		Min.	Typ.	Max.	Unit
Transmit Frequency Response	L_{OSS} T1	60			20	26	—	dB
	L_{OSS} T2	300			−0.1	−0.03	0.2	
	L_{OSS} T3	820	0		Reference			
	L_{OSS} T4	2020			−0.1	0.0	0.2	
	L_{OSS} T5	3000			−0.1	0.10	0.2	
	L_{OSS} T6	3400			0	0.45	0.8	
Receive Frequency Response	L_{OSS} R1	300			−0.1	−0.02	0.2	dB
	L_{OSS} R2	820			Reference			
	L_{OSS} R3	2020	0		−0.1	0.0	0.2	
	L_{OSS} R4	3000			−0.1	0.10	0.2	
	L_{OSS} R5	3400			0	0.65	0.8	
Transmit Signal to Distortion Ratio *1	SD T1		3		37	43	—	dB
	SD T2	1020	0		37	41	—	
	SD T3	or	−30		37	40	—	
	SD T4	820	−40	*2	32/31	34.5/33	—	
	SD T5		−45	*2	28/26	31/28.5	—	
Receive Signal to Distortion Ratio *1	SD R1		3		37	44	—	dB
	SD R2	1020	0		37	41	—	
	SD R3	or	−30		37	41	—	
	SD R4	820	−40	*2	32/32	35.5/35	—	
	SD R5		−45	*2	28/26	34/28.5	—	
Transmit Gain Tracking	GT T1		3		−0.2	−0.01	0.2	dB
	GT T2	1020	−10		Reference			
	GT T3	or	−40		−0.2	0.05	0.2	
	GT T4	820	−50		−0.4	0.25	0.4	
	GT T5		−55		−0.8	0.10	0.8	
Receive Gain Tracking	GT R1		3		−0.2	0.02	0.2	dB
	GT R2	1020	−10		Reference			
	GT R3	or	−40		−0.2	−0.05	0.2	
	GT R4	820	−50		−0.4	−0.16	0.4	
	GT R5		−55		−0.8	−0.31	0.8	

Notes: *1   The measurement is taken with P-message filter
          *2   The value before "/" is for the MSM6962 and the value after "/" for the MSM6963
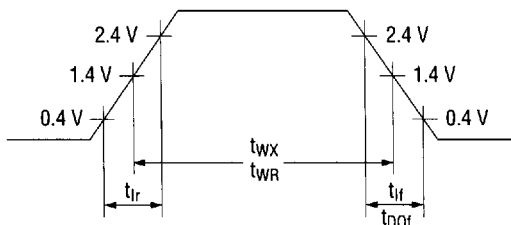
AC Characteristics (Continued)

$(V_{DD} = +5\ V \pm 5\%,\ V_{SS} = -5\ V \pm 5\%,\ Ta = 0°C\ to\ 70°C)$

Parameter		Symbol	Condition Freq. (Hz)	Level (dBmO)		Min.	Typ.	Max.	Unit
Idle Channel	Transmit	N_{IDL} T	—	—		—	−89	−75	dBmOp
Noise *1	Receive	N_{IDL} R	—	—		—	−89	−75	
Absolute Gain *3	Transmit	AV T	1020 or 820	0		−0.5	0	0.5	dB
	Receive	AV R	1020 or 820	0		−0.5	0	0.5	
Absolute Delay Time		t_D	—	0		—	0.47	0.5	ms
		t_{GD} T1	500			—	0.2	0.75	
		t_{GD} T2	600			—	0.1	0.35	
Transmit Group Delay Time *4		t_{GD} T3	1000	0		—	0	0.125	ms
		t_{GD} T4	2600			—	0.05	0.125	
		t_{GD} T5	2800			—	0.07	0.75	
		t_{GD} R1	500			—	−0.02	0.75	
		t_{GD} R2	600			—	−0.02	0.35	
Receive Group Delay Time *4		t_{GD} R3	1000	0		—	−0.03	0.125	ms
		t_{GD} R4	2600			—	0.07	0.125	
		t_{GD} R5	2800			—	0.10	0.75	
Crosstalk Attenuation	T to R	C_R T	1020 or 820	—		—	78	66	dB
	R to T	C_R R	1020 or 820			—	90	66	
Out-of-Band Spurious		S	300 to 3400	0		−30	−33	—	dBmO
Intermodulation Distortion		IMD 1	$f_a = 470$ $f_b = 320$	−4	$2 \times f_a - f_b$	—	−40	−35	dBmO
Discrimination		DIS	4.6 kHz to 72 kHZ	0		30	32	—	dB
V_{DD} Noise Rejection	Transmit	PPSR T	0 to 300 kHz	200 mVp-p		—	30	—	dB
Ratio	Receive	PPSR R				—	30	—	
V_{SS} Noise Rejection	Transmit	NPSR T				—	30	—	
Ratio	Receive	NPSR R				—	30	—	
		t_{SD}				50	150	300	ns
Digital Output Delay Time		t_{XD1}	$R_{DL} = 2\ k\Omega$			50	100	300	
		t_{XD2}	$C_{DL} = 100\ pF$			50	100	300	
		t_{XD3}				50	180	300	
Digital Output Fall Time		t_{DO}				—	20	100	ns

Notes:　*1　The measurement is taken with P-message filter
　　　　*2　The value before "/" is for the MSM6962 and the value after "/" for the MSM6963
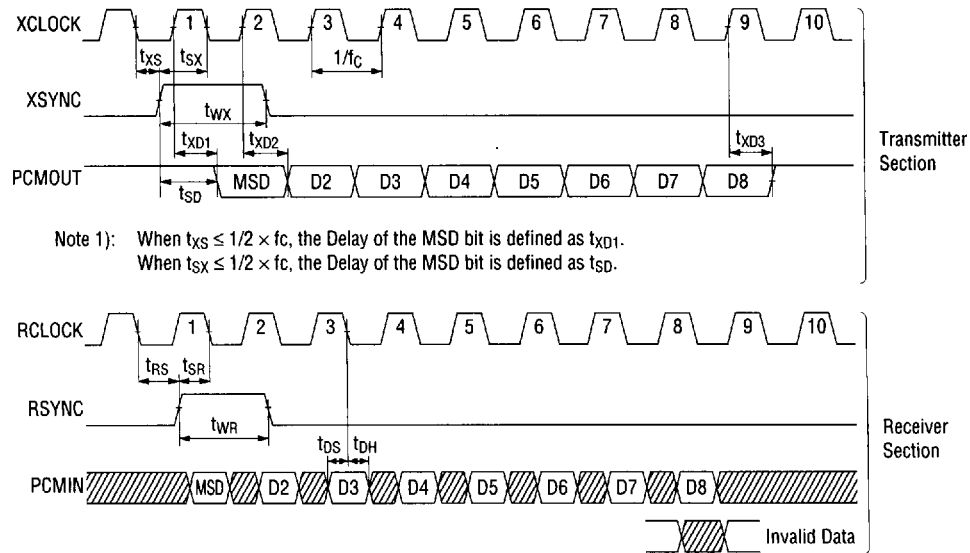　　　　*3　0 dB ÷ 1.252 Vrms
　　　　*4　Reference : 1800 Hz

TIMING DIAGRAM

Wave Time Measurement Level

2.4 V   2.4 V
1.4 V   1.4 V
0.4 V   0.4 V

t_{WX}
t_{WR}

t_{lr} t_{lf}
t_{DOf}

Note: Timing between signal waves is judged at 1.4 V

Figure 1

3

Basic Timing

XCLOCK

t_{XS} t_{SX} $1/f_C$

XSYNC

t_{WX}

t_{XD1} t_{XD2} t_{XD3}

Transmitter Section

PCMOUT t_{SD} MSD   D2   D3   D4   D5   D6   D7   D8

Note 1):   When $t_{XS} \leq 1/2 \times fc$, the Delay of the MSD bit is defined as t_{XD1}.
When $t_{SX} \leq 1/2 \times fc$, the Delay of the MSD bit is defined as t_{SD}.

RCLOCK

t_{RS} t_{SR}

RSYNC

t_{WR}

t_{DS} t_{DH}

Receiver Section

PCMIN   MSD   D2   D3   D4   D5   D6   D7   D8

Invalid Data

Note 2):   Transmit synchronizing and clock pulse, and Receive synchronizing and clock pulse may be asynchronous mutually.
Note 3):   The threshold level is 1.4 V.

Figure 2

Timing for 7 Bits Decode (Specified for MSM6962)
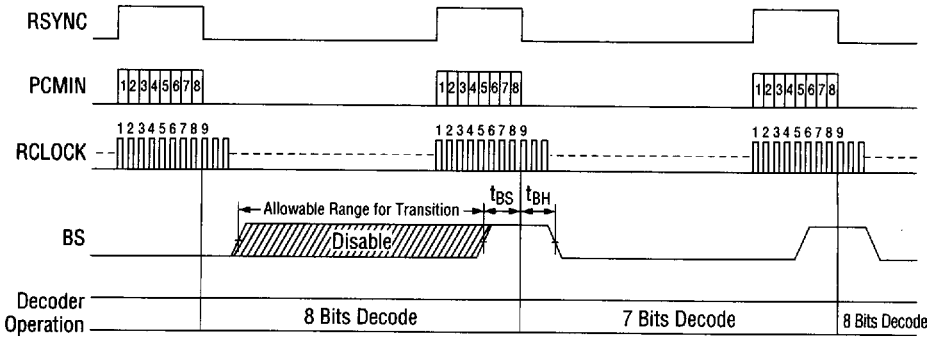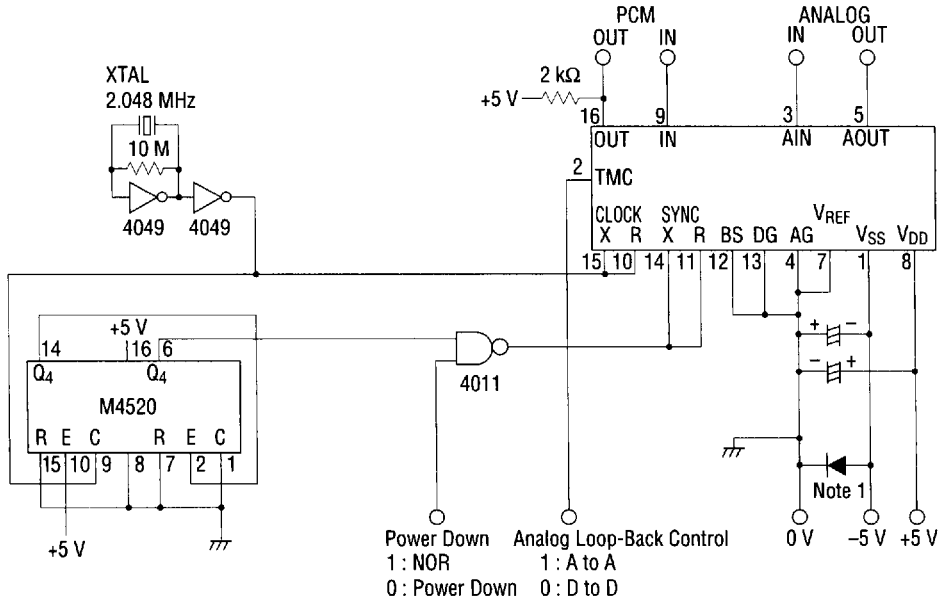

Figure 3

⋮ ■ 6724240 0021299 787 ■

APPLICATION CIRCUIT

### Basic Circuit

Notes: 1. Insert diode for preventing from Latch-Up at turn on Power.
Recommended Diode Specification.
- High Speed Switching
- Allowable Power dissipation 250 mW to 300 mW
- Forward Voltage Drop <1.3 V (at 100 mA)
2. AG and DG must be connected in the printed circuit board mounted this device, for preventing from Latch-Up.
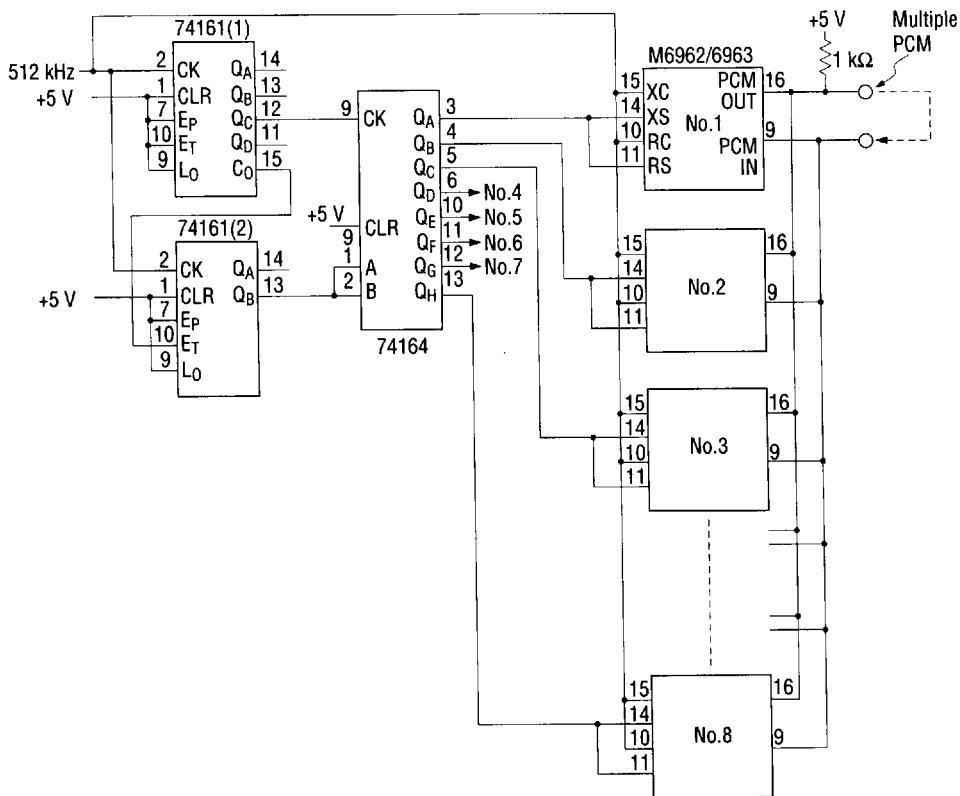
Four-Wire Line Connection

Connections of power source and clock depend on the basic circuit.
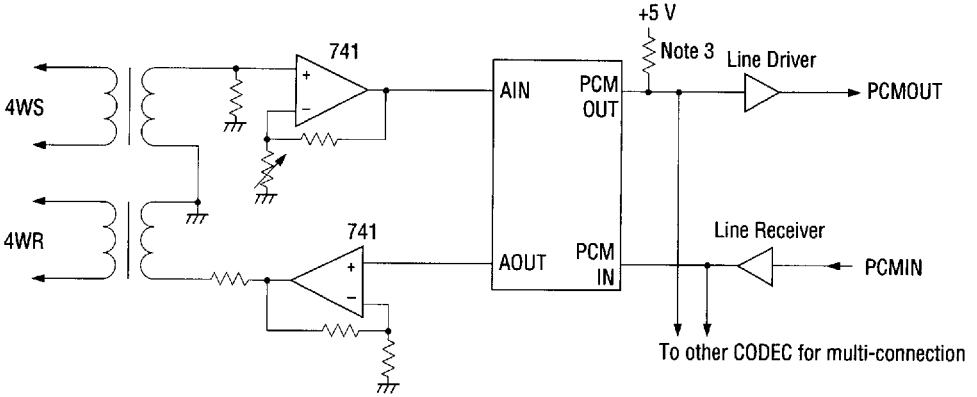
Note: 3.   In the case of multi-connection to other CODEC, the pull-up resistance is possibly 1 kΩ
up to a maximum of 8 CODECs.
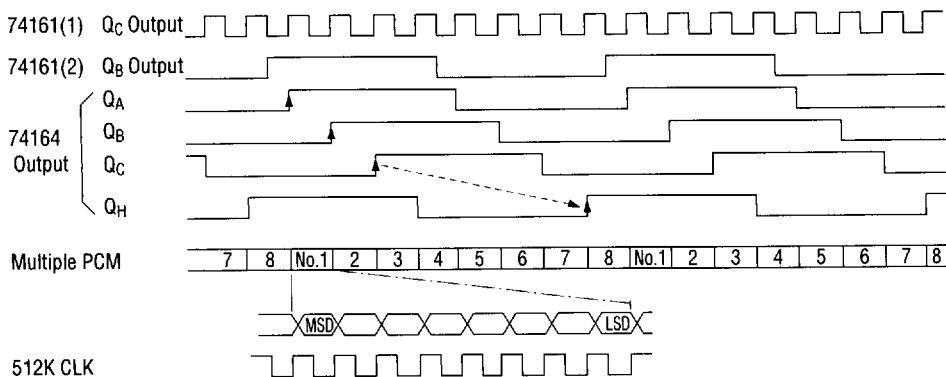In this case, take notice that the delay of PCMOUT is larger.

Example of Multi-Channel Connections (8ch)

Example of Multi-Channel Timing

RECOMMENDATIONS FOR ACTUAL DESIGN

* To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.

* Connect the AG pin and the DG pin each other as close as possible.
  Connected to the system ground with low impedance.

* Mount the device directly on the board when mounted on printed circuit board.
  Do not use IC sockets.
  If an IC socket is unavoidable, use the short lead type socket.

* When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.

* Keep the voltage on the V_{DD} pin not lower than –0.3 V and the voltage on the V_{SS} pin more than +0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.

* Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

6724240 0021303 T38