

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90945 Series

### MB90F946A/947A/F947/F947A/F949/F949A/ V390HA/V390HB

#### ■ DESCRIPTION

The MB90945 series with one FULL-CAN\* interface and FLASH ROM is especially designed for automotive HVAC applications. Its main feature is the on board CAN\* Interface, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal FULL-CAN\* approach. With the new 0.35  $\mu\text{m}$  CMOS technology, Fujitsu now offers on-chip FLASH-ROM program memory up to 384 K bytes. An internal voltage booster removes the necessity for a second programming voltage.

An on board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

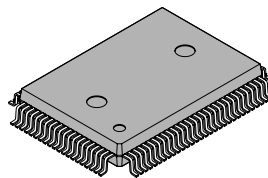
The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features a 4-channel Output Compare Unit and a 6-channel Input Capture Unit with two separate 16-bit free running timers. Up to 3 UARTs, one Serial I/O and one I<sup>2</sup>C constitute additional functionality for communication purposes.

\* : Controller Area Network (CAN) - License of Robert Bosch GmbH

#### ■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

# MB90945 Series

## ■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 42 ns instr. cycle time)
- New 0.35  $\mu\text{m}$  CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- One FULL-CAN interface; conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 8 external interrupts)
- EI<sup>2</sup>OS - Automatic transfer function independent of CPU; 16 channels of intelligent I/O Services
- 18-bit Time-base counter
- Watchdog Timer
- 1 full duplex UART; support 10.4 KBaud (USA standard)
- up to 2 full duplex UARTs (LIN/SCI/SPI)
- 1 Serial I/O (SPI)
- 1 I<sup>2</sup>C interface
- A/D Converter : 15 channels analog inputs (Resolution 10-bit or 8-bit)
- 16-bit reload timer  $\times$  1 channel
- ICU (Input capture) 16-bit  $\times$  6 channels
- OCU (Output compare) 16-bit  $\times$  4 channels
- 16-bit free running timer  $\times$  2 channels (FRT0 : ICU 0/1, OCU 0/1/2/3, FRT1 : ICU 2/3/4/5)
- 8/16-bit Programmable Pulse Generator 6 channels  $\times$  8/16-bit
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16-bit  $\times$  16-bit) and divide (32-bit/16-bit) instructions available
- Program Patch Function (3 address match registers)
- Fast Interrupt processing
- Low Power Consumption mode
  - Sleep mode
  - Timebase timer mode
  - Stop mode
  - CPU intermittent mode
- Automotive input levels
- Package : 100-pin plastic QFP

# MB90945 Series

## ■ PRODUCT LINEUP

Part Number Parameter	MB90947A	MB90F946A	MB90F947, MB90F947A MB90F949, MB90F949A	MB90V390HA MB90V390HB
CPU	F <sup>2</sup> MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz oscillation clock, PLL clock multiplied by 6)			
ROM	ROM memory 128 Kbytes	Boot-block Flash memory 384 Kbytes	Boot-block Flash memory 256 Kbytes: MB90F949 MB90F949A 128 Kbytes: MB90F947 MB90F947A	External
RAM	6 Kbytes	16 Kbytes	12 Kbytes: MB90F949 MB90F949A 6 Kbytes: MB90F947 MB90F947A	30 Kbytes
Emulator-specific power supply <sup>1</sup>	—			Yes
Technology	0.35 μm CMOS with on-chip voltage regulator for internal power supply	0.35 μm CMOS with on-chip voltage regulator for internal power supply + Flash memory with on-chip charge pump for programming voltage		0.35 μm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 V to 5.5 V : other than conditions listed below 4.0 V to 5.5 V : when writing to Flash 4.5 V to 5.5 V : if A/D Converter is used			5 V ± 10%
Temperature range	-40 °C to +105 °C			—
Package	QFP-100P			PGA-299C
UART	1 channel			2 channels
	Full duplex double buffer Supports asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 20 MHz			
UART (LIN/SCI/SPI)	1 channel	2 channels	1 channel	2 channels
Serial I/O	1 channel Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 20 MHz			
I <sup>2</sup> C (400 Kbps)	1 channel			

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# MB90945 Series

Part Number Parameter	MB90947A	MB90F946A	MB90F947, MB90F947A MB90F949, MB90F949A	MB90V390HA MB90V390HB
A/D Converter (15 input channels)	10-bit or 8-bit resolution Conversion time : Min 4.9 $\mu$ s includes sample time (per one channel, only at certain machine clock frequencies)			
16-bit Reload Timer	1 channel		2 channels	
	Operation clock frequency : $f_{sys}/2^1$ , $f_{sys}/2^3$ , $f_{sys}/2^5$ ( $f_{sys}$ = System clock frequency) Supports External Event Count function			
16-bit I/O Timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (ch0) Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ , $f_{sys}/2^5$ , $f_{sys}/2^6$ , $f_{sys}/2^7$ ( $f_{sys}$ = System clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 2/3/4/5			
16-bit Input Capture (6 channels)	Rising edge, falling edge or rising & falling edge sensitive Six 16-bit Capture registers Signals an interrupt upon external event			
	—		ICU 3/5 inputs are shared with OCU 6/7 outputs	
16-bit Output Compare	4 channels		8 channels	
	Signals an interrupt when a match with 16-bit I/O Timer Eight 16-bit compare registers. A pair of compare registers can be used to generate an output signal.			
	—		ICU 3/5 inputs are shared with OCU 6/7 outputs	
8/16-bit Programmable Pulse Generator (6 channels)	Supports 8-bit and 16-bit operation modes Twelve 8-bit reload counters Twelve 8-bit reload registers for L pulse width Twelve 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ or 102.4 $\mu$ s ( $f_{osc}$ = 5 MHz) ( $f_{sys}$ = System clock frequency, $f_{osc}$ = Oscillation clock frequency)			
CAN Interface	1 channel		5 channels	
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full-bit compare/Full-bit mask/Two partial bit masks Supports up to 1 Mbps <b>MB90F947/F949/V390HA:</b> Do not use clock modulation and CAN at the same time			

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# MB90945 Series

Part Number Parameter	MB90947A	MB90F946A	MB90F947, MB90F947A MB90F949, MB90F949A	MB90V390HA MB90V390HB
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive			
Stepping motor controller	—		2 channels	
Watch Timer	—		1 channel	
Sound generator	—		1 channel	
Machine clock output	—		2 channels (non-inverted and inverted)	
Program patch function	3 address match registers		5 address match registers	
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal			
	Automotive input level (P21/RX1, P42/SDA, P43/SCL have CMOS Schmitt input level)		Port-wise programmable as Automotive (default) or CMOS Schmitt input level	
I/O Ports with 4 mA CMOS output	All ports except P42, P43		All ports except P80, P81, PA0 to PA7, P42, P43	
I/O Ports with 3 mA CMOS output	P42, P43		P42, P43	
I/O Ports with 30 mA CMOS output with slewrate control	—		P80, P81, PA0 to PA7	
Clock Modulator	Phase modulation mode		Phase modulation mode	Frequency and phase modulation mode
			<b>MB90F947/F949/V390HA:</b> Do not use clock modulation and CAN at the same time	
	Reduces EMI by modulating the PLL clock			
Start-up time at power-on reset	3 × 2 <sup>16</sup> oscillation cycles (49.152 ms at 4 MHz oscillation) + oscillation time of oscillator*2		2 <sup>18</sup> oscillation cycles (65.536 ms at 4 MHz oscillation) + oscillation time of oscillator*2	

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# MB90945 Series

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Part Number Parameter	MB90947A	MB90F946A	MB90F947, MB90F947A MB90F949, MB90F949A	MB90V390HA MB90V390HB
Flash Memory	—	Supports automatic programming, Embedded Algorithm™*3 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years*4 Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory (address FFA000 <sub>H</sub> , mode data 00 <sub>H</sub> ) Boot block configuration Erase can be performed on each block Block protection with external programming voltage Write and erase at F <sub>max</sub> = 20 MHz		—

\*1 : It is setting of Jumper switch SI when Emulation Pod (MB2147) is used.  
Please refer to the Emulator hardware manual about details.

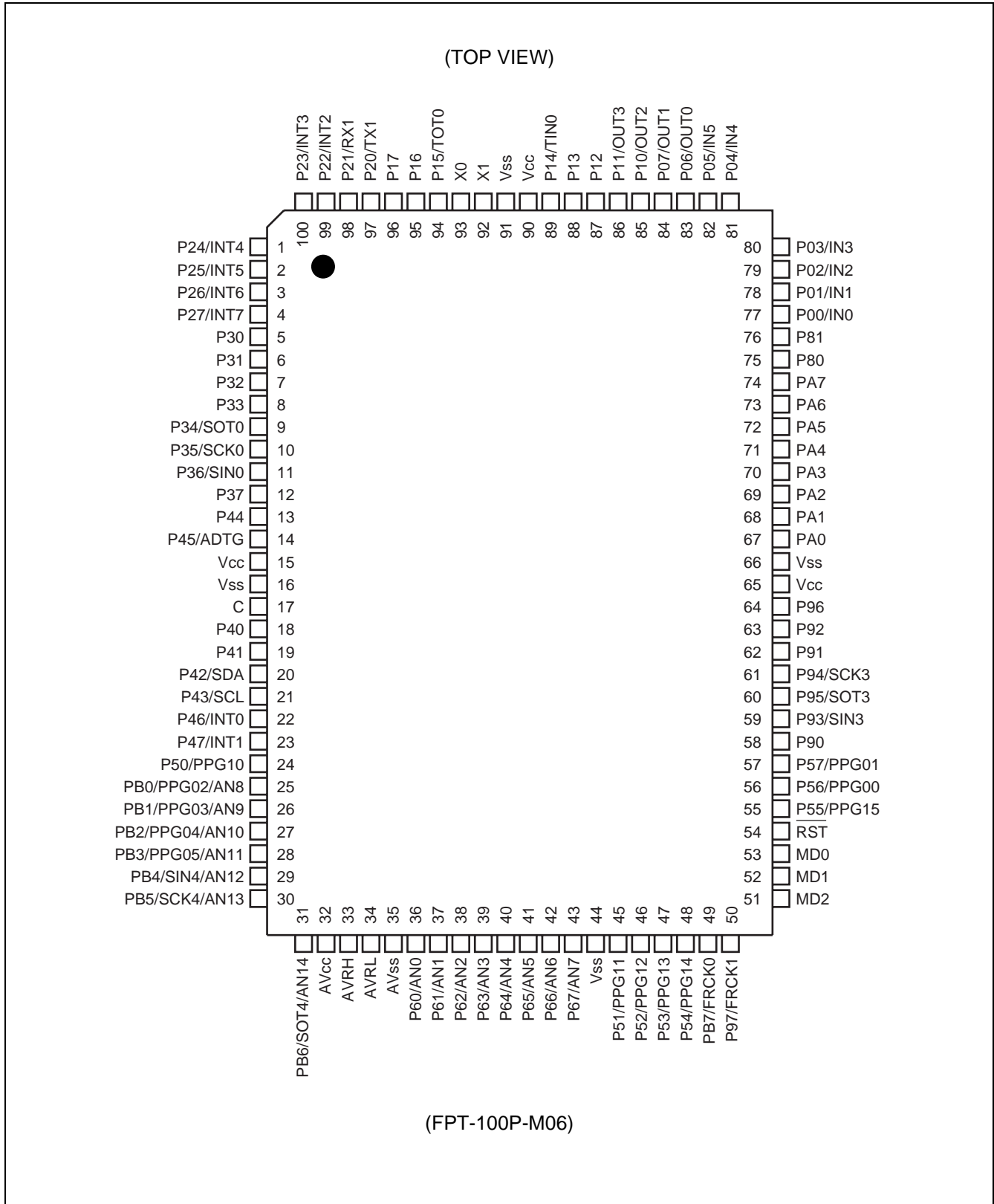
\*2 : Oscillation time of the oscillator is the time that the amplitude reaches 90%.

\*3 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

\*4 : Data is based on reliability tests during process qualification (the value for T<sub>A</sub> = + 85 °C is calculated via the Arrhenius formula from data of accelerated measurements at elevated temperature) .

## ■ PIN ASSIGNMENTS

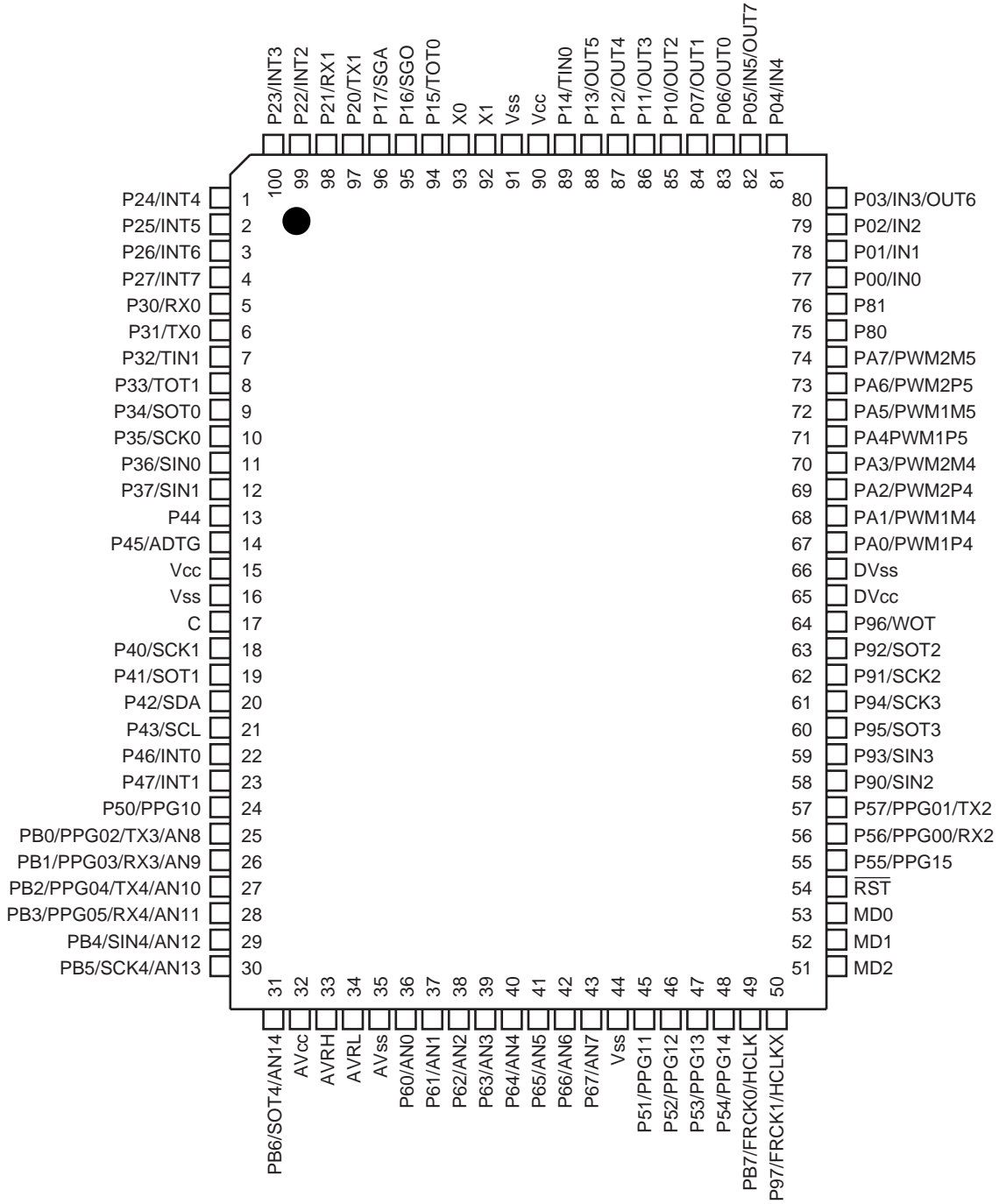
- MB90947A/F946A/F947/F947A/F949/F949A



# MB90945 Series

• MB90V390HA/V390HB

(TOP VIEW)



(FPT-100P-M06)

As seen with QFP100 probe cable



## ■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
92	X1	A	Pin for oscillation
93	X0		Pin for oscillation
54	$\overline{\text{RST}}$	B	Reset input
77 to 82	P00 to P05	D	General purpose I/O
	IN0 to IN5		Inputs for the Input Captures 0-5
83 to 86	P06, P07 P10, P11	D	General purpose I/O
	OUT0 to OUT3		Outputs for the Output Compares
87, 88	P12, P13	D	General purpose I/O
89	P14	D	General purpose I/O
	TIN0		TIN0 input for the 16-bit Reload Timer 0
94	P15	D	General purpose I/O
	TOT0		TOT0 output for the 16-bit Reload Timer 0
95, 96	P16, P17	D	General purpose I/O
97	P20	D	General purpose I/O
	TX1		TX output for CAN Interface 1
98	P21	F	General purpose I/O
	RX1		RX input for CAN Interface 1
99, 100 1 to 4	P22 to P27	D	General purpose I/O
	INT2 to INT7		External interrupt inputs for INT2 to INT7
5 to 8	P30 to P33	D	General purpose I/O
9	P34	D	General purpose I/O
	SOT0		SOT output for UART0
10	P35	D	General purpose I/O
	SCK0		SCK input/output for UART0
11	P36	D	General purpose I/O
	SIN0		SIN input for UART0
12	P37	D	General purpose I/O
13	P44	D	General purpose I/O
14	P45	D	General purpose I/O
	ADTG		External trigger input of the A/D Converter
18, 19	P40, P41	D	General purpose I/O
20	P42	F	General purpose I/O
	SDA		Serial data for I <sup>2</sup> C interface

(Continued)

# MB90945 Series

Pin no.	Pin name	Circuit type	Function
21	P43	F	General purpose I/O
	SCL		Serial clock for I <sup>2</sup> C interface
22, 23	P46, P47	D	General purpose I/O
	INT0, INT1		External interrupt inputs for INT0, INT1
24	P50	D	General purpose I/O
	PPG10		Output for the PPG1
25 to 28	PB0 to PB3	E	General purpose I/O
	PPG02 to PPG05		Outputs for the PPG4, 6, 8, A
	AN8 to AN11		Inputs for the A/D Converter
29	PB4	E	General purpose I/O
	SIN4		SIN input for Serial I/O
	AN12		Input for the A/D Converter
30	PB5	E	General purpose I/O
	SCK4		SCK input/output for Serial I/O
	AN13		Input for the A/D Converter
31	PB6	E	General purpose I/O
	SOT4		SOT output for Serial I/O
	AN14		Input for the A/D Converter
36 to 43	P60 to P67	E	General purpose I/O
	AN0 to AN7		Inputs for the A/D Converter
45 to 48	P51 to P54	D	General purpose I/O
	PPG11 to PPG14		Outputs for the PPG3, 5, 7, 9
49	PB7	D	General purpose I/O
	FRCK0		FRCK0 input for the 16-bit I/O Timer 0
50	P97	D	General purpose I/O
	FRCK1		FRCK1 input for the 16-bit I/O Timer 1
55	P55	D	General purpose I/O
	PPG15		Outputs for the PPGB
56, 57	P56, P57	D	General purpose I/O
	PPG00, PPG01		Outputs for the PPG0, PPG2
58	P90	D	General purpose I/O
	SIN2		SIN input for UART 2 (LIN/SCI/SPI) (only MB90V390HA, MB90V390HB and MB90F946A)
59	P93	D	General purpose I/O
	SIN3		SIN input for UART3 (LIN/SCI/SPI)

(Continued)

# MB90945 Series

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Pin no.	Pin name	Circuit type	Function
60	P95	D	General purpose I/O
	SOT3		SOT output for UART3 (LIN/SCI/SPI)
61	P94	D	General purpose I/O
	SCK3		SCK input/output for UART3 (LIN/SCI/SPI)
62	P91	D	General purpose I/O
	SCK2		SCK input/output for UART 2 (LIN/SCI/SPI) (only MB90V390HA, MB90V390HB and MB90F946A)
63	P92	D	General purpose I/O
	SOT2		SOT output for UART 2 (LIN/SCI/SPI) (only MB90V390HA, MB90V390HB and MB90F946A)
64	P96	D	General purpose I/O
67 to 74	PA0 to PA7	H	General purpose I/O. For the EVA device, these pins are high current outputs.
75, 76	P80, P81	H	General purpose I/O. For the EVA device, these pins are high current outputs.
32	AV <sub>cc</sub>	—	Dedicated power supply pin (5 V) for the A/D converter
33	AVRH	—	Dedicated pos. reference voltage pin for the A/D converter
34	AVRL	—	Dedicated neg. reference voltage pin for the A/D converter
35	AV <sub>ss</sub>	—	Dedicated power supply pin (0 V) for the A/D converter
52, 53	MD1, MD0	C	These are input pins used to designate the operating mode. They should be connected directly to V <sub>CC</sub> or V <sub>SS</sub> .
51	MD2	G	This is an input pin used to designate the operating mode. It should be connected directly to V <sub>CC</sub> or V <sub>SS</sub> .
15 65 90	V <sub>cc</sub>	—	These are power supply (5 V) input pins. For the EVA device, pin 65 is the DV <sub>CC</sub> supply pin for the high current outputs.
16 44 66 91	V <sub>ss</sub>	—	These are power supply (0 V) input pins. For the EVA device, pin 66 is the DV <sub>SS</sub> supply pin for the high current outputs.
17	C	—	This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 μF ceramic capacitor.

# MB90945 Series

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>Oscillation feedback resistor : 1 MΩ approx.</li> </ul>
B		<ul style="list-style-type: none"> <li>CMOS Hysteresis input with pull-up resistor : 50 kΩ approx.</li> </ul>
C		<ul style="list-style-type: none"> <li>EVA/ROM device : CMOS Hysteresis input</li> <li>Flash device : CMOS input.</li> </ul>
D		<ul style="list-style-type: none"> <li>CMOS output (4 mA)</li> <li>Automotive Hysteresis input</li> </ul>

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Type	Circuit	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS output (4 mA)</li> <li>• Automotive Hysteresis input</li> <li>• Analog input</li> </ul>
F		<ul style="list-style-type: none"> <li>• CMOS output P42, P43 : 3mA P21 : 4 mA</li> <li>• CMOS Hysteresis input</li> </ul>
G		<ul style="list-style-type: none"> <li>• EVA/ROM device : CMOS Hysteresis input with pull-down resistor : 50 kΩ approx.</li> <li>• Flash device : CMOS input without pull-down.</li> </ul>
H		<ul style="list-style-type: none"> <li>• EVA/ROM device : CMOS high current output (30 mA) with slewrate control</li> <li>• Flash device : CMOS output (4 mA)</li> <li>• Automotive Hysteresis input</li> </ul>

# MB90945 Series

## ■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins ( $V_{CC}/V_{SS}$ )
- Pull-up/pull-down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter if A/D Converter is unused.
- Caution on Operations during PLL Clock Mode

### 1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$ .
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AV_{RH}$ ) exceed the digital power-supply voltage.

### 2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified  $V_{CC}$  supply voltage operation range. Therefore, the  $V_{CC}$  supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that  $V_{CC}$  ripple variations (peak-to-peak values) at commercial frequencies (50 Hz to 60 Hz) fall below 10 % of the standard  $V_{CC}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

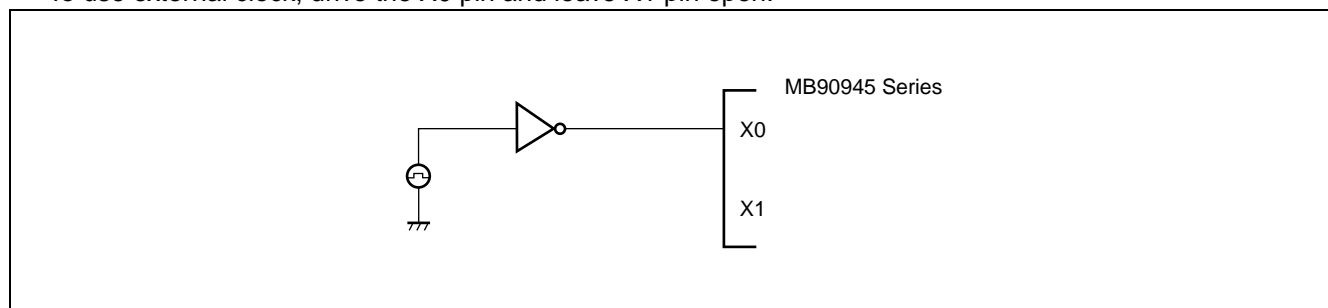
### 3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k $\Omega$  .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

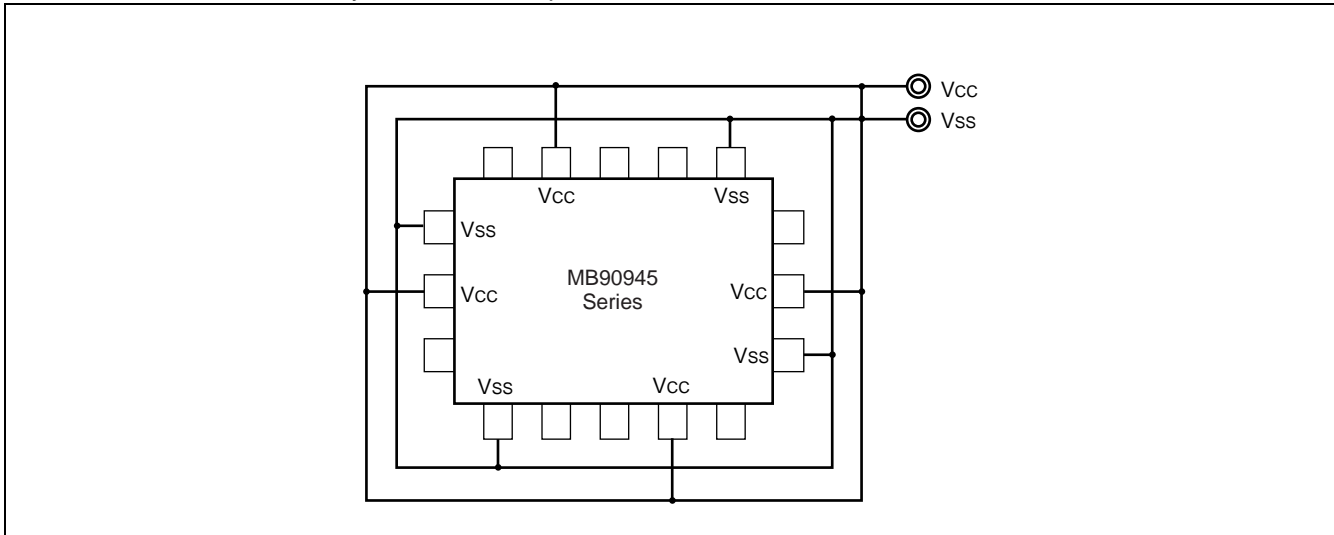
### 4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



## 5. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.  
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally.
- Connect  $V_{CC}$  and  $V_{SS}$  to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1  $\mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



## 6. Pull-up/pull-down resistors

The MB90945 series does not support internal pull-up/pull-down resistors option. Use external components where needed.

## 7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits while you design a printed circuit.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

## 8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ( $AV_{CC}$ ,  $AV_{RH}$ ,  $AV_{RL}$ ) and analog inputs ( $AN0$  to  $AN14$ ) after turning-on the digital power supply ( $V_{CC}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed  $AV_{RH}$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 9. Connection of Unused Pins of A/D Converter if A/D Converter is unused

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$ .

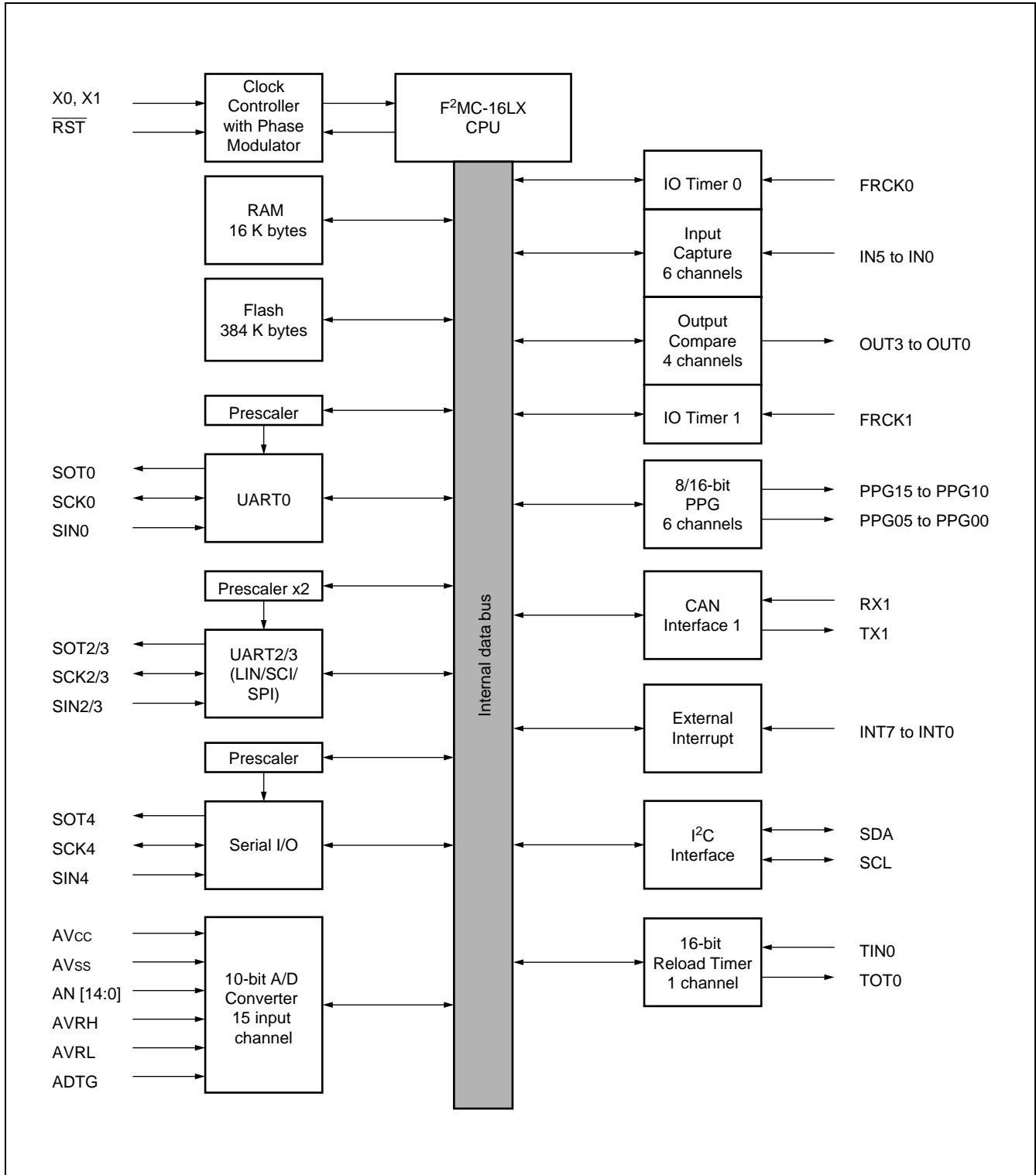
## 10. Notes on During Operation of PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

# MB90945 Series

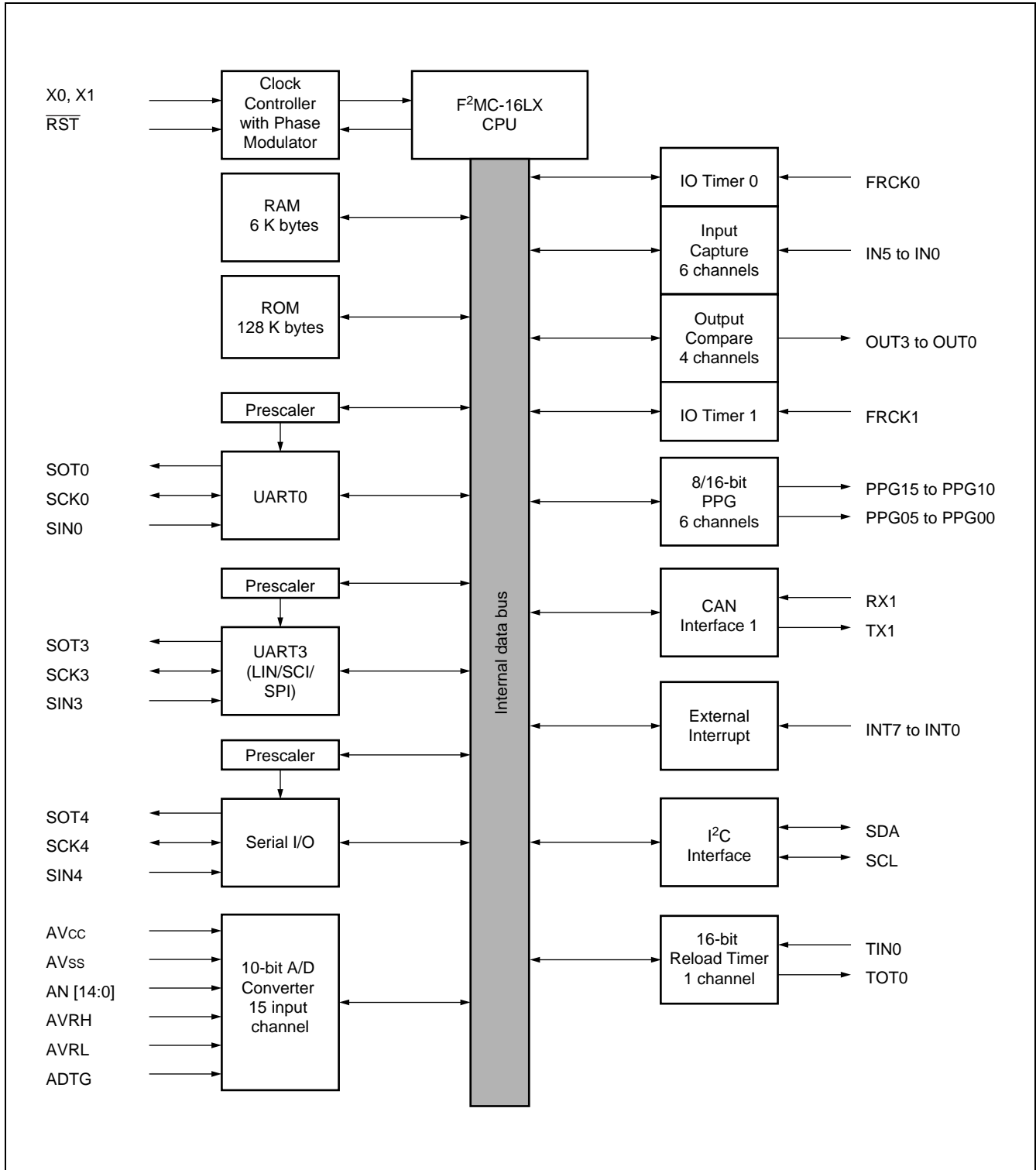
## ■ BLOCK DIAGRAMS

• MB90F946A



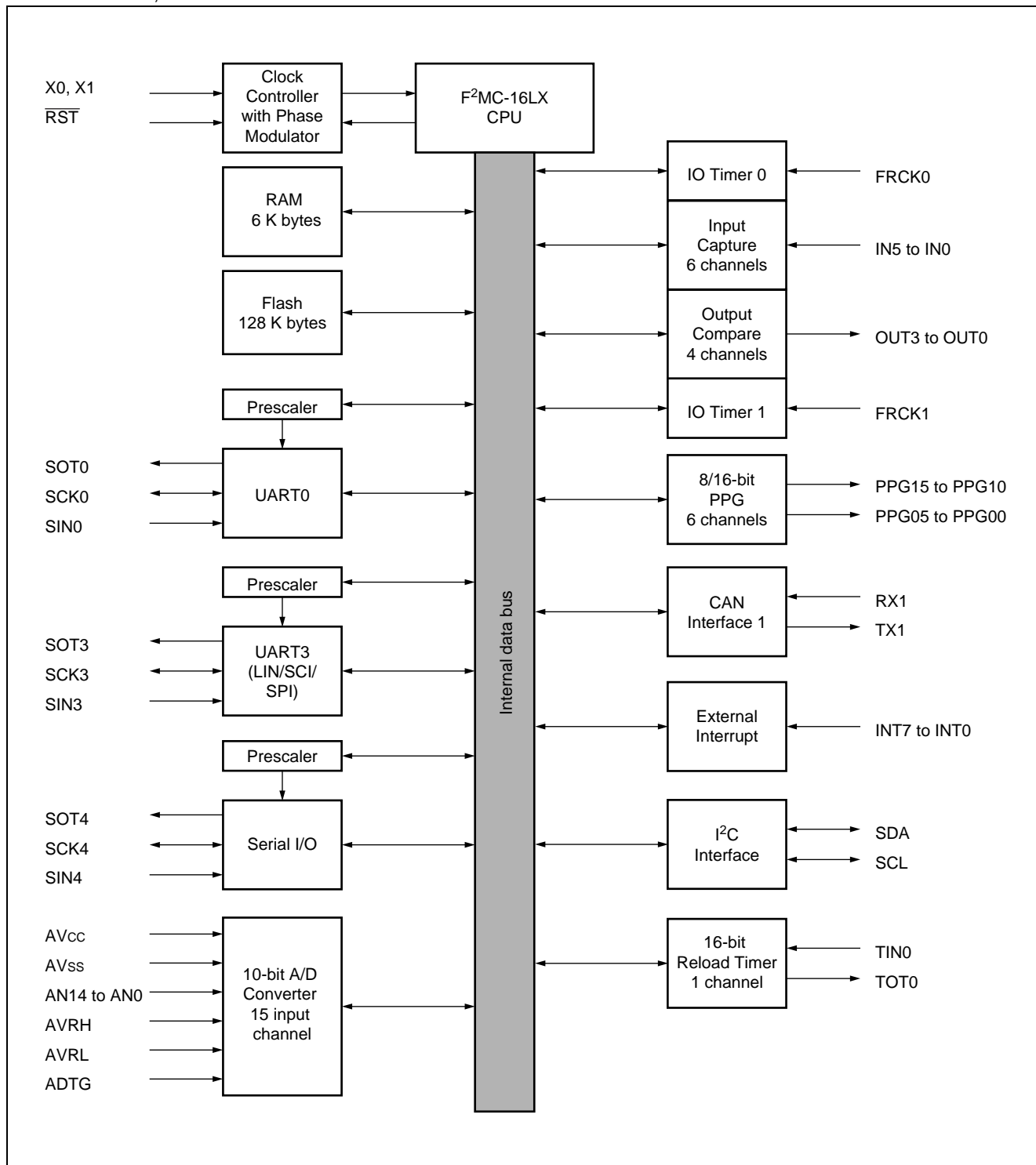


• MB90947A



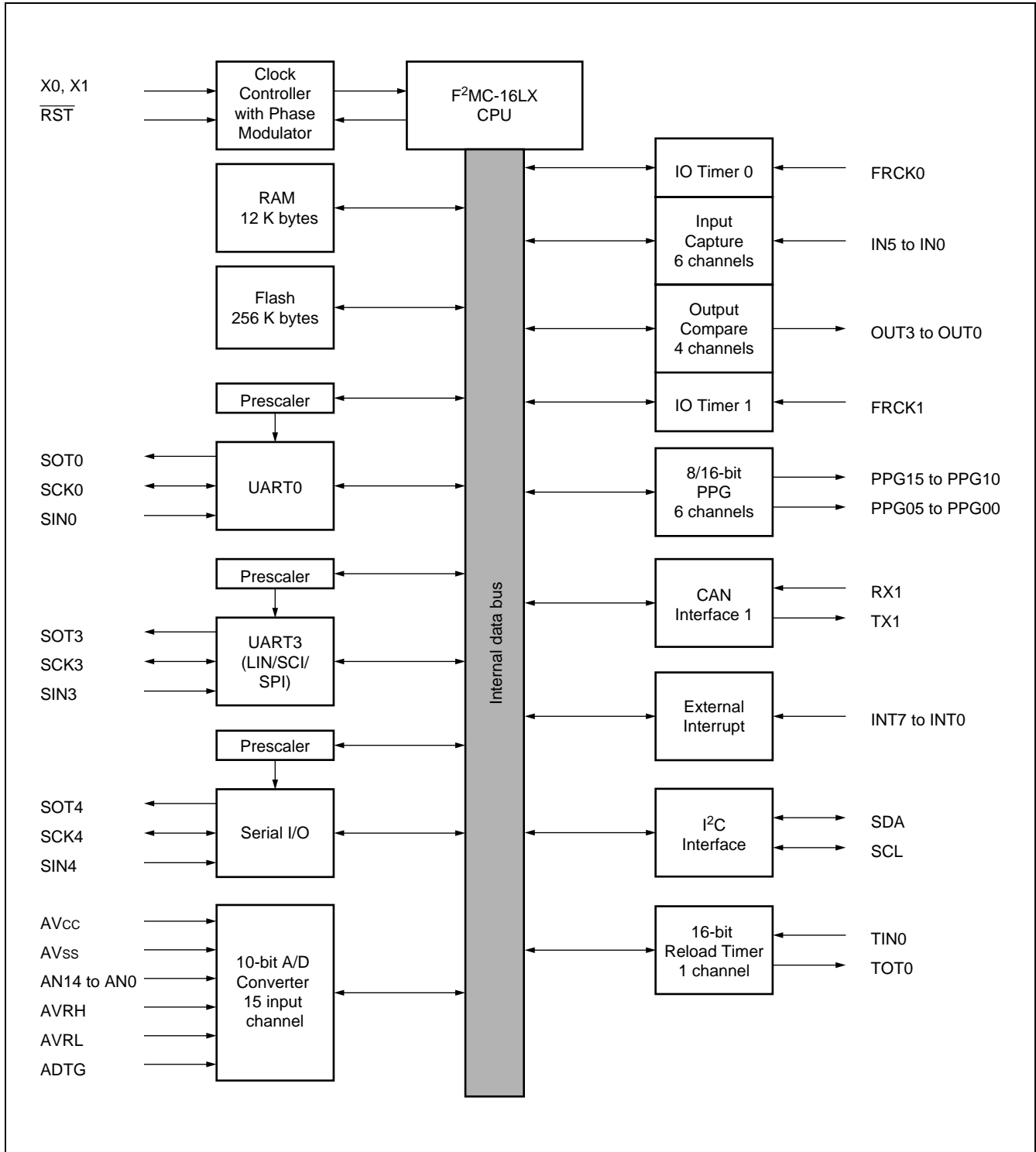
# MB90945 Series

- MB90F947, MB90F947A



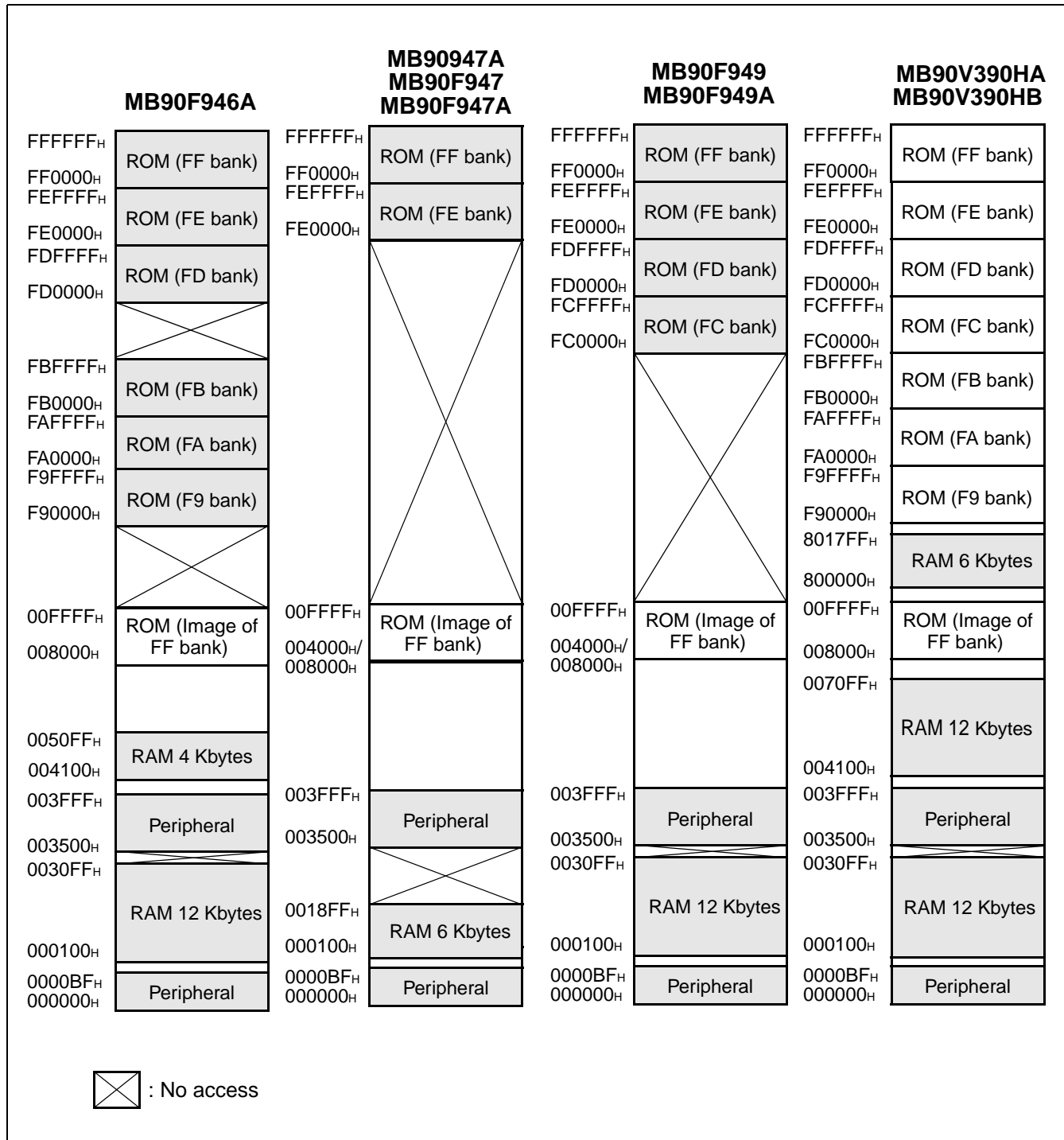
# MB90945 Series

- MB90F949, MB90F949A



# MB90945 Series

## MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.

For example, an attempt to access 00C000<sub>H</sub> accesses the value at FFC000<sub>H</sub> in ROM.

The ROM area in bank FF exceeds 32/48 K bytes, and its entire image cannot be shown in bank 00.

The image between FF4000<sub>H</sub>/FF8000<sub>H</sub> and FFFFF<sub>H</sub> is visible in bank 00, while the image between FF0000<sub>H</sub> and FF3FFF<sub>H</sub>/FF7FFF<sub>H</sub> is visible only in bank FF.

## ■ I/O MAP

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
00 <sub>H</sub>	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
01 <sub>H</sub>	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
02 <sub>H</sub>	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
03 <sub>H</sub>	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
04 <sub>H</sub>	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
05 <sub>H</sub>	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
06 <sub>H</sub>	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
07 <sub>H</sub>	Reserved				
08 <sub>H</sub>	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
09 <sub>H</sub>	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX
0A <sub>H</sub>	Port A data register	PDRA	R/W	Port A	XXXXXXXX
0B <sub>H</sub>	Port B data register	PDRB	R/W	Port B	XXXXXXXX
0C <sub>H</sub>	Analog Input Enable 0	ADER0	R/W	Port 6, A/D	11111111
0D <sub>H</sub>	Analog Input Enable 1/ ADC Select	ADER1	R/W	Port B, A/D	01111111
0E <sub>H</sub>	Input Level Select Register (MB90V390HA/MB90V390HB only)	ILSR	R/W	Ports	00000000
0F <sub>H</sub>	Input Level Select Register (MB90V390HA/MB90V390HB only)	ILSR	R/W	Ports	00000000
10 <sub>H</sub>	Port 0 direction register	DDR0	R/W	Port 0	00000000
11 <sub>H</sub>	Port 1 direction register	DDR1	R/W	Port 1	00000000
12 <sub>H</sub>	Port 2 direction register	DDR2	R/W	Port 2	00000000
13 <sub>H</sub>	Port 3 direction register	DDR3	R/W	Port 3	00000000
14 <sub>H</sub>	Port 4 direction register	DDR4	R/W	Port 4	00000000
15 <sub>H</sub>	Port 5 direction register	DDR5	R/W	Port 5	00000000
16 <sub>H</sub>	Port 6 direction register	DDR6	R/W	Port 6	00000000
17 <sub>H</sub>	Reserved				
18 <sub>H</sub>	Port 8 direction register	DDR8	R/W	Port 8	XXXXXXXX00
19 <sub>H</sub>	Port 9 direction register	DDR9	R/W	Port 9	00000000
1A <sub>H</sub>	Port A direction register	DDRA	R/W	Port A	00000000
1B <sub>H</sub>	Port B direction register	DDRB	R/W	Port B	00000000
1C <sub>H</sub> to 1F <sub>H</sub>	Reserved				

(Continued)

# MB90945 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
20H	Serial Mode Control 0	UMC0	R/W	UART0	00000100
21H	Status 0	USR0	R/W		00010000
22H	Input/Output Data 0	UIDR0/ UODR0	R/W		XXXXXXXX
23H	Rate and Data 0	URD0	R/W		0000000X
24H to 2BH	Reserved				
2CH	Serial Mode Control 4	SMCS4	R/W	Serial I/O Interface	XXXX0000
2DH	Serial Mode Control 4	SMCS4	R/W		00000010
2EH	Serial Data 4	SDR4	R/W		XXXXXXXX
2FH	Serial I/O Prescaler/Edge Selector 4	CDCR4	R/W		0X0X0000
30H	External Interrupt Enable	ENIR	R/W	External Interrupt	00000000
31H	External Interrupt Request	EIRR	R/W		XXXXXXXX
32H	External Interrupt Level	ELVR	R/W		00000000
33H	External Interrupt Level	ELVR	R/W		00000000
34H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00000000
35H	A/D Control Status 1	ADCS1	R/W		00000000
36H	A/D Data 0	ADCR0	R		XXXXXXXX
37H	A/D Data 1	ADCR1	R/W		000000XX
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0X000XX1
39H	PPG1 operation mode control register	PPGC1	R/W		0X000001
3AH	PPG0 and PPG1 clock select register	PPG01	R/W		000000XX
3BH	Reserved				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0X000XX1
3DH	PPG3 operation mode control register	PPGC3	R/W		0X000001
3EH	PPG2 and PPG3 clock select register	PPG23	R/W		000000XX
3FH	Reserved				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0X000XX1
41H	PPG5 operation mode control register	PPGC5	R/W		0X000001
42H	PPG4 and PPG5 clock select register	PPG45	R/W		000000XX
43H	Reserved				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1
45H	PPG7 operation mode control register	PPGC7	R/W		0X000001
46H	PPG6 and PPG7 clock select register	PPG67	R/W		000000XX
47H	Reserved				

(Continued)

# MB90945 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
48H	PPG8 operation mode control register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1
49H	PPG9 operation mode control register	PPGC9	R/W		0X000001
4AH	PPG8 and PPG9 clock select register	PPG89	R/W		000000XX
4BH	Reserved				
4CH	PPGA operation mode control register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0X000XX1
4DH	PPGB operation mode control register	PPGCB	R/W		0X000001
4EH	PPGA and PPGB clock select register	PPGAB	R/W		000000XX
4FH	Reserved				
50H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000
51H	Timer Control Status 0	TMCSR0	R/W		XXXX0000
52H to 53H	Reserved				
54H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000
55H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000
56H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000
57H	Reserved				
58H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00
59H	Output Compare Control Status 1	OCS1	R/W		0XX00000
5AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00
5BH	Output Compare Control Status 3	OCS3	R/W		0XX00000
5CH to 6EH	Reserved				
6FH	ROM Mirror	ROMM	W	ROM Mirror	XXXXXXXX1
70H to 7FH	Reserved				
80H to 8FH	Reserved for CAN Interface 1. Refer to "■ CAN CONTROLLER"				
90H to 9DH	Reserved				
9EH	ROM Correction Control Status 0	PACSR0	R/W	ROM Correction 0	00000000
9FH	Delayed Interrupt/release	DIRR	R/W	Delayed Interrupt	XXXXXXXX0
A0H	Low-power Mode	LPMCR	R/W	Low Power Controller	00011000
A1H	Clock Selector	CKSCR	R/W	Low Power Controller	11111100
A2H to A7H	Reserved				
A8H	Watchdog Control	WDTC	R/W	Watchdog Timer	XXXXX111
A9H	Timebase timer Control	TBTC	R/W	Timebase timer	1XX00100
AAH to ADH	Reserved				

(Continued)

# MB90945 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
AE <sub>H</sub>	Flash Control Status (Flash devices only. Otherwise reserved)	FMCS	R/W	Flash memory	000X0000
AF <sub>H</sub>	Reserved				
B0 <sub>H</sub>	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111
B1 <sub>H</sub>	Interrupt control register 01	ICR01	R/W		00000111
B2 <sub>H</sub>	Interrupt control register 02	ICR02	R/W		00000111
B3 <sub>H</sub>	Interrupt control register 03	ICR03	R/W		00000111
B4 <sub>H</sub>	Interrupt control register 04	ICR04	R/W		00000111
B5 <sub>H</sub>	Interrupt control register 05	ICR05	R/W		00000111
B6 <sub>H</sub>	Interrupt control register 06	ICR06	R/W		00000111
B7 <sub>H</sub>	Interrupt control register 07	ICR07	R/W		00000111
B8 <sub>H</sub>	Interrupt control register 08	ICR08	R/W		00000111
B9 <sub>H</sub>	Interrupt control register 09	ICR09	R/W		00000111
BA <sub>H</sub>	Interrupt control register 10	ICR10	R/W		00000111
BB <sub>H</sub>	Interrupt control register 11	ICR11	R/W		00000111
BC <sub>H</sub>	Interrupt control register 12	ICR12	R/W		00000111
BD <sub>H</sub>	Interrupt control register 13	ICR13	R/W		00000111
BE <sub>H</sub>	Interrupt control register 14	ICR14	R/W		00000111
BF <sub>H</sub>	Interrupt control register 15	ICR15	R/W	00000111	
C0 <sub>H</sub> to FF <sub>H</sub>	Reserved				

(Continued)



# MB90945 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
3500 <sub>H</sub>	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX
3501 <sub>H</sub>	Reload H	PRLH0	R/W		XXXXXXXX
3502 <sub>H</sub>	Reload L	PRLLO1	R/W		XXXXXXXX
3503 <sub>H</sub>	Reload H	PRLH1	R/W		XXXXXXXX
3504 <sub>H</sub>	Reload L	PRLLO2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX
3505 <sub>H</sub>	Reload H	PRLH2	R/W		XXXXXXXX
3506 <sub>H</sub>	Reload L	PRLLO3	R/W		XXXXXXXX
3507 <sub>H</sub>	Reload H	PRLH3	R/W		XXXXXXXX
3508 <sub>H</sub>	Reload L	PRLLO4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX
3509 <sub>H</sub>	Reload H	PRLH4	R/W		XXXXXXXX
350A <sub>H</sub>	Reload L	PRLLO5	R/W		XXXXXXXX
350B <sub>H</sub>	Reload H	PRLH5	R/W		XXXXXXXX
350C <sub>H</sub>	Reload L	PRLLO6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX
350D <sub>H</sub>	Reload H	PRLH6	R/W		XXXXXXXX
350E <sub>H</sub>	Reload L	PRLLO7	R/W		XXXXXXXX
350F <sub>H</sub>	Reload H	PRLH7	R/W		XXXXXXXX
3510 <sub>H</sub>	Reload L	PRLLO8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX
3511 <sub>H</sub>	Reload H	PRLH8	R/W		XXXXXXXX
3512 <sub>H</sub>	Reload L	PRLLO9	R/W		XXXXXXXX
3513 <sub>H</sub>	Reload H	PRLH9	R/W		XXXXXXXX
3514 <sub>H</sub>	Reload L	PRLLOA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX
3515 <sub>H</sub>	Reload H	PRLHA	R/W		XXXXXXXX
3516 <sub>H</sub>	Reload L	PRLLOB	R/W		XXXXXXXX
3517 <sub>H</sub>	Reload H	PRLHB	R/W		XXXXXXXX
3518 <sub>H</sub>	Serial Mode Register	SMR3	R/W	UART3	00000000
3519 <sub>H</sub>	Serial Control Register	SCR3	R/W		00000000
351A <sub>H</sub>	Reception/Transmission Data Register	RDR3/ TDR3	R/W		00000000
351B <sub>H</sub>	Serial Status Register	SSR3	R/W		00001000
351C <sub>H</sub>	Extended Communication Control Reg.	ECCR3	R/W		000000XX
351D <sub>H</sub>	Extended Status/Control Register	ESCR3	R/W		00000100
351E <sub>H</sub>	Baud Rate Register 0	BGR03	R/W		00000000
351F <sub>H</sub>	Baud Rate Register 1	BGR13	R/W		00000000

(Continued)

# MB90945 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
3520 <sub>H</sub>	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX
3521 <sub>H</sub>	Input Capture 0	IPCP0	R		XXXXXXXX
3522 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX
3523 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX
3524 <sub>H</sub>	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX
3525 <sub>H</sub>	Input Capture 2	IPCP2	R		XXXXXXXX
3526 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX
3527 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX
3528 <sub>H</sub>	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX
3529 <sub>H</sub>	Input Capture 4	IPCP4	R		XXXXXXXX
352A <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX
352B <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX
352C <sub>H</sub>	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000
352D <sub>H</sub>	Timer Data 0	TCDT0	R/W		00000000
352E <sub>H</sub>	Timer Control 0	TCCS0	R/W		00000000
352F <sub>H</sub>	Timer Control 0	TCCS0	R/W		0XXXXXXXX
3530 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX
3531 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXX
3532 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX
3533 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX
3534 <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX
3535 <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXX
3536 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX
3537 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX
3538 <sub>H</sub> to 353B <sub>H</sub>	Reserved				
353C <sub>H</sub>	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000
353D <sub>H</sub>	Timer Data 1	TCDT1	R/W		00000000
353E <sub>H</sub>	Timer Control 1	TCCS1	R/W		00000000
353F <sub>H</sub>	Timer Control 1	TCCS1	R/W		0XXXXXXXX
3540 <sub>H</sub>	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX
3541 <sub>H</sub>	Timer 0/Reload 0	TMR0/ TMRLR0	R/W		XXXXXXXX
3542 <sub>H</sub> to 356D <sub>H</sub>	Reserved				

(Continued)

# MB90945 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
356E <sub>H</sub>	CAN Direct Mode Register	CDMR	R/W	CAN clock sync	XXXXXXXX0
356F <sub>H</sub> to 359F <sub>H</sub>	Reserved				
35A0 <sub>H</sub>	I <sup>2</sup> C bus status register	IBSR	R	I <sup>2</sup> C Interface	00000000
35A1 <sub>H</sub>	I <sup>2</sup> C bus control register	IBCR	R/W		00000000
35A2 <sub>H</sub>	I <sup>2</sup> C ten bit slave address register	ITBAL	R/W		00000000
35A3 <sub>H</sub>		ITBAH	R/W		00000000
35A4 <sub>H</sub>	I <sup>2</sup> C ten bit address mask register	ITMKL	R/W		11111111
35A5 <sub>H</sub>		ITMKH	R/W		00111111
35A6 <sub>H</sub>	I <sup>2</sup> C seven bit slave address register	ISBA	R/W		00000000
35A7 <sub>H</sub>	I <sup>2</sup> C seven bit address mask register	ISMK	R/W		01111111
35A8 <sub>H</sub>	I <sup>2</sup> C data register	IDAR	R/W		00000000
35A9 <sub>H</sub> to 35AA <sub>H</sub>	Reserved				
35AB <sub>H</sub>	I <sup>2</sup> C clock control register	ICCR	R/W	I <sup>2</sup> C Interface	00011111
35AC <sub>H</sub> to 35C8 <sub>H</sub>	Reserved				
35C9 <sub>H</sub>	Input Capture Edge 0/1	ICE01	R/W	Input Capture 0/1	XXXXX0XX
35CA <sub>H</sub>	Input Capture Edge 2/3	ICE23	R	Input Capture 2/3	XXXXXXXX
35CB <sub>H</sub>	Input Capture Edge 4/5	ICE45	R/W	Input Capture 4/5	XXXXX0XX
35CC <sub>H</sub> to 35CE <sub>H</sub>	Reserved				
35CF <sub>H</sub>	PLL and Special Configuration Control Register	PSCCR	W	PLL	XXXX0000
35D0 <sub>H</sub> to 35D7 <sub>H</sub>	Reserved				
35D8 <sub>H</sub>	Serial Mode Register	SMR2	R/W	UART2 (MB90V390HA, MB90V390HB and MB90F946A only)	00000000
35D9 <sub>H</sub>	Serial Control Register	SCR2	R/W		00000000
35DA <sub>H</sub>	Reception/Transmission Data Register	RDR2/ TDR2	R/W		00000000
35DB <sub>H</sub>	Serial Status Register	SSR2	R/W		00001000
35DC <sub>H</sub>	Extended Communication Control Reg.	ECCR2	R/W		000000XX
35DD <sub>H</sub>	Extended Status/Control Register	ESCR2	R/W		00000100
35DE <sub>H</sub>	Baud Rate Register 0	BGR02	R/W		00000000
35DF <sub>H</sub>	Baud Rate Register 1	BGR12	R/W	UART2 (MB90V390HA, MB90V390HB and MB90F946A only)	00000000

# MB90945 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
35E0 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W	Address Matching Detection Function 0	XXXXXXXX
35E1 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W		XXXXXXXX
35E2 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W		XXXXXXXX
35E3 <sub>H</sub>	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
35E4 <sub>H</sub>	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
35E5 <sub>H</sub>	ROM Correction Address 1	PADR1	R/W		XXXXXXXX

(Continued)

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Address	Register	Abbreviation	Access	Resource name	Initial value
35E6 <sub>H</sub>	ROM Correction Address 2	PADR2	R/W	Address Matching Detection Function 0	XXXXXXXX
35E7 <sub>H</sub>	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
35E8 <sub>H</sub>	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
35E9 <sub>H</sub> to 37FF <sub>H</sub>	Reserved				
3800 <sub>H</sub> to 38FF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLER”				
3900 <sub>H</sub> to 39FF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLER”				
3A00 <sub>H</sub> to 3FFF <sub>H</sub>	Reserved				

\_ : Unused bit

X : Unknown value

Note : Any write access to reserved addresses in I/O map should not be performed.  
A read access to reserved address results in reading “X”.

## ■ CAN CONTROLLER

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance mask register 0/acceptance mask register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

**List of Control Registers (1)**

Address	Register	Abbreviation	Access	Initial Value
<b>CAN1</b>				
000080H	Message buffer valid register	BVALR	R/W	00000000 00000000
000081H				
000082H	Transmit request register	TREQR	R/W	00000000 00000000
000083H				
000084H	Transmit cancel register	TCANR	W	00000000 00000000
000085H				
000086H	Transmit complete register	TCR	R/W	00000000 00000000
000087H				
000088H	Receive complete register	RCR	R/W	00000000 00000000
000089H				
00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000
00008BH				
00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000
00008DH				
00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000
00008FH				

# MB90945 Series

List of Control Registers (2)

Address	Register	Abbreviation	Access	Initial Value
<b>CAN1</b>				
003900H	Control status register	CSR	R/W, R	00XXX000 0XXXX0X1
003901H				
003902H	Last event indicator register	LEIR	R/W	XXXXXXXX 000X0000
003903H				
003904H	Receive/transmit error counter	RTEC	R	00000000 00000000
003905H				
003906H	Bit timing register	BTR	R/W	X1111111 11111111
003907H				
003908H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX
003909H				
00390AH	Transmit RTR register	TRTRR	R/W	00000000 00000000
00390BH				
00390CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX
00390DH				
00390EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000
00390FH				
003910H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX
003911H				
003912H				XXXXXXXX XXXXXXXX
003913H				
003914H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX
003915H				
003916H				XXXXXXXX XXXXXXXX
003917H				
003918H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX
003919H				
00391AH				XXXXXXXX XXXXXXXX
00391BH				

List of Message Buffers (ID Registers) (1)

Address	Register	Abbreviation	Access	Initial Value
<b>CAN1</b>				
003800 <sub>H</sub> to 00381F <sub>H</sub>	General- purpose RAM	—	R/W	XXXXXXXX to XXXXXXXX
003820 <sub>H</sub>	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX
003821 <sub>H</sub>				XXXXXXXX XXXXXXXX
003822 <sub>H</sub>				XXXXXXXX XXXXXXXX
003823 <sub>H</sub>				XXXXXXXX XXXXXXXX
003824 <sub>H</sub>	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX
003825 <sub>H</sub>				XXXXXXXX XXXXXXXX
003826 <sub>H</sub>				XXXXXXXX XXXXXXXX
003827 <sub>H</sub>				XXXXXXXX XXXXXXXX
003828 <sub>H</sub>	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX
003829 <sub>H</sub>				XXXXXXXX XXXXXXXX
00382A <sub>H</sub>				XXXXXXXX XXXXXXXX
00382B <sub>H</sub>				XXXXXXXX XXXXXXXX
00382C <sub>H</sub>	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX
00382D <sub>H</sub>				XXXXXXXX XXXXXXXX
00382E <sub>H</sub>				XXXXXXXX XXXXXXXX
00382F <sub>H</sub>				XXXXXXXX XXXXXXXX
003830 <sub>H</sub>	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX
003831 <sub>H</sub>				XXXXXXXX XXXXXXXX
003832 <sub>H</sub>				XXXXXXXX XXXXXXXX
003833 <sub>H</sub>				XXXXXXXX XXXXXXXX
003834 <sub>H</sub>	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX
003835 <sub>H</sub>				XXXXXXXX XXXXXXXX
003836 <sub>H</sub>				XXXXXXXX XXXXXXXX
003837 <sub>H</sub>				XXXXXXXX XXXXXXXX
003838 <sub>H</sub>	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX
003839 <sub>H</sub>				XXXXXXXX XXXXXXXX
00383A <sub>H</sub>				XXXXXXXX XXXXXXXX
00383B <sub>H</sub>				XXXXXXXX XXXXXXXX
00383C <sub>H</sub>	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX
00383D <sub>H</sub>				XXXXXXXX XXXXXXXX
00383E <sub>H</sub>				XXXXXXXX XXXXXXXX
00383F <sub>H</sub>				XXXXXXXX XXXXXXXX

# MB90945 Series

List of Message Buffers (ID Registers) (2)

Address	Register	Abbreviation	Access	Initial Value
<b>CAN1</b>				
003840 <sub>H</sub>	ID register 8	IDR8	R/W	XXXXXXXX
003841 <sub>H</sub>				XXXXXXXX
003842 <sub>H</sub>				XXXXXXXX
003843 <sub>H</sub>				XXXXXXXX
003844 <sub>H</sub>	ID register 9	IDR9	R/W	XXXXXXXX
003845 <sub>H</sub>				XXXXXXXX
003846 <sub>H</sub>				XXXXXXXX
003847 <sub>H</sub>				XXXXXXXX
003848 <sub>H</sub>	ID register 10	IDR10	R/W	XXXXXXXX
003849 <sub>H</sub>				XXXXXXXX
00384A <sub>H</sub>				XXXXXXXX
00384B <sub>H</sub>				XXXXXXXX
00384C <sub>H</sub>	ID register 11	IDR11	R/W	XXXXXXXX
00384D <sub>H</sub>				XXXXXXXX
00384E <sub>H</sub>				XXXXXXXX
00384F <sub>H</sub>				XXXXXXXX
003850 <sub>H</sub>	ID register 12	IDR12	R/W	XXXXXXXX
003851 <sub>H</sub>				XXXXXXXX
003852 <sub>H</sub>				XXXXXXXX
003853 <sub>H</sub>				XXXXXXXX
003854 <sub>H</sub>	ID register 13	IDR13	R/W	XXXXXXXX
003855 <sub>H</sub>				XXXXXXXX
003856 <sub>H</sub>				XXXXXXXX
003857 <sub>H</sub>				XXXXXXXX
003858 <sub>H</sub>	ID register 14	IDR14	R/W	XXXXXXXX
003859 <sub>H</sub>				XXXXXXXX
00385A <sub>H</sub>				XXXXXXXX
00385B <sub>H</sub>				XXXXXXXX
00385C <sub>H</sub>	ID register 15	IDR15	R/W	XXXXXXXX
00385D <sub>H</sub>				XXXXXXXX
00385E <sub>H</sub>				XXXXXXXX
00385F <sub>H</sub>				XXXXXXXX



List of Message Buffers (DLC Registers and Data Registers) (1)

Address	Register	Abbreviation	Access	Initial Value
003860 <sub>H</sub>	DLC register 0	DLCR0	R/W	XXXXXXXX
003861 <sub>H</sub>				
003862 <sub>H</sub>	DLC register 1	DLCR1	R/W	XXXXXXXX
003863 <sub>H</sub>				
003864 <sub>H</sub>	DLC register 2	DLCR2	R/W	XXXXXXXX
003865 <sub>H</sub>				
003866 <sub>H</sub>	DLC register 3	DLCR3	R/W	XXXXXXXX
003867 <sub>H</sub>				
003868 <sub>H</sub>	DLC register 4	DLCR4	R/W	XXXXXXXX
003869 <sub>H</sub>				
00386A <sub>H</sub>	DLC register 5	DLCR5	R/W	XXXXXXXX
00386B <sub>H</sub>				
00386C <sub>H</sub>	DLC register 6	DLCR6	R/W	XXXXXXXX
00386D <sub>H</sub>				
00386E <sub>H</sub>	DLC register 7	DLCR7	R/W	XXXXXXXX
00386F <sub>H</sub>				
003870 <sub>H</sub>	DLC register 8	DLCR8	R/W	XXXXXXXX
003871 <sub>H</sub>				
003872 <sub>H</sub>	DLC register 9	DLCR9	R/W	XXXXXXXX
003873 <sub>H</sub>				
003874 <sub>H</sub>	DLC register 10	DLCR10	R/W	XXXXXXXX
003875 <sub>H</sub>				
003876 <sub>H</sub>	DLC register 11	DLCR11	R/W	XXXXXXXX
003877 <sub>H</sub>				
003878 <sub>H</sub>	DLC register 12	DLCR12	R/W	XXXXXXXX
003879 <sub>H</sub>				
00387A <sub>H</sub>	DLC register 13	DLCR13	R/W	XXXXXXXX
00387B <sub>H</sub>				
00387C <sub>H</sub>	DLC register 14	DLCR14	R/W	XXXXXXXX
00387D <sub>H</sub>				
00387E <sub>H</sub>	DLC register 15	DLCR15	R/W	XXXXXXXX
00387F <sub>H</sub>				

# MB90945 Series

List of Message Buffers (DLC Registers and Data Registers) (2)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003880 <sub>H</sub> to 003887 <sub>H</sub>	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX to XXXXXXXX
003888 <sub>H</sub> to 00388F <sub>H</sub>	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX to XXXXXXXX
003890 <sub>H</sub> to 003897 <sub>H</sub>	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX to XXXXXXXX
003898 <sub>H</sub> to 00389F <sub>H</sub>	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX to XXXXXXXX
0038A0 <sub>H</sub> to 0038A7 <sub>H</sub>	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX to XXXXXXXX
0038A8 <sub>H</sub> to 0038AF <sub>H</sub>	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX to XXXXXXXX
0038B0 <sub>H</sub> to 0038B7 <sub>H</sub>	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX to XXXXXXXX
0038B8 <sub>H</sub> to 0038BF <sub>H</sub>	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX to XXXXXXXX
0038C0 <sub>H</sub> to 0038C7 <sub>H</sub>	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX to XXXXXXXX
0038C8 <sub>H</sub> to 0038CF <sub>H</sub>	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX to XXXXXXXX
0038D0 <sub>H</sub> to 0038D7 <sub>H</sub>	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
0038D8 <sub>H</sub> to 0038DF <sub>H</sub>	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX to XXXXXXXX
0038E0 <sub>H</sub> to 0038E7 <sub>H</sub>	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX to XXXXXXXX
0038E8 <sub>H</sub> to 0038EF <sub>H</sub>	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX to XXXXXXXX

# MB90945 Series

List of Message Buffers (DLC Registers and Data Registers) (3)

Address	Register	Abbreviation	Access	Initial Value
<b>CAN1</b>				
0038F0 <sub>H</sub> to 0038F7 <sub>H</sub>	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX to XXXXXXXX
0038F8 <sub>H</sub> to 0038FF <sub>H</sub>	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX to XXXXXXXX

# MB90945 Series

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI <sup>2</sup> OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC <sub>H</sub>	—	—
INT9 instruction	N/A	#09	FFFFD8 <sub>H</sub>	—	—
Exception	N/A	#10	FFFFD4 <sub>H</sub>	—	—
Timebase timer	N/A	#11	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
External Interrupt INT0 to INT7	○	#12	FFFFCC <sub>H</sub>		
Reserved	×	#13	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
Reserved	×	#14	FFFFC4 <sub>H</sub>		
CAN 1 RX	N/A	#15	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
CAN 1 TX/NS	N/A	#16	FFFFBC <sub>H</sub>		
PPG 0/1	N/A	#17	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
PPG 2/3	N/A	#18	FFFFB4 <sub>H</sub>		
PPG 4/5	N/A	#19	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
PPG 6/7	N/A	#20	FFFFAC <sub>H</sub>		
PPG 8/9	N/A	#21	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
PPG A/B	N/A	#22	FFFFA4 <sub>H</sub>		
16-bit Reload Timer 0	○	#23	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
Reserved	×	#24	FFFF9C <sub>H</sub>		
Input Capture 0/1	○	#25	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
Output compare 0/1	○	#26	FFFF94 <sub>H</sub>		
Input Capture 2/3	○	#27	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
Output Compare 2/3	○	#28	FFFF8C <sub>H</sub>		
Input Capture 4/5	○	#29	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
I <sup>2</sup> C	○	#30	FFFF84 <sub>H</sub>		
A/D Converter	○	#31	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
I/O Timer 0 / I/O Timer 1	N/A	#32	FFFF7C <sub>H</sub>		
Serial I/O	○	#33	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
Reserved	×	#34	FFFF74 <sub>H</sub>		
UART 0 RX	◎	#35	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
UART 0 TX	○	#36	FFFF6C <sub>H</sub>		
Reserved	×	#37	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
Reserved	×	#38	FFFF64 <sub>H</sub>		

(Continued)

(Continued)

Interrupt cause	EI <sup>2</sup> OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
UART 2 RX / UART 3 RX	⊙	#39	FFFF60 <sub>H</sub>	ICR14	0000BE <sub>H</sub>
UART 2 TX / UART 3 TX	○	#40	FFFF5C <sub>H</sub>		
Flash memory	N/A	#41	FFFF58 <sub>H</sub>	ICR15	0000BF <sub>H</sub>
Delayed interrupt	N/A	#42	FFFF54 <sub>H</sub>		

- : The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal.
- ⊙ : The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal. A stop request is available.
- × : Unavailable
- N/A : The interrupt request flag is not cleared by the EI<sup>2</sup>OS interrupt clear signal.

- Notes :
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI<sup>2</sup>OS interrupt clear signal.
  - At the end of EI<sup>2</sup>OS, the EI<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI<sup>2</sup>OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the EI<sup>2</sup>OS for this interrupt number.
  - If EI<sup>2</sup>OS is enabled, EI<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI<sup>2</sup>OS, the other interrupt should be disabled.

# MB90945 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH, AV_{CC} \geq AVRL, AVRH \geq AVRL$
Input voltage*1	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	$I_{CLAMP}$	-4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\sum  I_{CLAMP} $	—	40	mA	*5
"L" level maximum output current	$I_{OL1}$	—	15	mA	*4
"L" level average output current	$I_{OLAV1}$	—	4	mA	*4
"L" level maximum overall output current	$\Sigma I_{OL1}$	—	100	mA	*4
"L" level average overall output current	$\Sigma I_{OLAV1}$	—	50	mA	*4
"H" level maximum output current	$I_{OH1}$	—	-15	mA	*4
"H" level average output current	$I_{OHAV1}$	—	-4	mA	*4
"H" level maximum overall output current	$\Sigma I_{OH1}$	—	-100	mA	*4
"H" level average overall output current	$\Sigma I_{OHAV}$	—	-50	mA	*4
Power consumption	$P_D$	—	500	mW	MB90947A/F947/F947A/F949/ F949A
		—	525		MB90F946A
Operating temperature	$T_A$	-40	+105	°C	
Storage temperature	$T_{STG}$	-55	+150	°C	

\*1 : This parameter is based on  $V_{SS} = AV_{SS} = 0$  V.

\*2 : Set  $AV_{CC}$  and  $V_{CC}$  to the same voltage. Make sure that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  when the power is switched on.

\*3 :  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3$  V.  $V_I$  should not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the  $I_{CLAMP}$  rating supercedes the  $V_I$  rating.

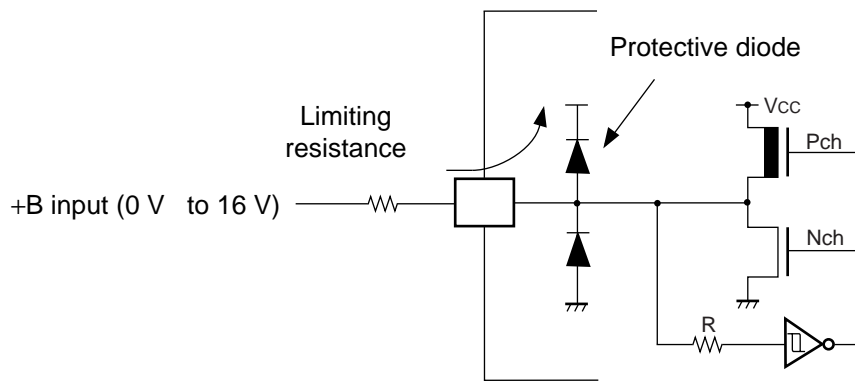
\*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80, P81, P90 to P97, PA0 to PA7, PB0 to PB7

\*5 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80, P81, P90 to P97, PA0 to PA7, PB0 to PB7

- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

- Input/output equivalent circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB90945 Series

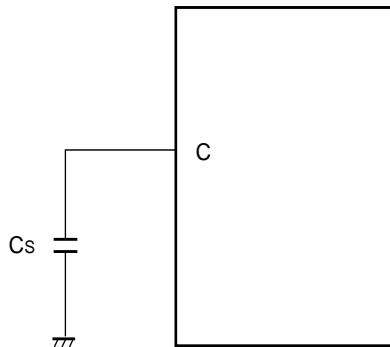
## 2. Recommended Conditions

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}$ , $AV_{CC}$	3.5	5.0	5.5	V	Other than when writing to Flash memory and when using the A/D converter
		4.0	5.0	5.5	V	When writing to Flash memory
		4.5	5.0	5.5	V	When using the A/D converter
		2.0	—	5.5	V	Retain RAM data in stop mode
Smoothing capacitor	$C_s$	0.1	—	1.0	$\mu\text{F}$	*
Operating temperature	$T_A$	-40	—	+105	$^{\circ}\text{C}$	

\* : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the  $V_{CC}$  pin, use a bypass capacitor that has a larger capacity than that of  $C_s$ . Refer to the following figure for connection of smoothing capacitor  $C_s$ .

### • C Pin Connection Diagram



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.



# MB90945 Series

## 3. DC Characteristics

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	$V_{IHA}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs except ports P21/RX1, P42/SDA, P43/SCL
	$V_{IHS}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs P21/RX1, P42/SDA, P43/SCL
	$V_{IHR}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input "L" voltage	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs except ports P21/RX1, P42/SDA, P43/SCL
	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	Port inputs P21/RX1, P42/SDA, P43/SCL
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output "H" voltage	$V_{OH}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output "H" voltage	$V_{OHI}$	I <sup>2</sup> C outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH1} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output "L" voltage	$V_{OL}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
Output "L" voltage	$V_{OLI}$	I <sup>2</sup> C outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL1} = 3.0\text{ mA}$	—	—	0.4	V	
Input leak current	$I_{IL}$	—	$V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_I < V_{CC}$	-1	—	1	$\mu\text{A}$	

(Continued)

# MB90945 Series

(Continued)

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks		
				Min	Typ	Max				
Pull-down resistance	R <sub>DOWN</sub>	MD2	—	25	50	100	kOhm	only ROM devices		
Power supply current*	I <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	60	75	mA	MB90947A MB90F947/A MB90F949/A		
				—	65	85	mA	MB90F946A		
			V <sub>CC</sub> = 5.0 V, Internal frequency : 20 MHz, At normal operation.	—	50	65	mA	MB90947A MB90F947/A MB90F949/A		
				—	55	75	mA	MB90F946A		
			V <sub>CC</sub> = 5.0 V, Internal frequency : 20 MHz, At writing FLASH memory.	—	65	80	mA	MB90F947/A MB90F949/A		
				—	70	90	mA	MB90F946A		
			V <sub>CC</sub> = 5.0 V, Internal frequency : 20 MHz, At erasing FLASH memory.	—	70	85	mA	MB90F947/A MB90F949/A		
				—	75	95	mA	MB90F946A		
			I <sub>CCS</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	MB90947A MB90F947/A MB90F949/A
						—	28	40	mA	MB90F946A
			I <sub>CTS</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency : 2 MHz, At Main Timebase timer mode	—	0.3	0.6	mA	MB90947A MB90F946A MB90F947/A MB90F949/A
			I <sub>CTSPLL6</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At PLL Timebase timer mode, external frequency = 4 MHz	—	5	7	mA	MB90947A MB90F946A MB90F947/A MB90F949/A
	I <sub>CCH</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, At Stop mode, T <sub>A</sub> = +25°C	—	5	100	μA	MB90947A MB90F946A MB90F947/A MB90F949/A		
	Input capacity	C <sub>IN</sub>	Other than C, AV <sub>CC</sub> , AV <sub>SS</sub> , AVRH, AVRL, V <sub>CC</sub> , V <sub>SS</sub>	—	5	15	pF			

\* : The power supply current is measured with an external clock.

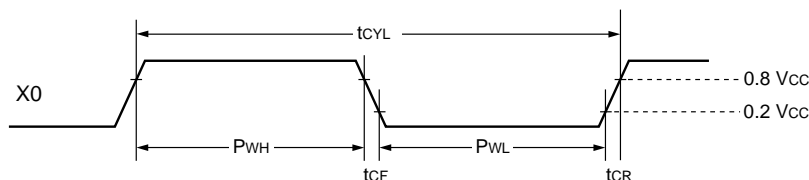
## 4. AC Characteristics

### (1) Clock Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

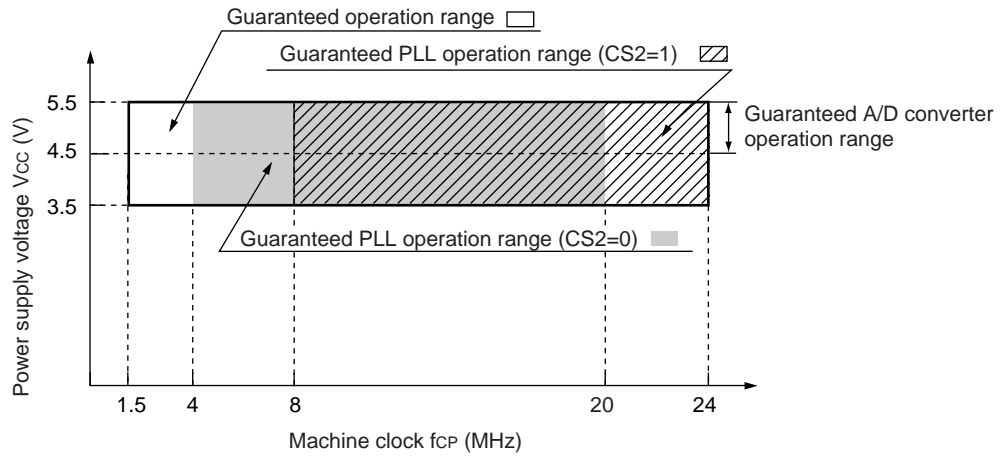
Parameter	Symbol	Pin	Value				Unit	Remarks
			Min	Typ	Max			
					CS2 = 0	CS2 = 1		
Clock frequency	$f_c$	X0, X1	3	—	8	8	MHz	$\times 1/2$ (When PLL stops) When using an oscillation circuit
			4	—	8	—	MHz	PLL $\times 1$ When using an oscillation circuit
			4	—	8	8	MHz	PLL $\times 2$ When using an oscillation circuit
			4	—	6.67	—	MHz	PLL $\times 3$ When using an oscillation circuit
			4	—	5	6	MHz	PLL $\times 4$ When using an oscillation circuit
			4	—	—	4	MHz	PLL $\times 6$ When using an oscillation circuit
		X0	3	—	12	12	MHz	$\times 1/2$ (When PLL stops) When using an external circuit
			4	—	12	—	MHz	PLL $\times 1$ When using an external circuit
			4	—	10	12	MHz	PLL $\times 2$ When using an external circuit
			4	—	6.67	—	MHz	PLL $\times 3$ When using an external circuit
			4	—	5	6	MHz	PLL $\times 4$ When using an external circuit
			4	—	—	4	MHz	PLL $\times 6$ When using an external circuit
Clock cycle time	$t_{CYL}$	X0, X1	125	—	333		ns	When using an oscillation circuit
		X0, X1	83.33	—	333		ns	When using an external clock
Input clock pulse width	$P_{WH}, P_{WL}$	X0	20	—	—		ns	Duty ratio is about 30% to 70%.
Input clock rise and fall time	$t_{CR}, t_{CF}$	X0	—	—	5		ns	When using external clock
Machine clock frequency	$f_{CP}$	—	1.5	—	24		MHz	Except programming or erasing Flash memory.
		—	1.5	—	20		MHz	When programming or erasing Flash memory. Be sure that the maximum momentary frequency $F_{max}$ does not exceed 20MHz.
Machine clock cycle time	$t_{CP}$	—	41.67	—	666		ns	Except programming or erasing Flash memory.
		—	50	—	666		ns	When programming or erasing Flash memory.

#### • Clock Timing



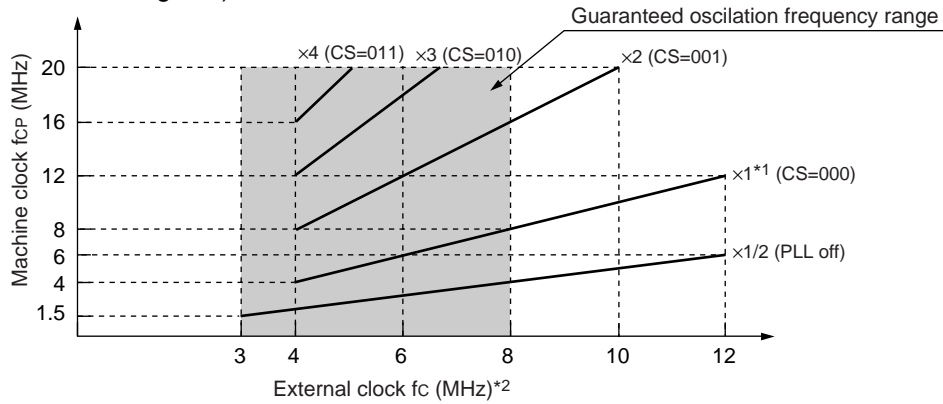
# MB90945 Series

- Guaranteed PLL operation range

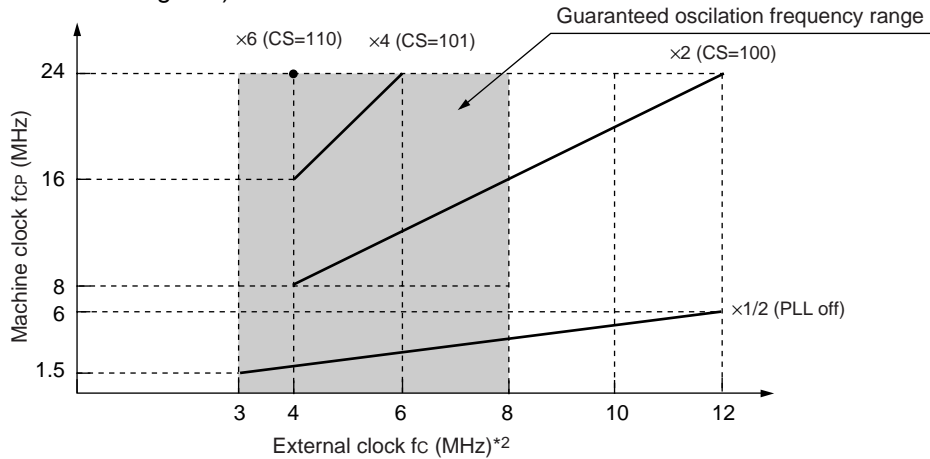


### Guaranteed operation range of MB90F947/MB90F949

- CS2 (bit 0 in PSCCR register) = 0



- CS2 (bit 0 in PSCCR register) = 1



\*1 : PLL  $\times 1$  guaranteed operation range is from 4.0 MHz to 12 MHz.

\*2 : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 8 MHz

### External clock frequency and Machine clock frequency

## (2) Reset Standby Input

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{V}$ )

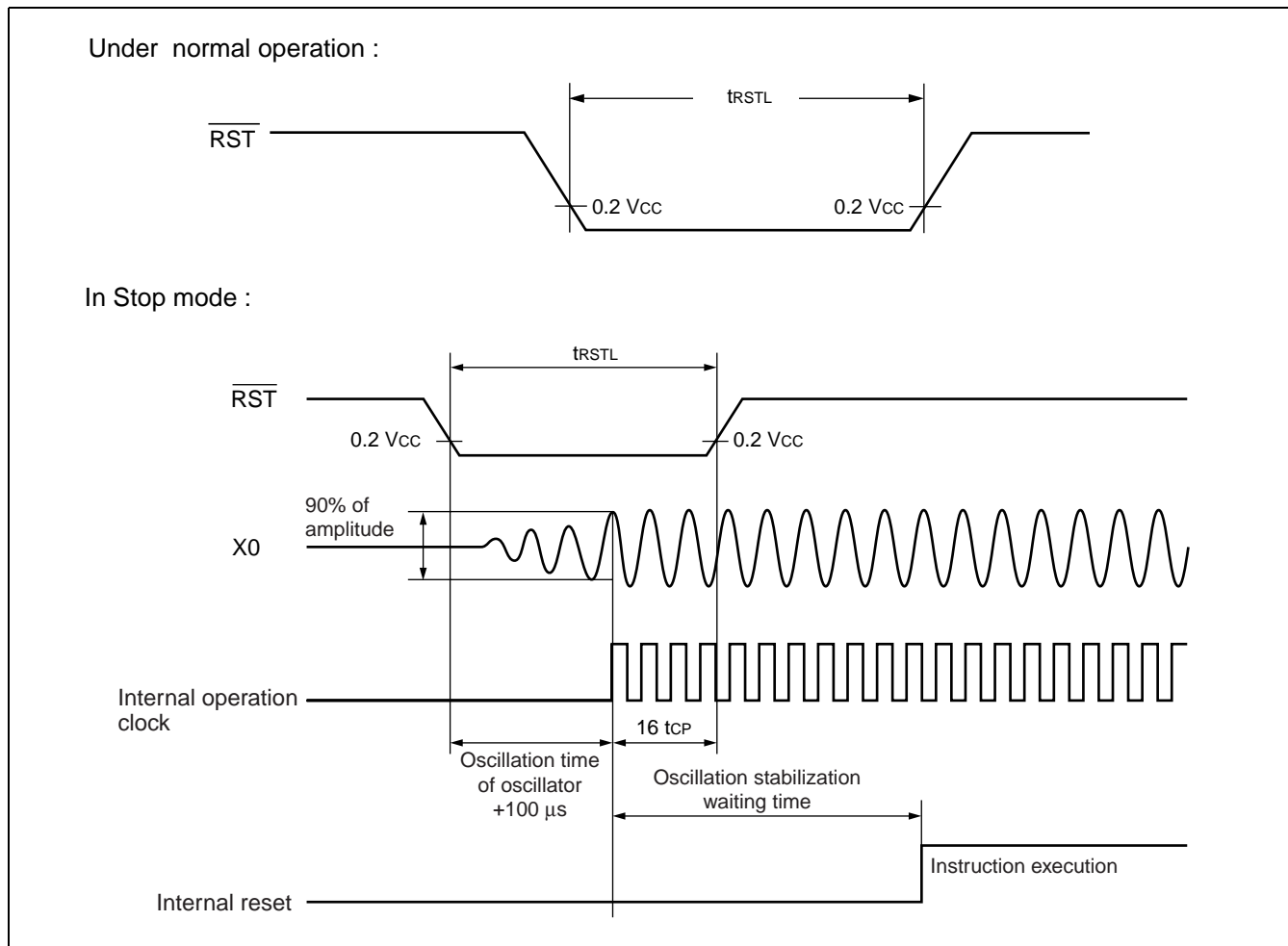
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	$t_{RSTL}$	$\overline{RST}$	$16\ t_{CP}^{*1}$	—	ns	Under normal operation
			Oscillation time of oscillator <sup>*2</sup> $+ 100 + 16\ t_{CP}^{*1}$	—	$\mu\text{s}$	In Stop mode
			100	—	$\mu\text{s}$	In Timebase timer mode

\*1 : " $t_{CP}$ " represents one cycle time of the machine clock.

No reset can fully initialize the Flash memory if it is performing the automatic algorithm.

\*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.

In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. With an external clock, the oscillation time is 0 ms.

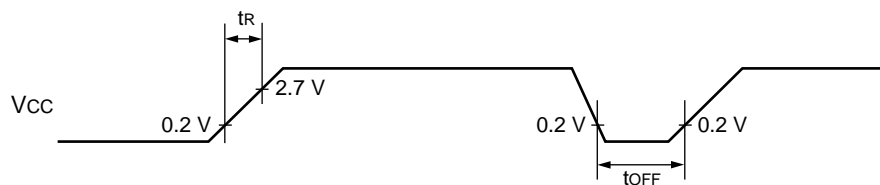


# MB90945 Series

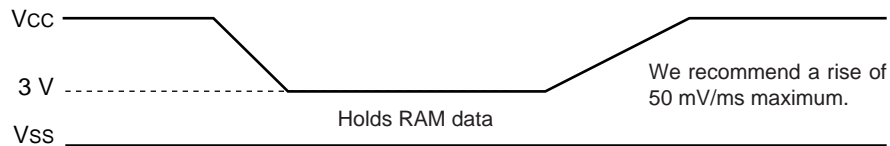
## (3) Power On Reset

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power off time	$t_{OFF}$	$V_{CC}$	—	1	—	ms	Due to repetitive operation



If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



# MB90945 Series

## (4) UART0, SIO Timing

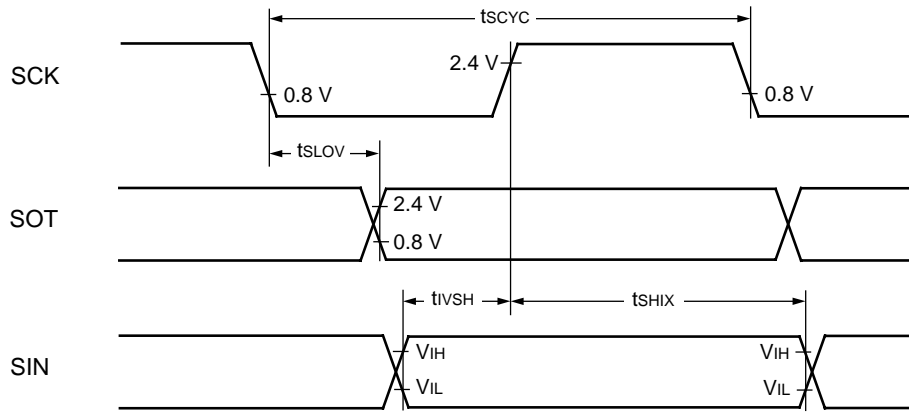
( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK0, SCK4	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$8\ t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0, SCK4, SOT0, SOT4		-80	+80	ns	
Valid SIN → SCK ↑	$t_{IVSH}$	SCK0, SCK4, SIN0, SIN4		100	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIX}$	SCK0, SCK4, SIN0, SIN4		60	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK0, SCK4	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4\ t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	SCK0, SCK4		$4\ t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0, SCK4, SOT0, SOT4		—	150	ns	
Valid SIN → SCK ↑	$t_{IVSH}$	SCK0, SCK4, SIN0, SIN4		60	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIX}$	SCK0, SCK4, SIN0, SIN4		60	—	ns	

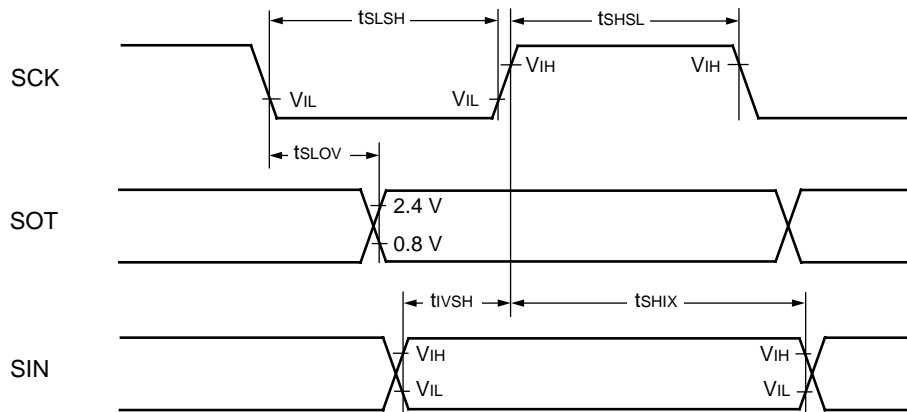
- Notes :
- AC characteristics in CLK synchronized mode.
  - $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for  $t_{CP}$ .

# MB90945 Series

## • Internal Shift Clock Mode



## • External Shift Clock Mode





## (5) UART2/3 Timing

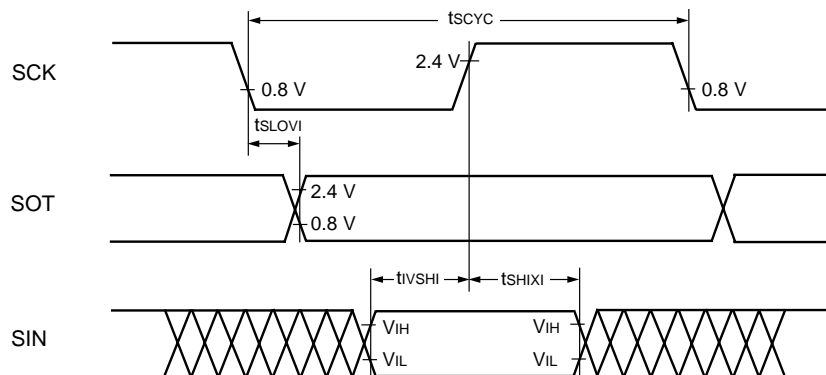
- Bit setting : ESCR : SCES = 0, ECCR : SCDE = 0

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK2,SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK2,SCK3 SOT2,SOT3		-50	+50	ns	
Valid SIN → SCK ↑	$t_{IVSHI}$	SCK2,SCK3 SIN2,SIN3		$t_{CP} + 80$	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIXI}$	SCK2,SCK3 SIN2,SIN3		0	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK2,SCK3	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$t_{CP} + 10$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	SCK2,SCK3		$3 t_{CP} - t_R$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCK2,SCK3 SOT2,SOT3		—	$2 t_{CP} + 60$	ns	
Valid SIN → SCK ↑	$t_{IVSHE}$	SCK2,SCK3 SIN2,SIN3		30	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIXE}$	SCK2,SCK3 SIN2,SIN3		$t_{CP} + 30$	—	ns	
SCK fall time	$t_F$	SCK2,SCK3		—	10	ns	
SCK rise time	$t_R$	SCK2,SCK3		—	10	ns	

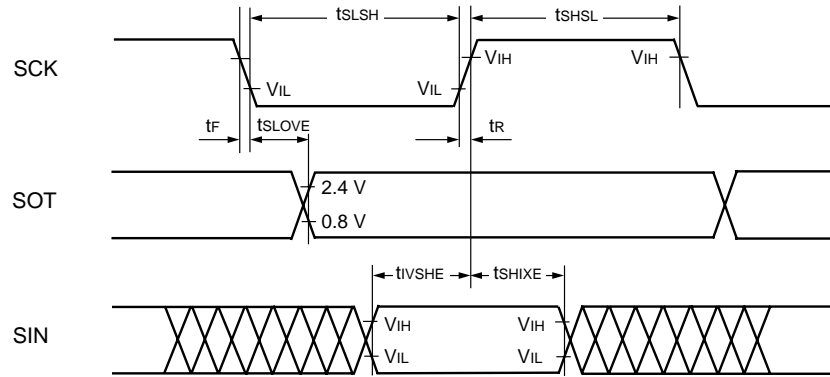
Note :  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to " (1) Clock timing" rating for  $t_{CP}$

### • Internal Shift Clock Mode



# MB90945 Series

• External Shift Clock Mode



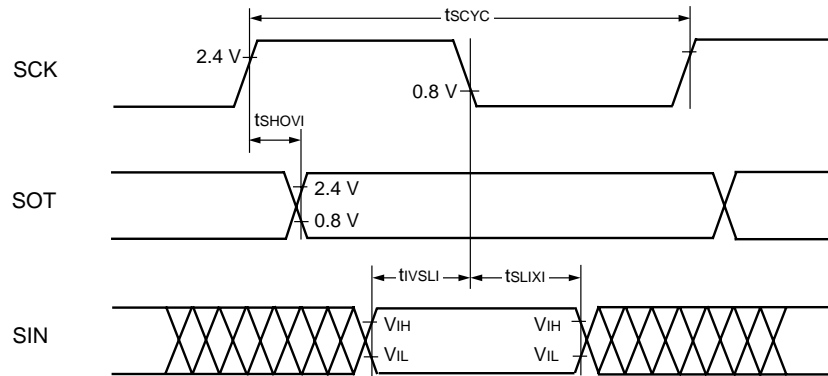
• Bit setting : ESCR : SCES = 1, ECCR : SCDE = 0

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

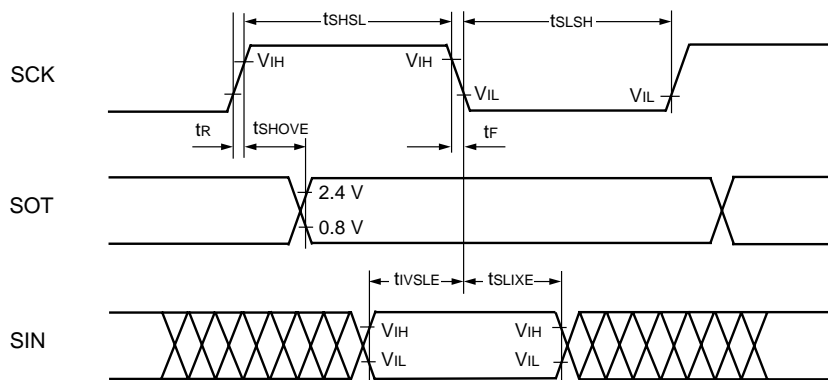
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK2,SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns	
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK2,SCK3 SOT2,SOT3		-50	+50	ns	
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK2,SCK3 SIN2,SIN3		$t_{CP} + 80$	—	ns	
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXI}$	SCK2,SCK3 SIN2,SIN3		0	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK2,SCK3	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3 t_{CP} - t_R$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	SCK2,SCK3		$t_{CP} + 10$	—	ns	
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCK2,SCK3 SOT2,SOT3		—	$2 t_{CP} + 60$	ns	
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLE}$	SCK2,SCK3 SIN2,SIN3		30	—	ns	
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXE}$	SCK2,SCK3 SIN2,SIN3		$t_{CP} + 30$	—	ns	
SCK fall time	$t_F$	SCK2,SCK3		—	10	ns	
SCK rise time	$t_R$	SCK2,SCK3		—	10	ns	

Note :  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to " (1) Clock timing" rating for  $t_{CP}$

- Internal Shift Clock Mode



- External Shift Clock Mode



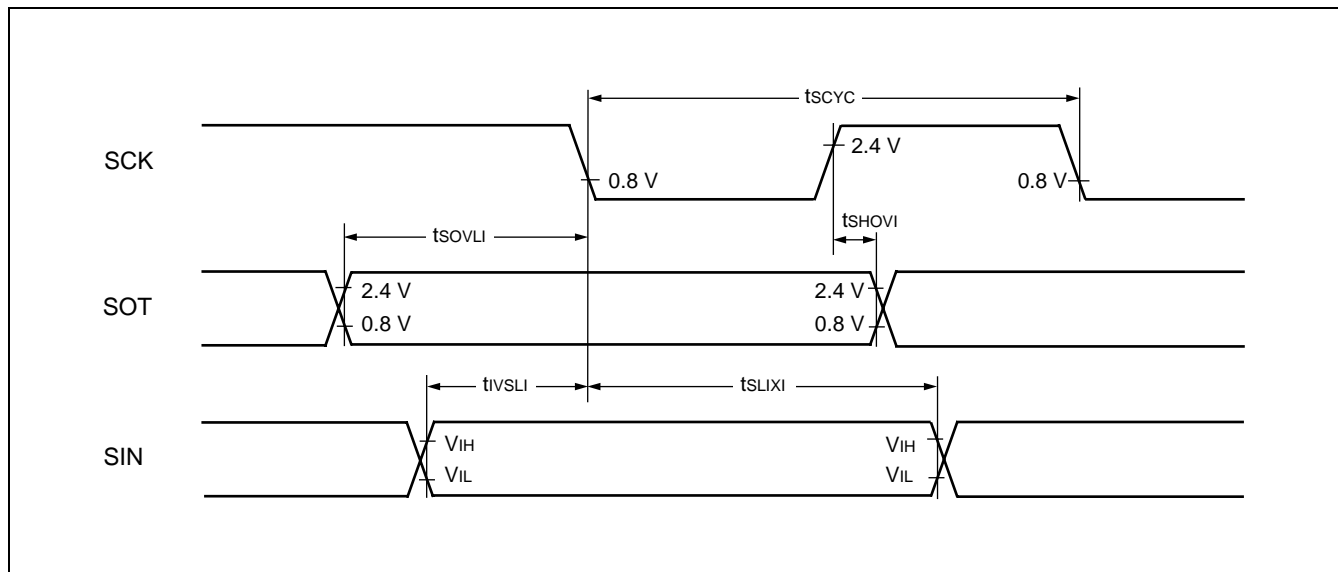
# MB90945 Series

- Bit setting : ESCR : SCES = 0, ECCR : SCDE = 1

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK2,SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns	
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK2,SCK3 SOT2,SOT3		-50	+50	ns	
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK2,SCK3 SIN2,SIN3		$t_{CP} + 80$	—	ns	
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXI}$	SCK2,SCK3 SIN2,SIN3		0	—	ns	
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK2,SCK3 SOT2,SOT3		$3 t_{CP} - 70$	—	ns	

Note :  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for  $t_{CP}$

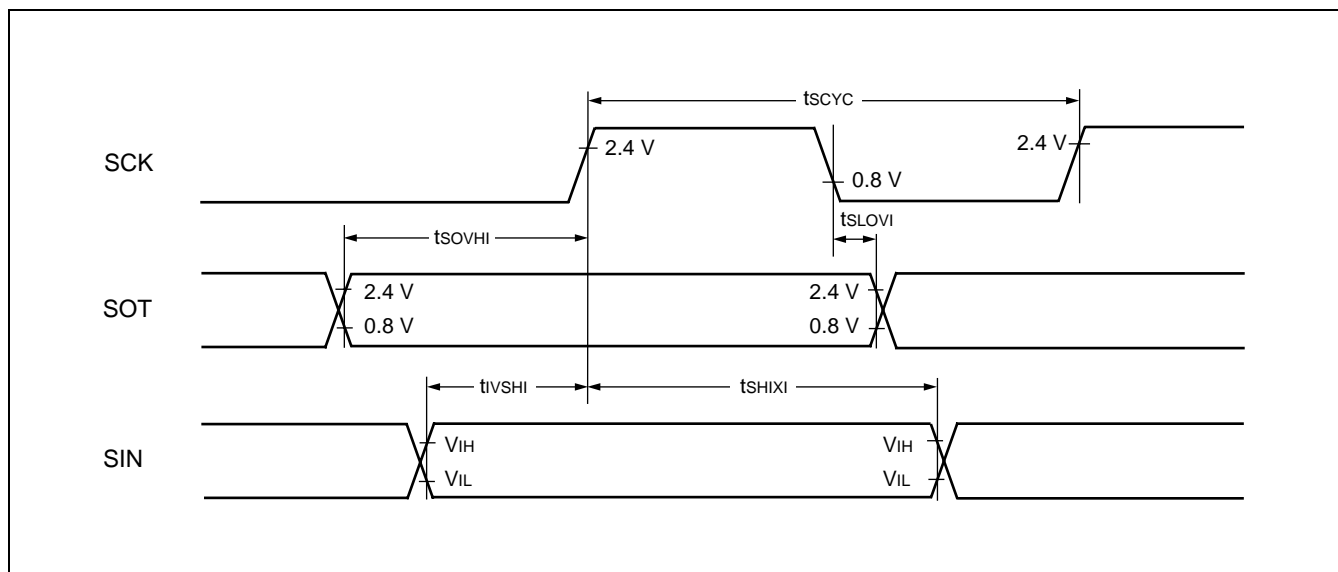


- Bit setting : ESCR : SCES = 1, ECCR : SCDE = 1

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK2,SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns	
SCK $\downarrow$ $\rightarrow$ SOT delay time	$t_{SLOVI}$	SCK2,SCK3 SOT2,SOT3		-50	+50	ns	
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHI}$	SCK2,SCK3 SIN2,SIN3		$t_{CP} + 80$	—	ns	
SCK $\uparrow$ $\rightarrow$ Valid SIN hold time	$t_{SHIXI}$	SCK2,SCK3 SIN2,SIN3		0	—	ns	
SOT $\rightarrow$ SCK $\uparrow$ delay time	$t_{SOVHI}$	SCK2,SCK3 SOT2,SOT3		$3 t_{CP} - 70$	—	ns	

Note :  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for  $t_{CP}$



# MB90945 Series

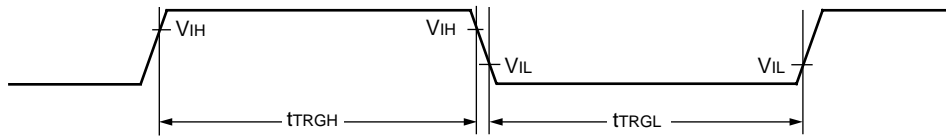
## (6) Trigger Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$	INT0 to INT7	—	200	—	ns	
	$t_{TRGL}$	ADTG		$t_{CP} + 200$	—	ns	

Note :  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for  $t_{CP}$

### • Trigger Input Timing



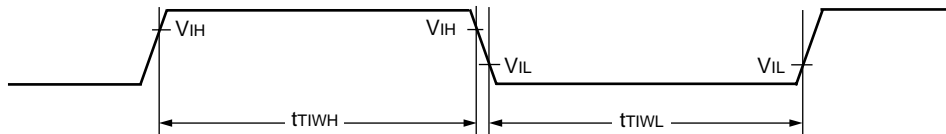
## (7) Timer Related Resource Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$	TIN0, IN0 to IN5	—	$4 t_{CP}$	—	ns	
	$t_{TIWL}$						

Note :  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for  $t_{CP}$

### • Timer Input Timing



## (8) I<sup>2</sup>C Timing

(T<sub>A</sub> = -40 °C to +105 °C, V<sub>CC</sub> = 3.5V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V)

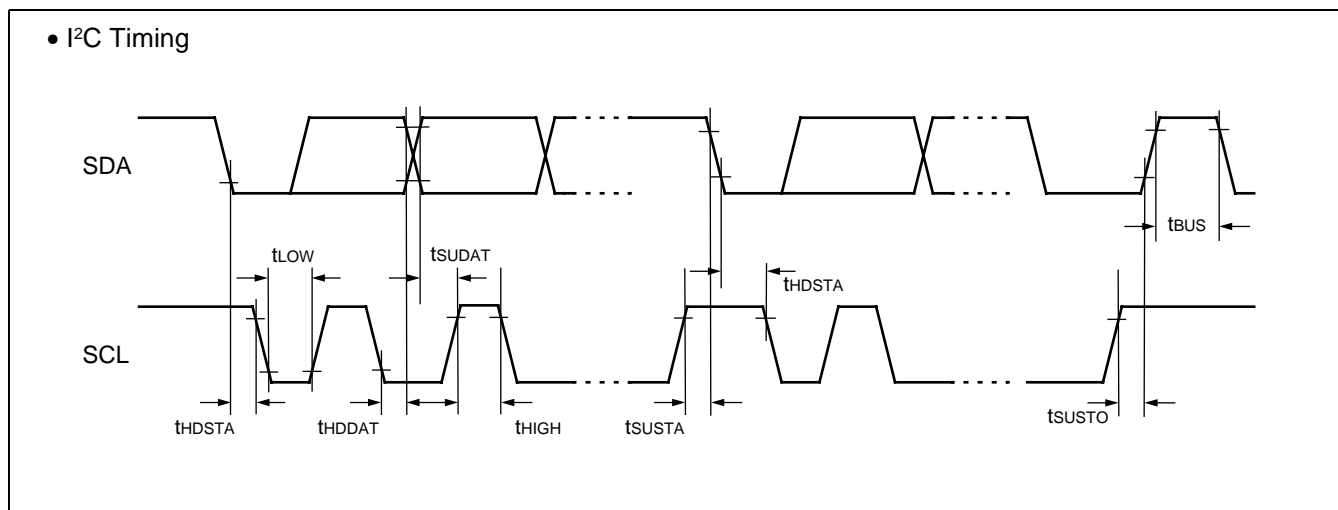
Parameter	Symbol	Condition	Standard-mode		Fast-mode <sup>4</sup>		Unit
			Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	R = 1.3 kΩ, C = 50 pF <sup>*1</sup>	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	—	0.6	—	μs
“L” width of SCL clock	t <sub>LOW</sub>		4.7	—	1.3	—	μs
“H” width of SCL clock	t <sub>HIGH</sub>		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	—	0.6	—	μs
Data hold time SCL ↑ → SDA ↓↑	t <sub>HDDAT</sub>		0	3.45 <sup>*2</sup>	0	0.9 <sup>*3</sup>	μs
Data set-up time SDA ↓↑ → SCL ↑	t <sub>SUDAT</sub>		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	—	0.6	—	μs
Bus free time between STOP and START condition	t <sub>BUS</sub>	4.7	—	1.3	—	μs	

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : The maximum t<sub>HDDAT</sub> only has to be met if the device does not stretch the “L” width (t<sub>LOW</sub>) of the SCL signal.

\*3 : A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SUDAT</sub> ≥ 250 ns must then be met.

\*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



# MB90945 Series

## 5. A/D Converter

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$ ,  $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	$\pm 3.0$	LSB	
Nonlinearity error	—	—	—	—	$\pm 2.5$	LSB	
Differential nonlinearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero reading voltage	$V_{OT}$	AN0 to AN14	$\text{AVRL} - 1.5$	$\text{AVRL} + 0.5$	$\text{AVRL} + 2.5$	LSB	
Full scale reading voltage	$V_{FST}$	AN0 to AN14	$\text{AVRH} - 3.5$	$\text{AVRH} - 1.5$	$\text{AVRH} + 0.5$	LSB	
Compare time	—	—	3.3	66 $t_{CP}$	16500	$\mu\text{s}$	
Sampling time	—	—	1.6	32 $t_{CP}$	$\infty$	$\mu\text{s}$	
Analog port input current	$I_{AIN}$	AN0 to AN14	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage range	$V_{AIN}$	AN0 to AN14	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	$\text{AV}_{CC}$	V	
		AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	$I_A$	$\text{AV}_{CC}$	—	3.5	7.5	mA	
	$I_{AH}$	$\text{AV}_{CC}$	—	—	5	$\mu\text{A}$	*
Reference voltage current	$I_R$	AVRH	—	165	250	$\mu\text{A}$	
	$I_{RH}$	AVRH	—	—	5	$\mu\text{A}$	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

\* : When not operating A/D converter, this is the current ( $V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$ ) .

### Terminology

- Conversion error : Absolute maximum conversion deviation with respect to the theoretical conversion line.
- Nonlinearity : Relative maximum conversion deviation with respect to the theoretical conversion line connecting to the device unique zero reading voltage and full scale reading voltage.
- Differential nonlinearity : Max conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.
- Zero reading voltage : Input voltage which results in the minimum conversion value.
- Full scale reading voltage : Input voltage which results in the maximum conversion value.

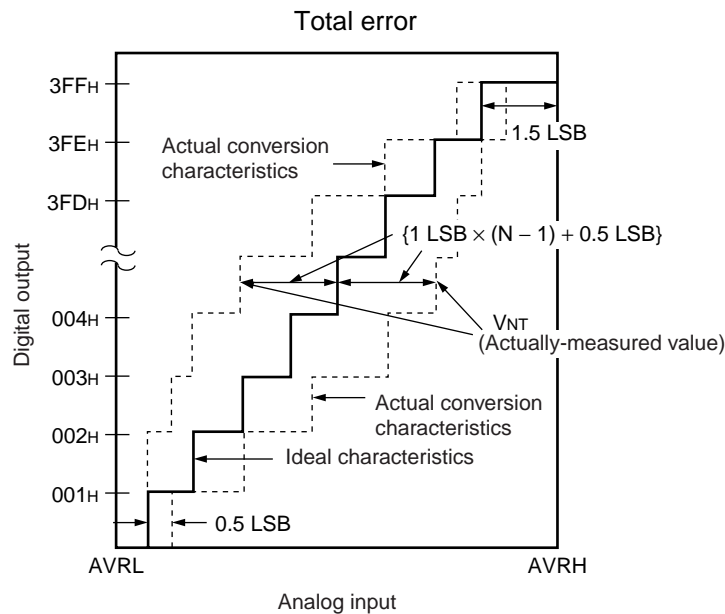
Notes : •  $t_{CP}$  is the machine clock cycle time (Unit : ns) . Refer to "4. AC Characteristics (1) Clock timing" rating for  $t_{CP}$

- The accuracy gets worse as  $|\text{AVRH} - \text{AVRL}|$  becomes smaller.



## 6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linear error : Deviation between a line across zero-transition line ( "00 0000 0000"  $\leftarrow \rightarrow$  "00 0000 0001" ) and full-scale transition line ( "11 1111 1110"  $\leftarrow \rightarrow$  "11 1111 1111" ) and actual conversion characteristics.
- Differential linear error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$V_{OT} \text{ (Ideal value)} = AVRL + 0.5 \text{ LSB [V]}$$

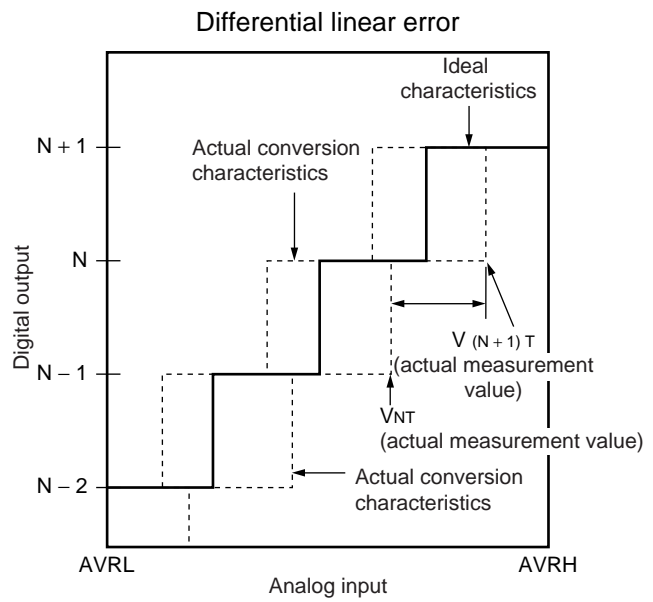
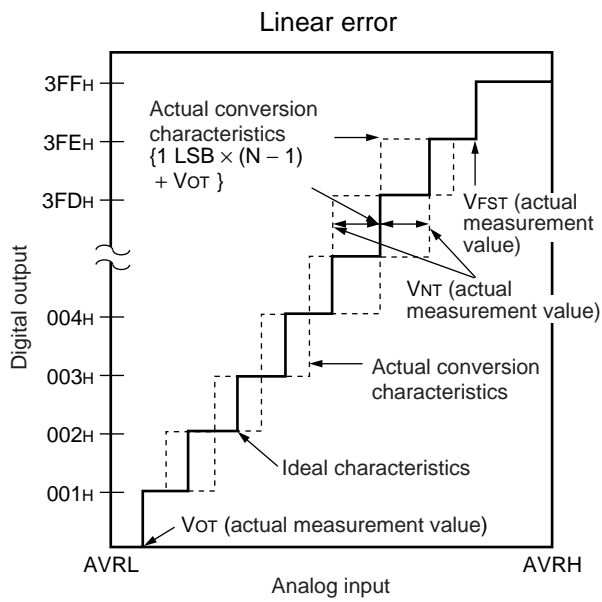
$$V_{FST} \text{ (Ideal value)} = AVRH - 1.5 \text{ LSB [V]}$$

$V_{NT}$  : A voltage at which digital output transitions from (N - 1) to N.

(Continued)

# MB90945 Series

(Continued)



$$\text{Linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

$V_{OT}$  : Voltage at which digital output transits from "000H" to "001H."

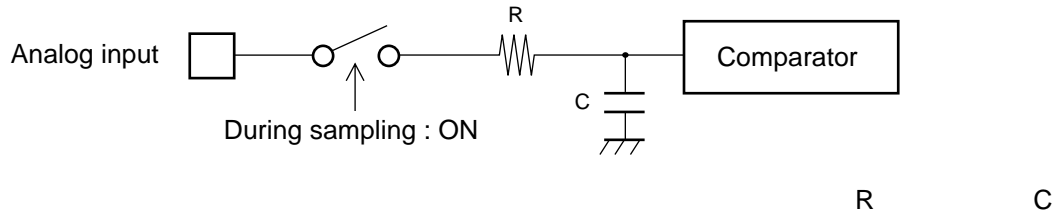
$V_{FST}$  : Voltage at which digital output transits from "3FEH" to "3FFH."

## 7. Notes on A/D Converter Section

### • About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

#### • Analog input circuit model

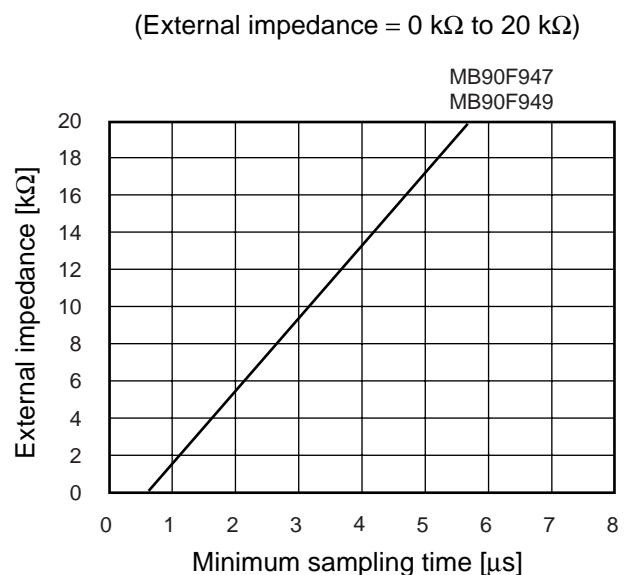
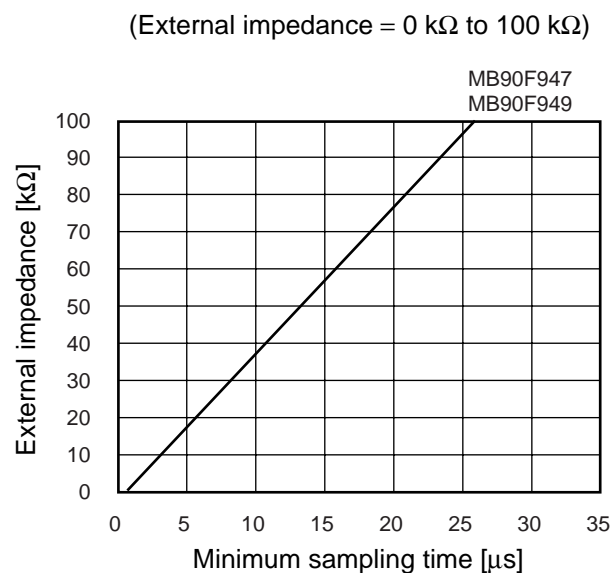


Note : The values are reference values.

	R	C
MB90F946A/947A/ F947/F947A/F949/ F949A	2.4 kΩ (Max)	36.4 pF (Max)

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

#### • The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

### • About the error

The accuracy gets worse as  $|AVRH - AVRL|$  becomes smaller.

# MB90945 Series

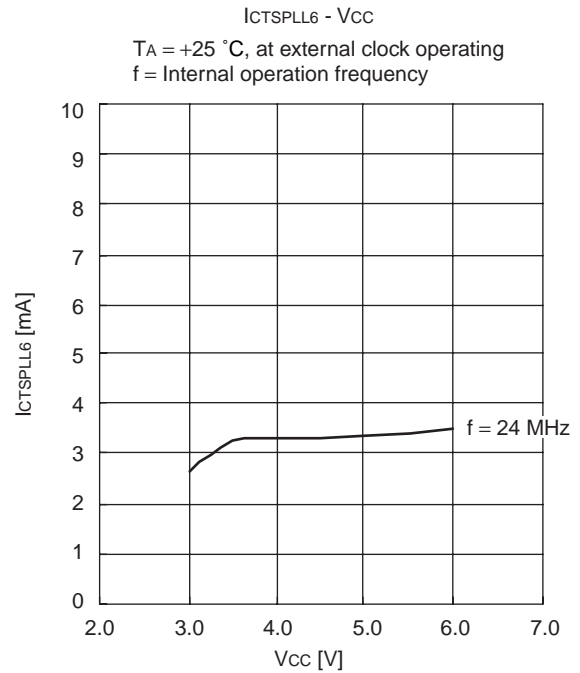
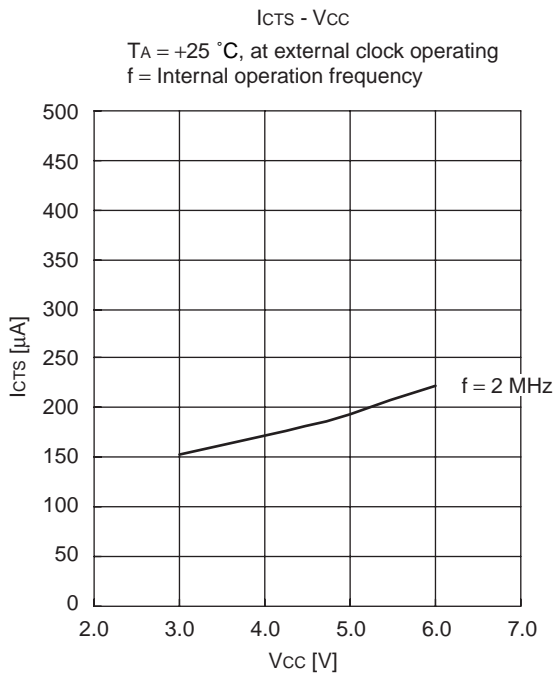
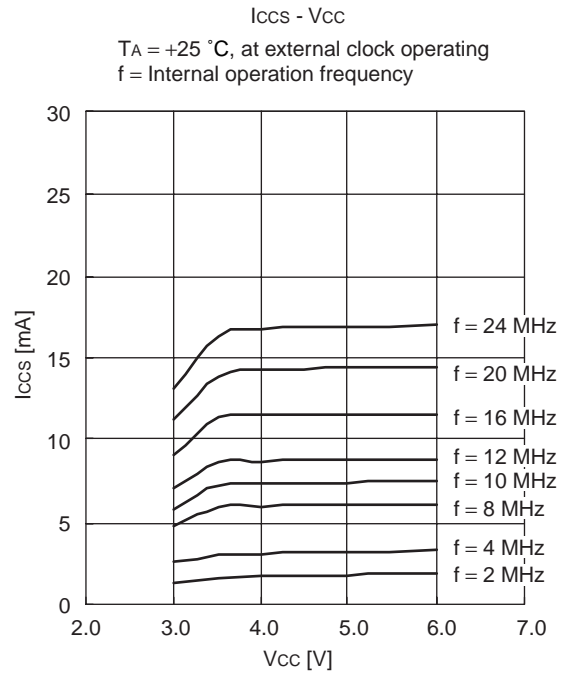
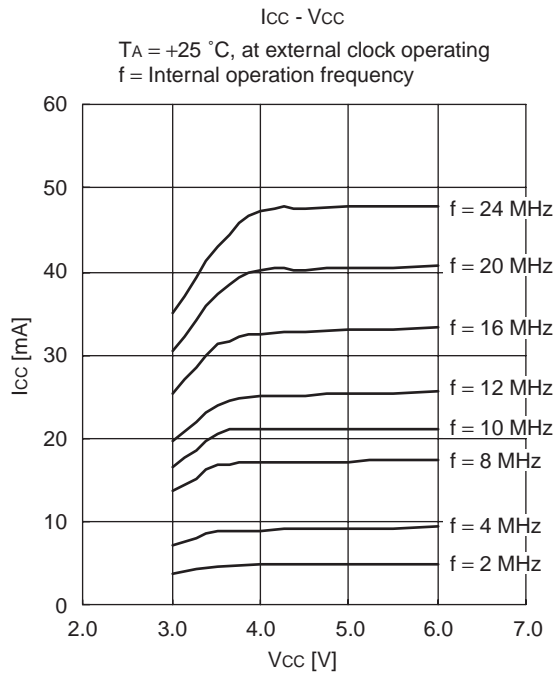
## 8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T <sub>A</sub> = +25 °C V <sub>CC</sub> = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	5	—	s	MB90F947, Excludes programming prior to erasure
		—	7	—	s	MB90F949, Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	μs	Except for the overhead time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average T <sub>A</sub> = +85 °C	20	—	—	Year	*

\* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

## EXAMPLE CHARACTERISTICS

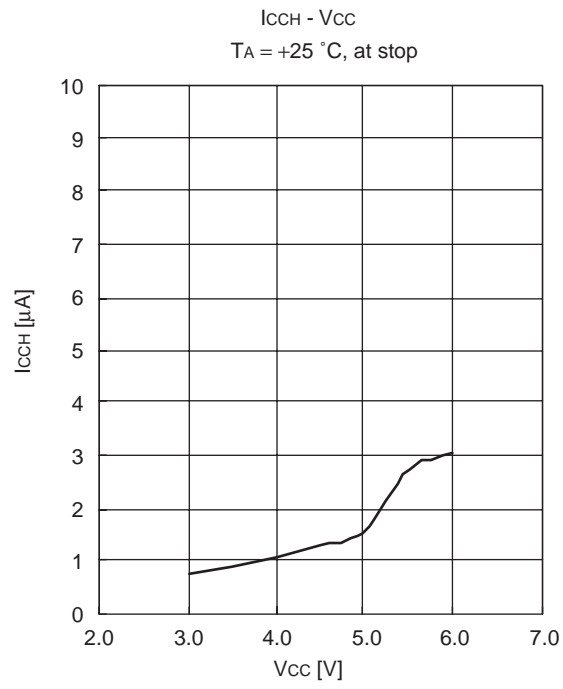
●MB90F947



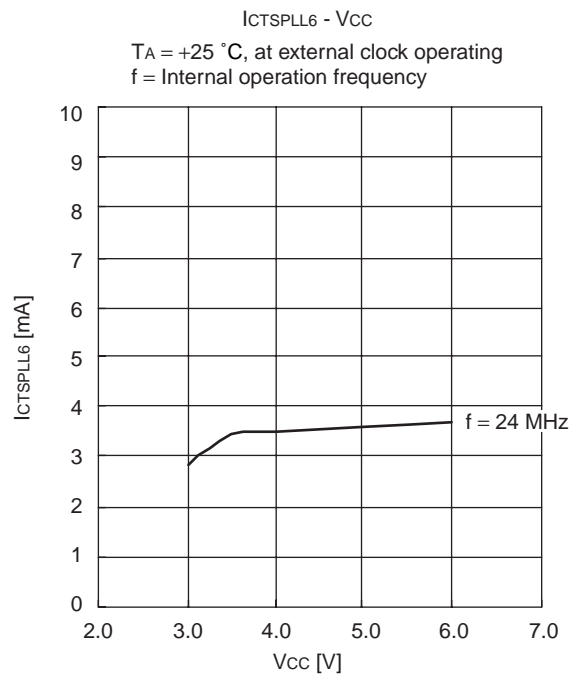
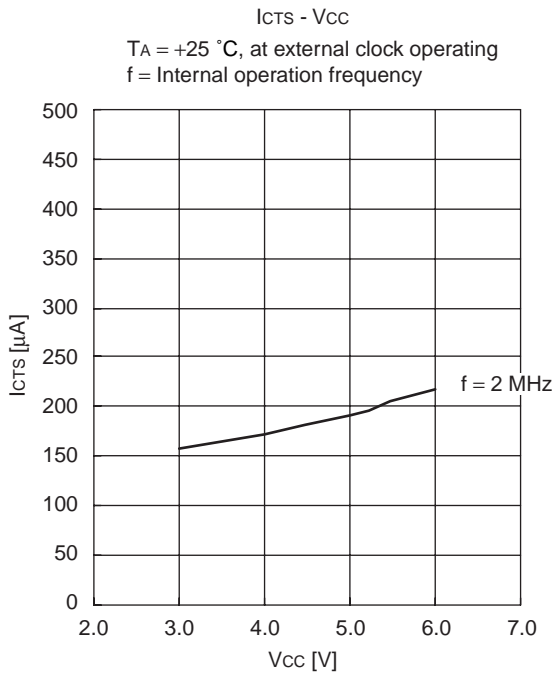
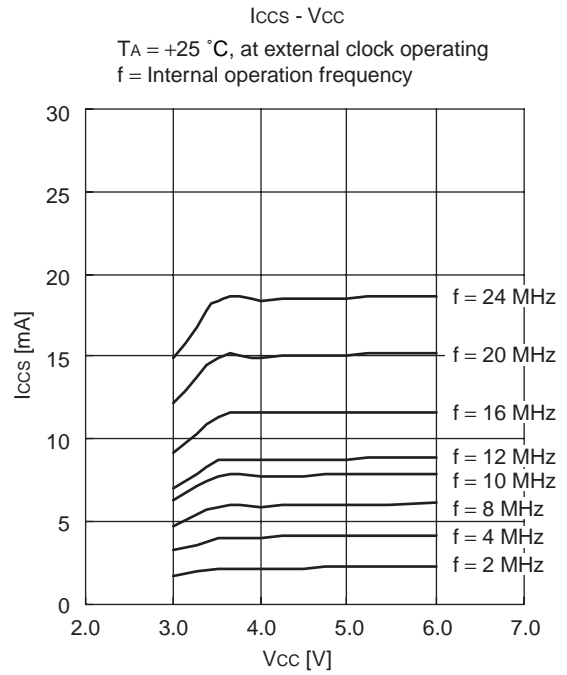
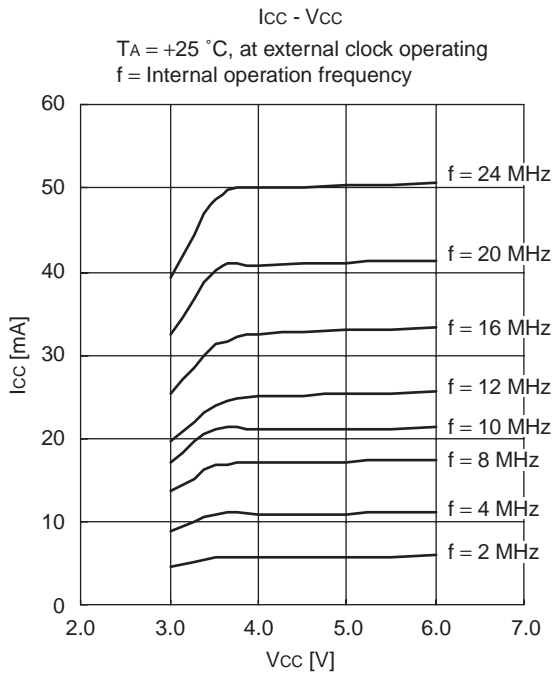
(Continued)

# MB90945 Series

(Continued)



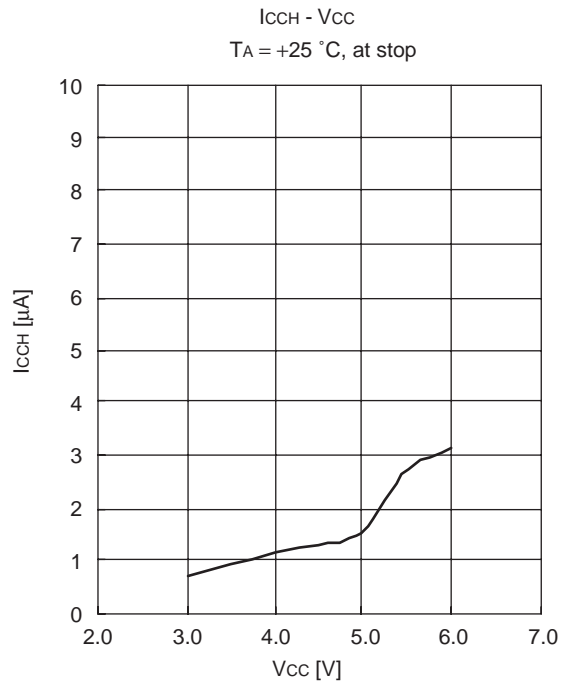
•MB90F949



(Continued)

# MB90945 Series

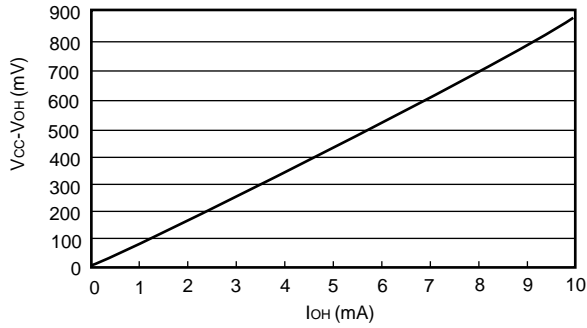
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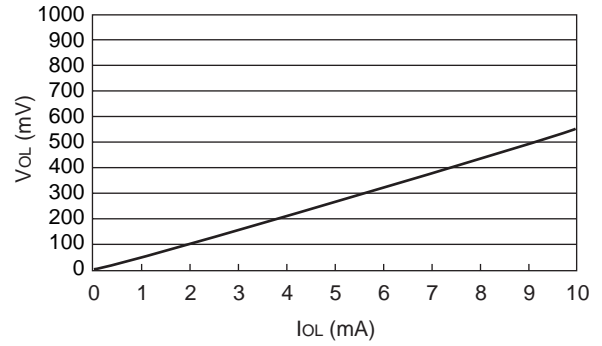


## •I/O Characteristic

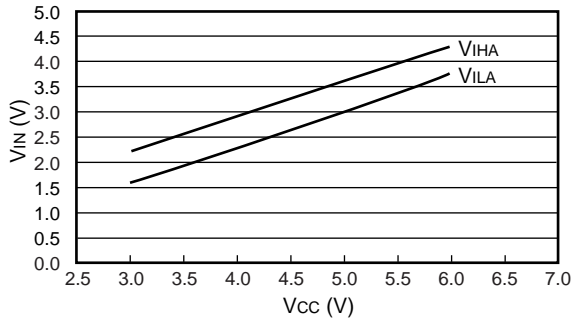
$(V_{CC}-V_{OH}) - I_{OH}$   
 $T_A = +25\text{ }^\circ\text{C}, V_{CC} = 4.5\text{ V}$



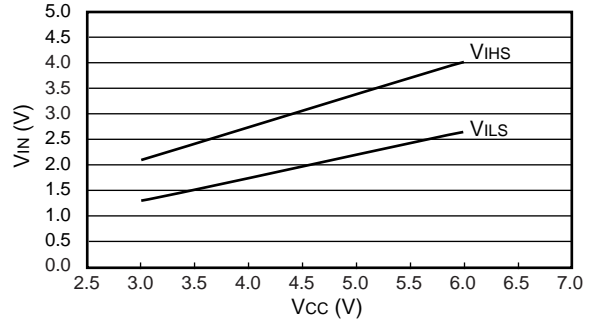
$V_{OL} - I_{OL}$   
 $T_A = +25\text{ }^\circ\text{C}, V_{CC} = 4.5\text{ V}$



Automotive  $V_{IN} - V_{CC}$   
 $T_A = +25\text{ }^\circ\text{C}$



CMOS  $V_{IN} - V_{CC}$   
 CAN RX pin, I<sup>2</sup>C pin  
 $T_A = +25\text{ }^\circ\text{C}$



# MB90945 Series

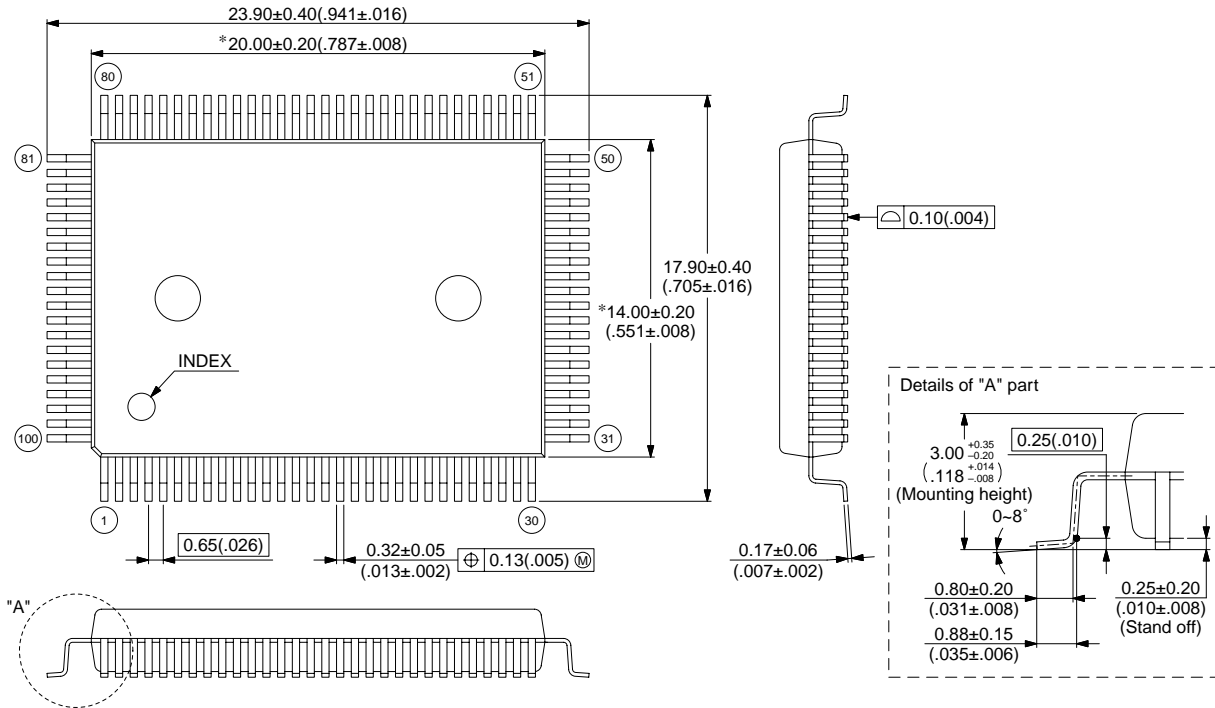
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F946APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90947APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F947PF	100-pin Plastic QFP (FPT-100P-M06)	It is recommended to use MB90F947A, because MB90F947 does not support clock modulation and CAN at the same time
MB90F947APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F949PF	100-pin Plastic QFP (FPT-100P-M06)	It is recommended to use MB90F949A, because MB90F949 does not support clock modulation and CAN at the same time
MB90F949APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V390HACR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation It is recommended to use MB90V390HB
MB90V390HBCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation

## ■ PACKAGE DIMENSIONS

100-pin Plastic QFP  
(FPT-100P-M06)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

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