Integrated Circuit Systems, Inc.

ICS9248-185

Frequency Generator & Integrated Buffers for PENTIUM/Pro™ & K6

Recommended Application:

VIA PM133 chipset

Output Features:

- 2 - CPUs @ 2.5V
- 5 - SDRAM @ 3.3V
- 3 - PCI @ 3.3V,
- 1 - 48MHz, @ 3.3V fixed.
- 2 - REF @ 3.3V, 14.318MHz.

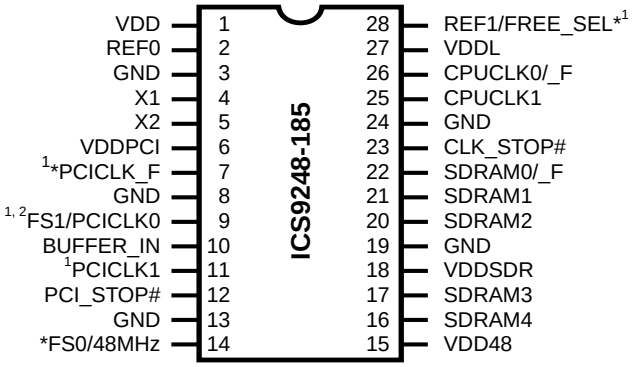
Features:

- Up to 133MHz frequency support
- Support power management: PCI_STOP & CLK_STOP
- Spread spectrum for EMI control (-0.5% down spread).
- Uses external 14.318MHz crystal
- FS pins for frequency select

Key Specifications:

- CPU – PCI Skew: 1-4ns
- PCI – PCI Skew: ±500ps
- CPU – CPU Skew: ±175ps
- CPU Jitter: 250ps (cyc-cyc)
- PCI Jitter: 500ps (cyc-cyc)

Pin Configuration

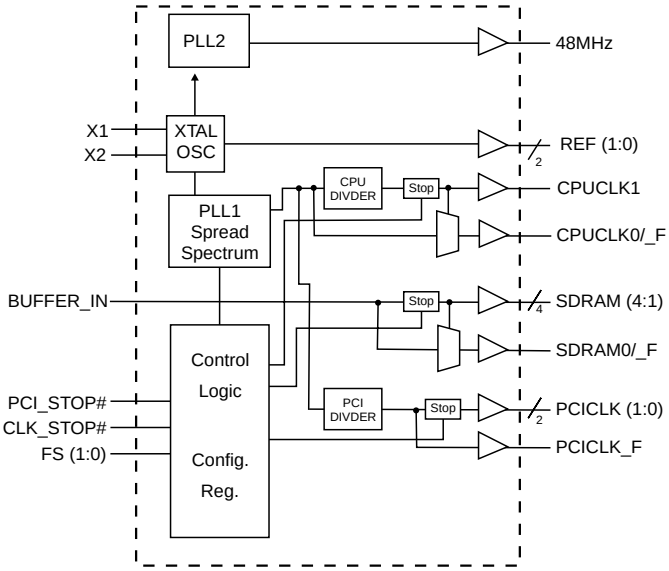


28-Pin SSOP/TSSOP

* Internal Pull-up Resistor of 120K to VDD

1. These pin will have 2X drive strength
2. FS1 is a pull down

Block Diagram



Frequency Select

FS1	FS0	CPUCLK	PCICLK	Down Spread
0	0	66.66	33.33	-0.5%
0	1	100.00	33.33	-0.5%
1	0	97.00	32.33	-0.5%
1	1	133.33	33.33	-0.5%

General Description

The **ICS9248-185** is the single chip clock solution for Notebook designs using the 440BX or the VIA Apollo Pro 133 style chipset. It provides all necessary clock signals for such a system. The **ICS9248-185** provides CPU and PCI clocks with continous spread spectrum. The **ICS9248-185** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 6, 15, 18,	VDD	PWR	Power supply, nominal 3.3V
2	REF0	OUT	14.318 Mhz reference clock.This REF output is the STRONGER buffer for ISA BUS loads
3, 8, 13, 19, 24	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz.
7	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
9	FS1[1, 2]	IN	Frequency select pin. Latched Input.
	PCICLK0	OUT	PCI clock output. Synchronous to CPU clocks with 1-4ns skew (CPU early)
10	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
11	PCICLK1	OUT	PCI clock output. Synchronous to CPU clocks with 1-4ns skew (CPU early)
12	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low (In mobile mode, MODE=0)
14	FS0[1, 2]	IN	Frequency select pin. Latched Input
	48MHz	OUT	48MHz output clock
16, 17, 20, 21	SDRAM (4:1)	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
22	SDRAM0/_F	OUT	Either free running SDRAM or stoppable depending on FREE_SEL
23	CLK_STOP#	IN	This asynchronous input halts CPUCLKs, & SDRAMs at logic "0" level when driven low.
25	CPUCLK1	OUT	CPU clock output, powered by VDDL
26	CPUCLK0/_F	OUT	Either free running CPUCLK or stoppable depending on FREE_SEL
27	VDDL	PWR	Supply for CPU clocks 2.5V
28	FREE_SEL	IN	Selects CPUCLK0/_F and SDRAM0/_F to be either free running or stoppable by CLK_STOP#. When FREE_SEL is set to (0) low the above clocks are free running - when set to (1) high, the clocks are stoppable.
	REF1	OUT	14.318 MHz reference clock.

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Operating Supply Current	$I_{DD3.3OP}$	C_L = 30 pF; Select @ 66MHz		63	150	mA
		C_L = 30 pF; Select @ 100MHz		67	170	
		C_L = 30 pF; Select @ 133MHz		73	180	
Powerdown Current	I_{DDPD}	CL = 0 pF; Input address VDD or GND			600	µA
Input Frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			5.5	ms
Skew[1]	$t_{CPU-PCI1}$	V_T = 1.5 V	1	28	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2A}	I_{OH} = -20 mA	2.4	2.85		V
Output Low Voltage	V_{OL2A}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-45	-27	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	22	29		mA
Rise Time[1]	t_{r2A}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.9	1.6	ns
Fall Time[1]	t_{f2A}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle[1]	d_{t2A}	V_T = 1.5 V	45	50	55	%
Skew window[1]	t_{sk2A}	V_T = 1.5 V		35	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2A}$	V_T = 1.5 V Dram not running, CPU=66.6MHz		123	150	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2A}$	V_T = 1.5 V Dram running		119	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; VDDL= 2.5V, +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2A}	I_{OH} = -20 mA	2	2.3		V
Output Low Voltage	V_{OL2A}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-39	-21	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	22	26		mA
Rise Time[1]	t_{r2A}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		0.96	1.6	ns
Fall Time[1]	t_{f2A}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.06	1.6	ns
Duty Cycle[1]	d_{t2A}	V_T = 1.25 V	45	50.3	55	%
Skew window[1]	t_{sk2A}	V_T = 1.25 V		35	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2A}$	V_T = 1.25 V Dram not running		123	150	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2A}$	V_T = 1.25 V Dram running		119	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V , VDDL = 2.5V, +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-33	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	38	43		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.51	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.47	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50.1	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		58	500	ps
Jitter, Cycle to cycle	t_{cycle}	V_T = 1.5 V		145	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3 V, VDDL= 2.50V, +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL3}	I_{OL} = 19 mA		0.3	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-69	-46	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	32	42		mA
Rise Time[1]	T_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.07	1.3	ns
Fall Time[1]	T_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.3	2	ns
Duty Cycle[1]	D_{t3}	V_T = 1.5 V	45	50.8	55	%
Skew window[1]	T_{sk3}	V_T = 1.5 V		104	250	ps
Propagation Time[1] (Buffer In to output)	T_{sk3}	V_T = 1.5 V			5	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = 3.3 V, VDDL= 2.5V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL} = 6 mA		0.22	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.11	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.14	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52.1	55	%
Jitter, cycle to cycle[1]	$t_{jcycle5}$	V_T = 1.5 V	-600	848	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz

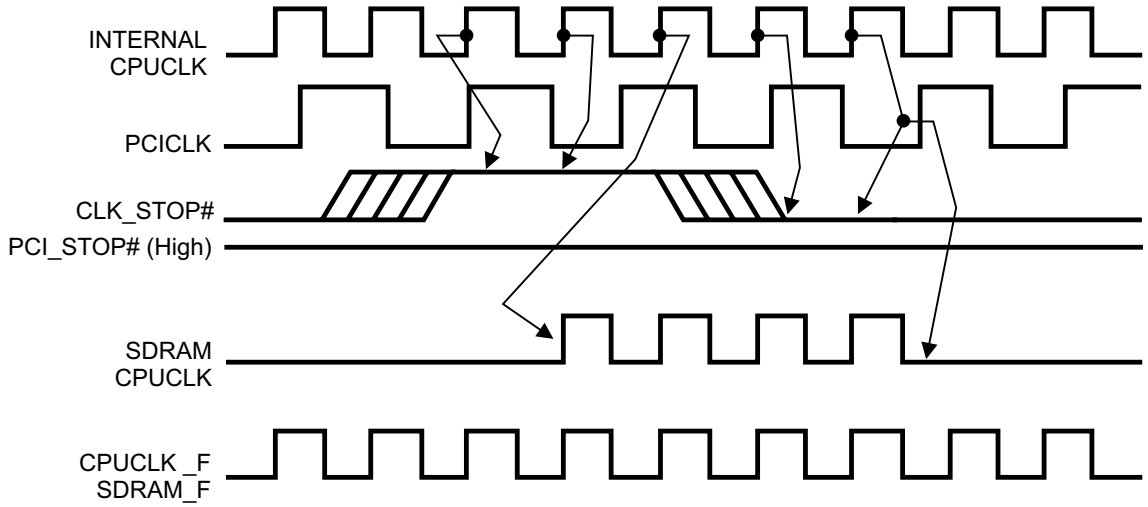
T_A = 0 - 70C; V_{DD} = 3.3 V, VDDL= 2.5V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL} = 6 mA		0.22	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.79	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.92	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	50.8	55	%
Jitter, cycle to cycle	t_{jcycle}	V_T = 1.5 V		267	500	ps

[1]Guaranteed by design, not 100% tested in production.

CLK_STOP# Timing Diagram

CLK_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the **ICS9248-185**. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

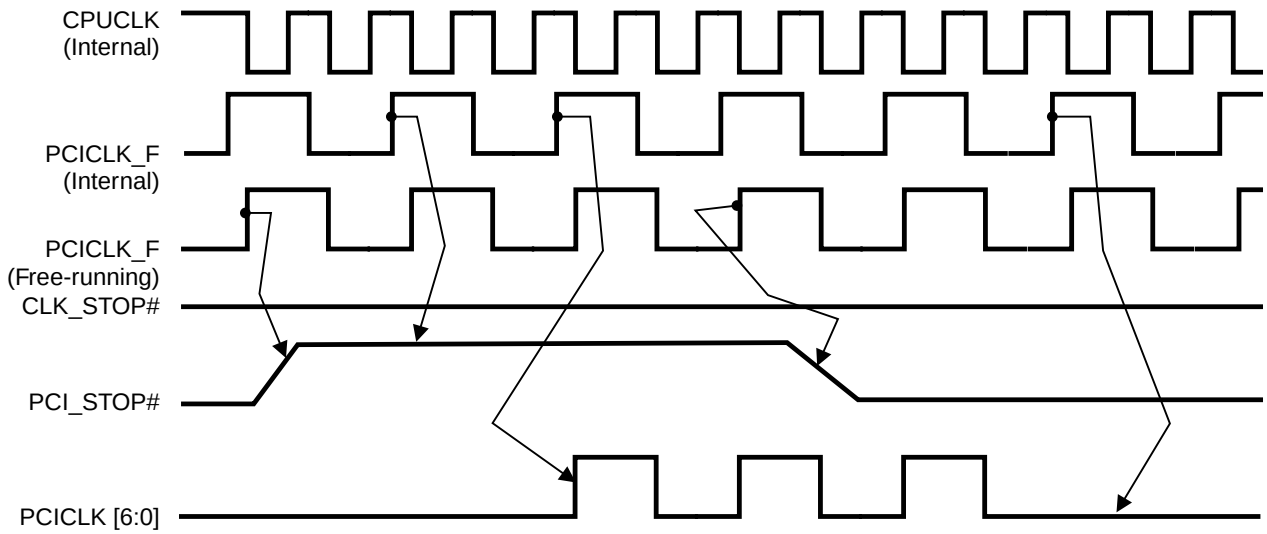


Notes:

1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-185.
3. All other clocks continue to run undisturbed.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-185**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-185** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only three rising PCICLK clocks, off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. CLK_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

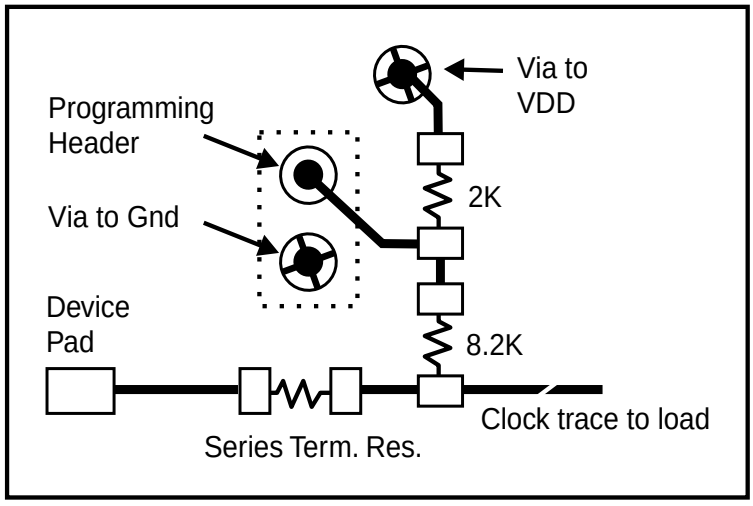
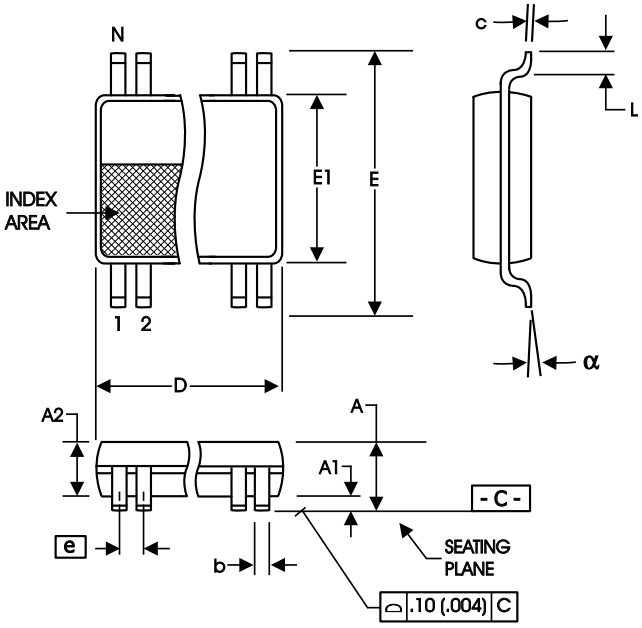


Fig. 1



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

Ordering Information

ICS9248yF-185-T

Example:

ICS XXXX y F - PPP -

T

Designation for tape and reel packaging

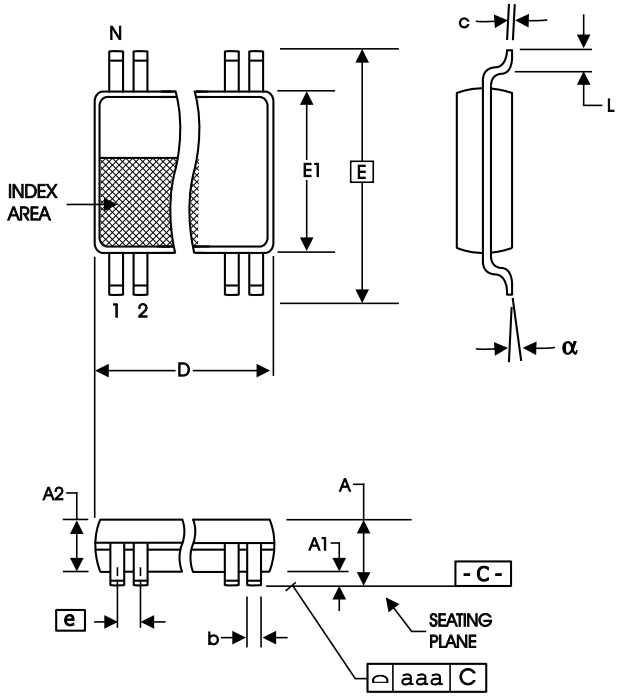
Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

Ordering Information

ICS9248yG-185-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device