

FDN339AN

N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

This N-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

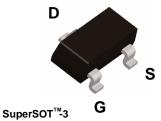
Applications

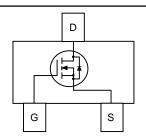
- DC/DC converter
- Load switch

Features

• 3 A, 20 V.
$$R_{DS(ON)} = 0.035 \Omega$$
 @ $V_{GS} = 4.5 V$ $R_{DS(ON)} = 0.050 \Omega$ @ $V_{GS} = 2.5 V$.

- Low gate charge (7nC typical).
- \bullet High performance trench technology for extremely low $R_{\mbox{\tiny DS(ON)}}.$
- High power and current handling capability.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V _{DSS}	Drain-Source Voltage	20	V	
V _{GSS}	Gate-Source Voltage	<u>±</u> 8	V	
I _D	Drain Current - Continuous	(Note 1a)	3	А
	- Pulsed		20	
P _D	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T _J , T _{stg}	Operating and Storage Junction Temperature	-55 to +150	°C	

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
R _{0.IC}	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity	
339	FDN339AN	7"	8mm	3000 units	

Symbol	Parameter	Min	Тур	Max	Units	
Off Char	acteristics	•				
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	20	Ì		V
<u>ΔBVpss</u> ΔT,j	Breakdown Voltage Temperature Coefficient	I _D = 250 μA,Referenced to 25°C		14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 8 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.4	0.85	1.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to $25^{\circ} C$		-3		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 4.5 V, I _D = 3 A V _{GS} = 4.5 V, I _D = 3 A, T _J =125°C V _{GS} = 2.5 V, I _D = 2.4 A		0.029 0.040 0.039	0.035 0.061 0.050	Ω
I _{D(on)}	On-State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	10			Α
g FS	Forward Transconductance	V _{DS} = 5 V, I _D = 3 A		11		S
Dynamic	Characteristics	•				
C _{iss}	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$		700		pF
Coss	Output Capacitance	f = 1.0 MHz		175		pF
Crss	Reverse Transfer Capacitance			85		pF
Switchin	g Characteristics (Note 2)	•			•	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 10 \text{ V}, I_D = 1 \text{ A},$	l	8	16	ns
t _r	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		10	18	ns
t _{d(off)}	Turn-Off Delay Time			18	29	ns
t _f	Turn-Off Fall Time			5	10	ns
Qg	Total Gate Charge	V _{DS} = 10 V, I _D = 3 A,		7	10	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 4.5 V	1	1.2		nC
Q _{gd}	Gate-Drain Charge			1.9		nC
Drain-Sc	ource Diode Characteristics a	and Maximum Ratings				
l _s	Maximum Continuous Drain-Source				0.42	Α
V _{SD}	Drain-Source Diode Forward Voltage	e V _{GS} = 0 V, I _S = 0.42 A (Note	 	0.65	1.2	V

^{1:} R_{BJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² Pad of 2 oz. Cu.



b) 270°C/W on a minimum mounting pad of 2 oz. Cu.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width $\leq 300~\mu\text{s},~\text{Duty Cycle} \leq 2.0\%$

Typical Characteristics

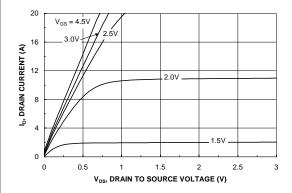


Figure 1. On-Region Characteristics.

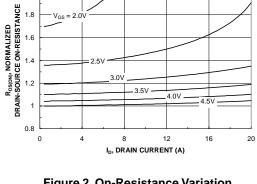


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

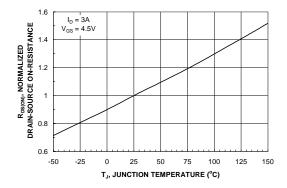


Figure 3. On-Resistance Variation with Temperature.

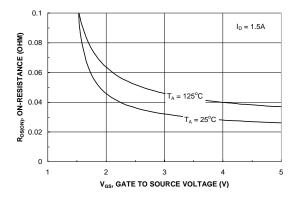


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

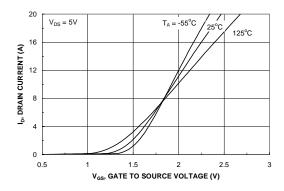


Figure 5. Transfer Characteristics.

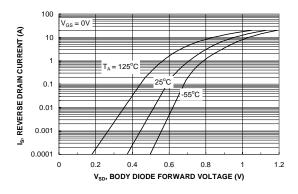
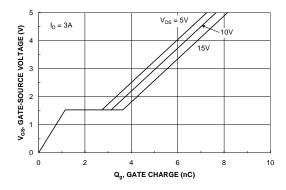


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)



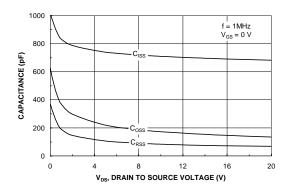
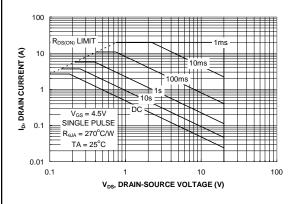


Figure 7. Gate Charge Characteristics.





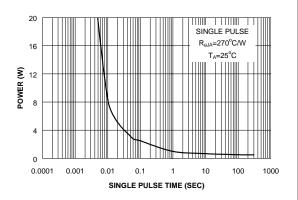


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

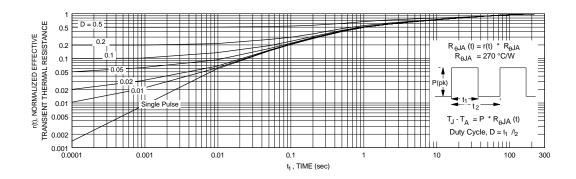
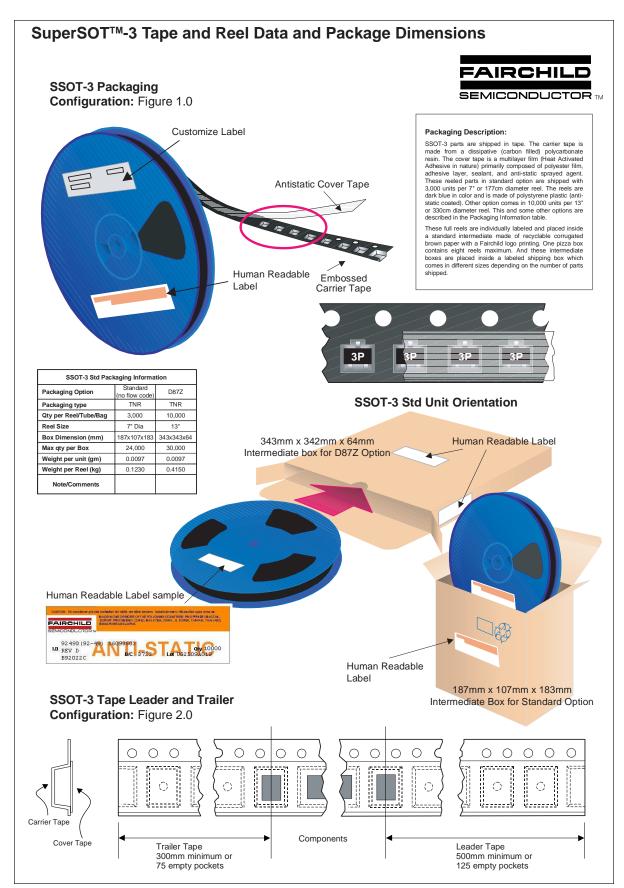


Figure 11. Transient Thermal Response Curve.

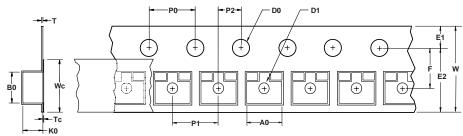
Thermal characterization performed using the conditions described in Note 1b. Transient themal response will change depending on the circuit board design.

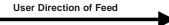




SSOT-3 Embossed Carrier Tape

Configuration: Figure 3.0



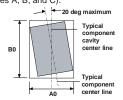


	Dimensions are in millimeter													
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-02

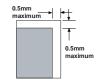
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

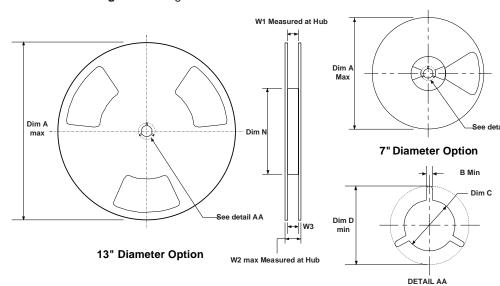


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

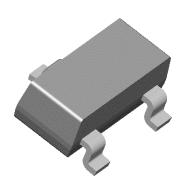
SSOT-3 Reel Configuration: Figure 4.0

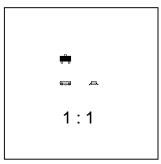


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

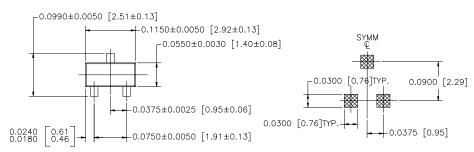
SuperSOT™-3 (FS PKG Code 32)



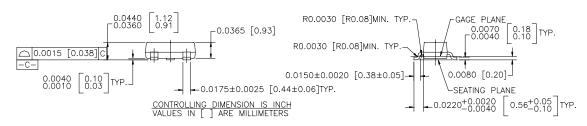


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

- 1. STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
- 2. NO JEDEC REGISTRATION AS OF DEC. 1995.

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