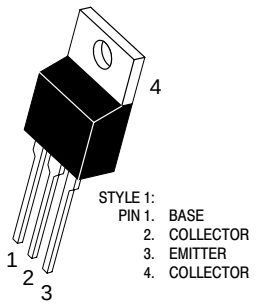
Plastic High Power Silicon Transistor

NPN
BD809
PNP
BD810

. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 2.0 Adc

10 AMPERE
POWER TRANSISTORS
PNP SILICON
60, 80 VOLTS
90 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	 80	— —	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	 —	 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
DC Current Gain (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 4.0 A, V_{CE} = 2.0 V)	h_{FE}	 30 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	—	1.1	Vdc
Base–Emitter On Voltage* (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
Current–Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	1.5	—	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

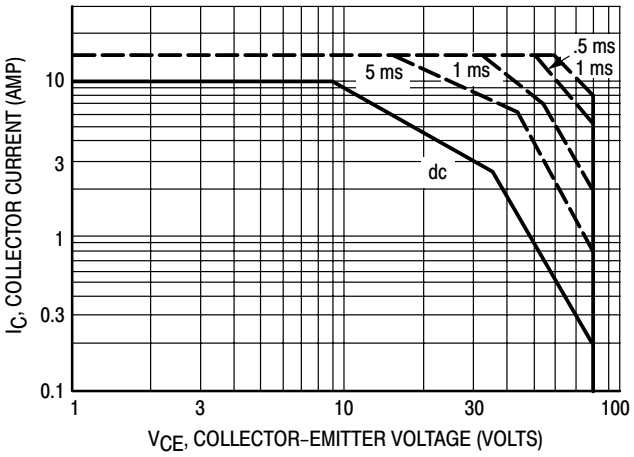


Figure 1. Active Region DC Safe Operating Area (see Note 1)

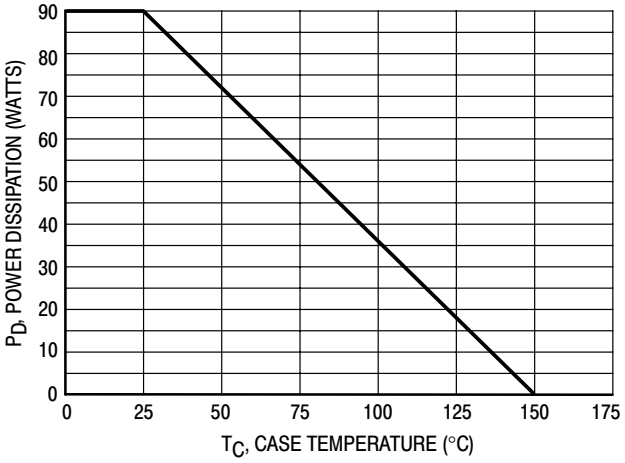


Figure 2. Power–Temperature Derating Curve

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PNP
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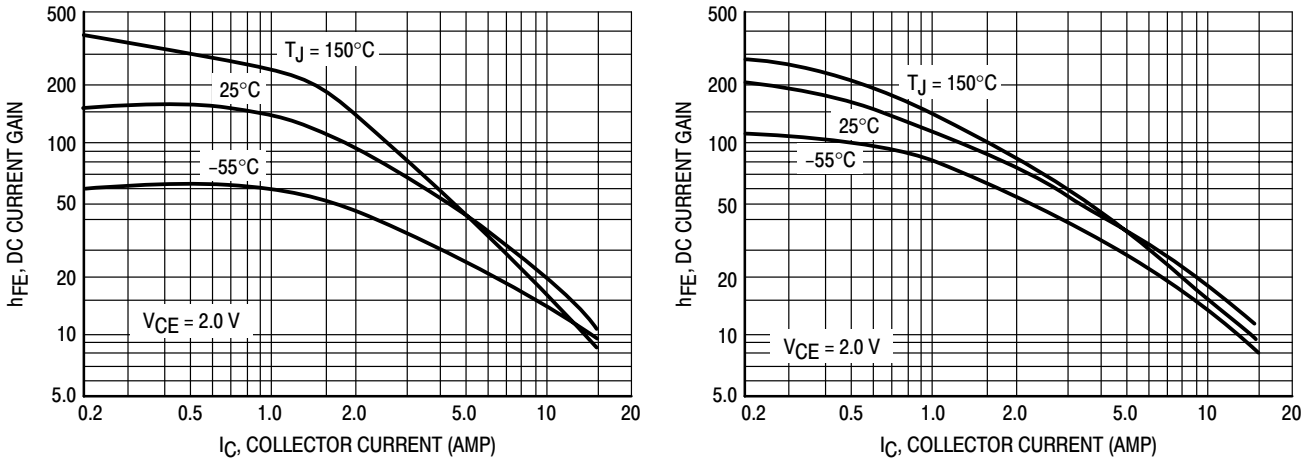


Figure 3. DC Current Gain

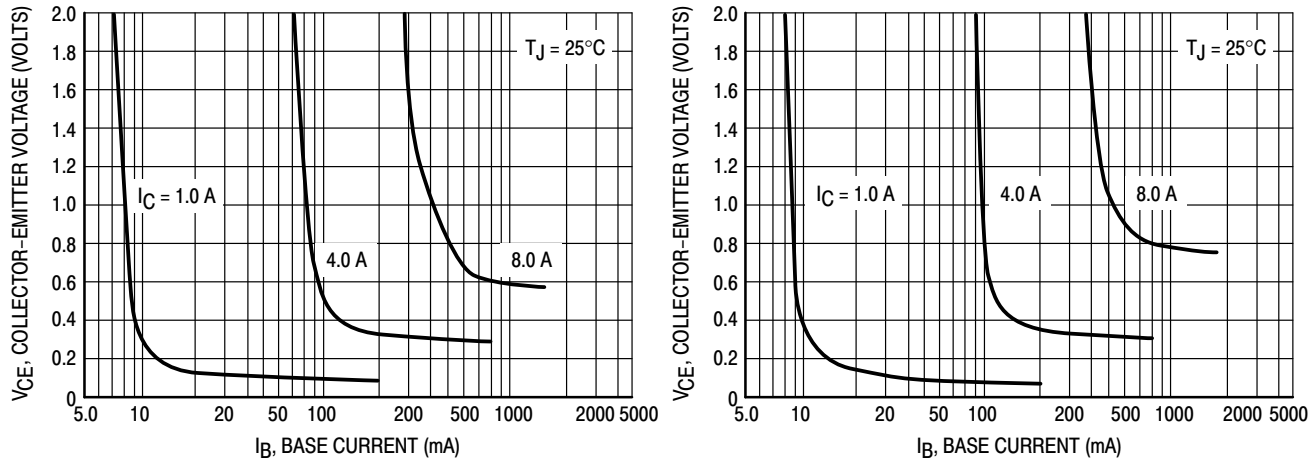


Figure 4. Collector Saturation Region

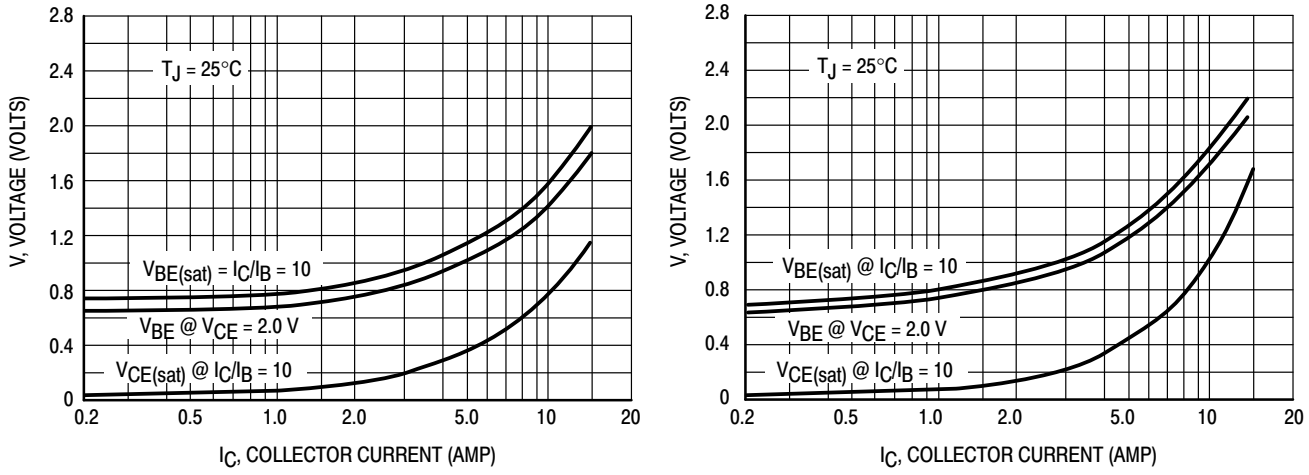


Figure 5. “On” Voltages

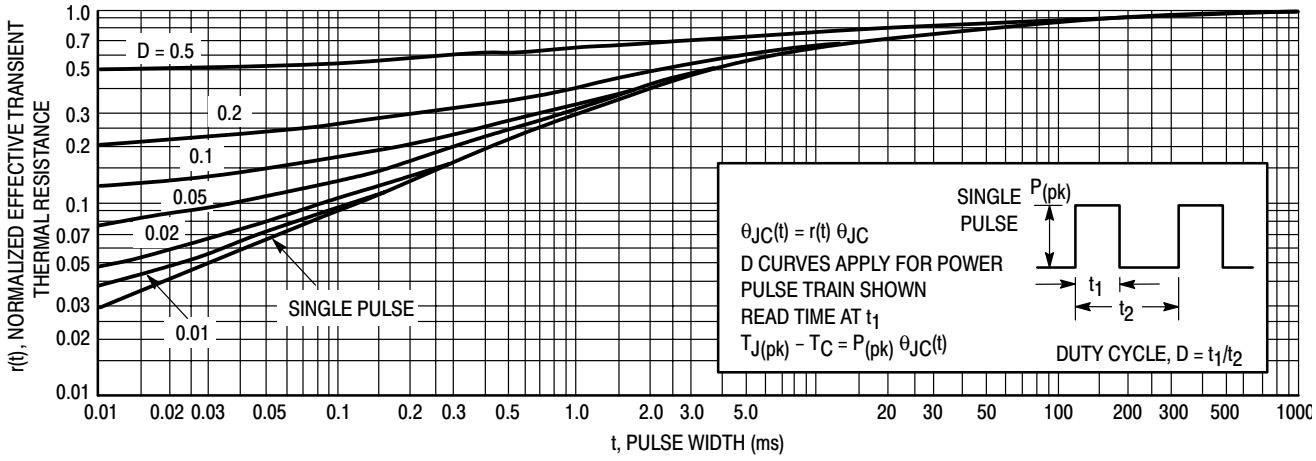


Figure 6. Thermal Response

Note 1:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

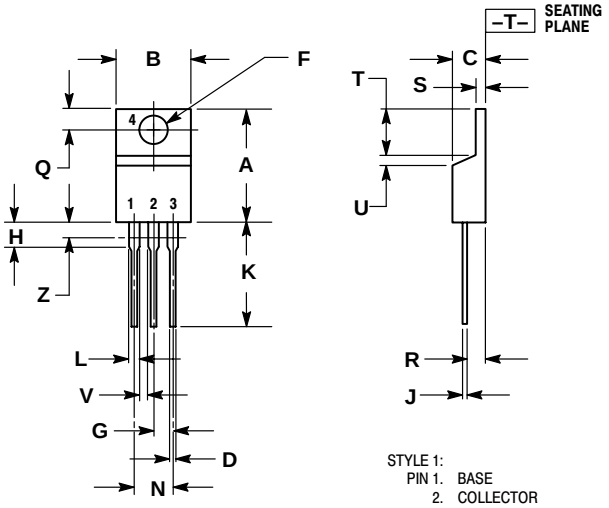
The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Notes

Notes

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AA



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

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