

Reset Circuits with Manual Reset Input

FEATURES

- Ultra Low Supply Current 1 μ A(typ.)
- Guaranteed Reset Valid to Vcc=0.9V
- Available in two Output Types: Push-Pull Active Low (AIC811), Push-Pull Active High (AIC812)
- 140ms Min. Power-On Reset Pulse Width
- Internally Fixed Threshold 2.3V, 2.6V, 2.9V, 3.1V, 4.0V, 4.4V, and 4.6V
- Tight Voltage Threshold Tolerance: 1.5%
- Low profile Package: SOT-23-5

APPLICATIONS

- Notebook Computers
- Digital Still Cameras
- PDAs
- Critical Microprocessor Monitoring

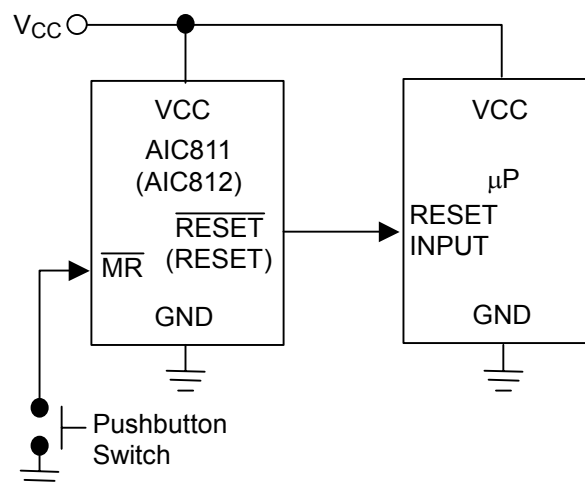
DESCRIPTION

AIC811/AIC812 are low-power microprocessor (μ P) supervisory circuits used to monitor power supplies in μ P and digital systems. They provide applications with benefits of circuit reliability and low cost by eliminating external components. AIC811/AIC812 also offer a manual reset input.

These devices perform as valid singles in applications with Vcc ranging from 6.0V down to 0.9V. The reset signal lasts for a minimum period of 140ms whenever VCC supply voltage falls below preset threshold. Both AIC811 and AIC812 were designed with a reset comparator to help identify invalid signals, which last less than 140ms. The only difference between them is that they have an active-low $\overline{\text{RESET}}$ output and active-high RESET output, respectively.

Low supply current (1 μ A) makes AIC811/AIC812 ideal for portable equipment. The devices are available in SOT-23-5 package.

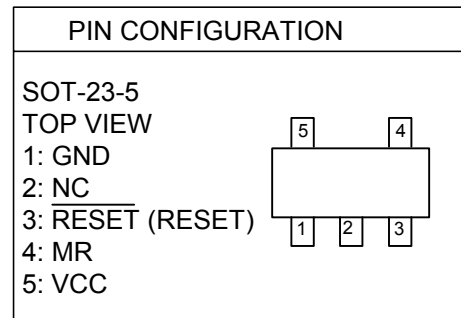
TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

AIC811-XXXXXX
AIC812-XXXXXX

- PACKING TYPE
TR: TAPE & REEL
BG: BAG
- PACKAGE TYPE
V: SOT-23-5
- C: COMMERCIAL
P: LEAD FREE COMMERCIAL
- RESET THRESHOLD VOLTAGE
23: 2.3V
26: 2.6V
29: 2.9V
31: 3.1V
40: 4.0V
44: 4.4V
46: 4.6V



(Additional voltage versions with a unit of 0.1V within the voltage range from 1.5V to 5.5V for this product line may be available on demand with prior consultation with AIC.)

Example: AIC811-31CVTR

→ 3.1V version, in SOT-23-5 Package & Tape & Reel Packing Type

AIC811-31PVTR

→ 3.1V version, in Lead Free SOT-23-5 Package & Tape & Reel Packing Type

SOT-23-5 Marking

| Part No. | Marking |
|-------------|---------|
| AIC811-23CV | BQ23 |
| AIC811-26CV | BQ26 |
| AIC811-29CV | BQ29 |
| AIC811-31CV | BQ31 |
| AIC811-40CV | BQ40 |
| AIC811-44CV | BQ44 |
| AIC811-46CV | BQ46 |

| Part No. | Marking |
|-------------|---------|
| AIC812-23CV | BR23 |
| AIC812-26CV | BR26 |
| AIC812-29CV | BR29 |
| AIC812-31CV | BR31 |
| AIC812-40CV | BR40 |
| AIC812-44CV | BR44 |
| AIC812-46CV | BR46 |

| Part No. | Marking |
|-------------|---------|
| AIC811-23PV | BQ23P |
| AIC811-26PV | BQ26P |
| AIC811-29PV | BQ29P |
| AIC811-31PV | BQ31P |
| AIC811-40PV | BQ40P |
| AIC811-44PV | BQ44P |
| AIC811-46PV | BQ46P |

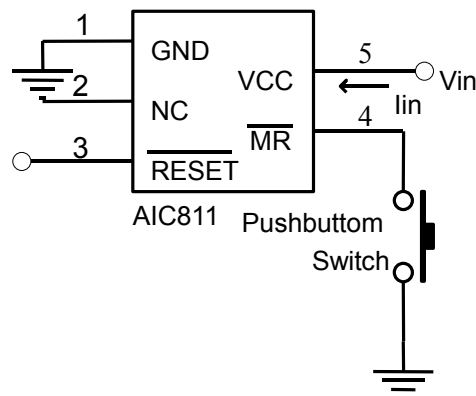
| Part No. | Marking |
|-------------|---------|
| AIC812-23PV | BR23P |
| AIC812-26PV | BR26P |
| AIC812-29PV | BR29P |
| AIC812-31PV | BR31P |
| AIC812-40PV | BR40P |
| AIC812-44PV | BR44P |
| AIC812-46PV | BR46P |

■ ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------|
| V_{CC} | -0.3V ~6.5V |
| RESET, $\overline{\text{RESET}}$ | -0.3V ~ (VCC+0.3V) |
| Input Current (V_{CC} , MR) | 20mA |
| Output Current (RESET or $\overline{\text{RESET}}$) | 20mA |
| Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) | 320mW |
| Operating Junction Temperature Range | -40°C ~ 85°C |
| Junction Temperature | 125°C |
| Storage Temperature Range | - 65°C ~ 150°C |
| Lead Temperature (Soldering) 10 sec | 260°C |

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

■ TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

 (Typical values are at $T_A=25^\circ\text{C}$, unless otherwise specified) (Note 1)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|---|----------|---|--|-------|--------------|------------------|----|
| Operating Voltage Range | V_{CC} | | 0.9 | | 6 | V | |
| Supply Current | I_{CC} | $V_{CC} = V_{TH} + 0.1V$ | | 1 | 3 | μA | |
| Reset Threshold | V_{TH} | AIC811-23 | $T_A=+25^\circ\text{C}$ | 2.265 | 2.3 | 2.335 | V |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 2.254 | | 2.346 | |
| | | AIC811-26 | $T_A=+25^\circ\text{C}$ | 2.561 | 2.6 | 2.639 | |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 2.548 | | 2.652 | |
| | | AIC811-29 | $T_A=+25^\circ\text{C}$ | 2.857 | 2.9 | 2.944 | |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 2.842 | | 2.958 | |
| | | AIC811-31 | $T_A=+25^\circ\text{C}$ | 3.054 | 3.1 | 3.147 | |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 3.038 | | 3.162 | |
| | | AIC811-40 | $T_A=+25^\circ\text{C}$ | 3.940 | 4.0 | 4.060 | |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 3.920 | | 4.080 | |
| | | AIC811-44 | $T_A=+25^\circ\text{C}$ | 4.334 | 4.4 | 4.466 | |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 4.312 | | 4.488 | |
| | | AIC811-46 | $T_A=+25^\circ\text{C}$ | 4.531 | 4.6 | 4.669 | |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 4.508 | | 4.692 | |
| V_{CC} to Reset Delay | T_{RD} | $V_{CC}=V_{TH}$ to $(V_{TH}-0.1V)$, $V_{TH}=3.1V$ | | 20 | | μS | |
| Reset Active Timeout Period | T_{RP} | $V_{CC} = V_{TH(MAX)}$ | $T_A=+25^\circ\text{C}$ | 140 | 230 | 560 | mS |
| | | | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | 100 | | 1030 | |
| $\overline{\text{MR}}$ to Reset Propagation Delay | T_{MD} | $V_{CC}=6V$ | | 0.5 | | μS | |
| $\overline{\text{MR}}$ Input Threshold | V_{IH} | | $0.7V_{CC}$ | | | V | |
| | V_{IL} | | | | $0.25V_{CC}$ | | |
| $\overline{\text{MR}}$ Pull-Up Resistance | | | 10 | 20 | 30 | $\text{K}\Omega$ | |
| $\overline{\text{RESET}}$ Output Voltage | V_{OH} | $V_{CC}=V_{TH}+0.1V, I_{SOURCE}=1\text{mA}$ | $0.8V_{CC}$ | | | V | |
| | V_{OL} | $V_{CC}=V_{TH}-0.1V, I_{SINK}=1\text{mA}$ | | | $0.2V_{CC}$ | | |
| RESET Output Voltage | V_{OH} | $V_{CC}=V_{TH}+0.1V, I_{SOURCE}=1\text{mA}$ | $0.8V_{CC}$ | | | V | |
| | V_{OL} | $V_{CC}=V_{TH}-0.1V, I_{SINK}=1\text{mA}$ | | | $0.2V_{CC}$ | | |

Note1: Specifications are production tested at $T_A=25^\circ\text{C}$. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note2: $\overline{\text{RESET}}$ output is for AIC811; RESET output is for AIC812.

TYPICAL PERFORMANCE CHARACTERISTICS

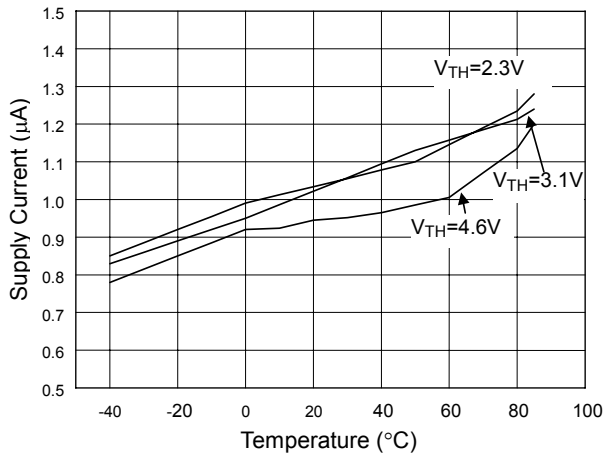


Fig 1 Supply Current vs. Temperature

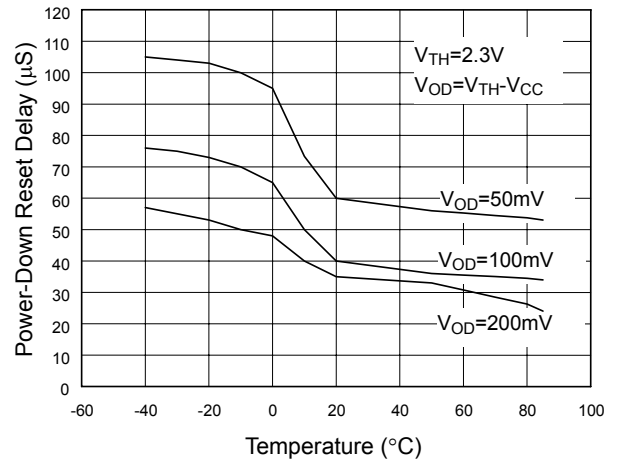


Fig 2 Power-Down Reset Delay vs. Temperature

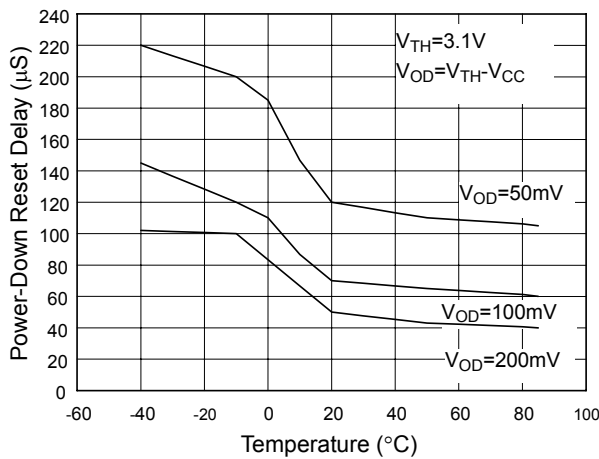


Fig 3 Power-Down Reset Delay vs. Temperature

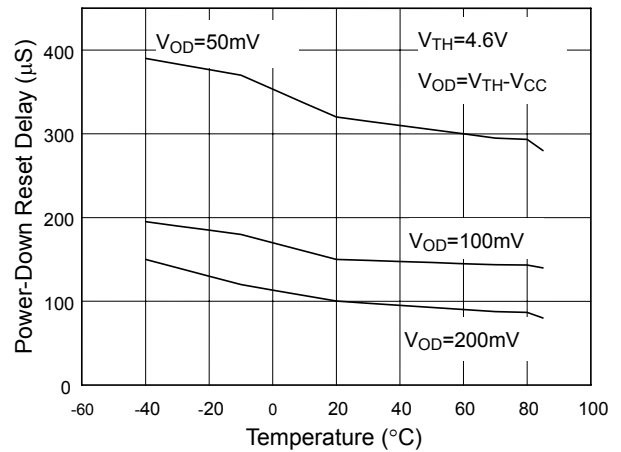


Fig 4 Power-Down Reset Delay vs. Temperature

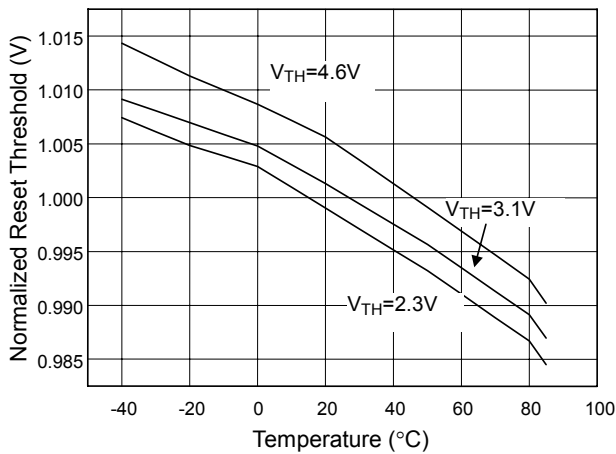


Fig 5 Normalized Reset Threshold vs. Temperature

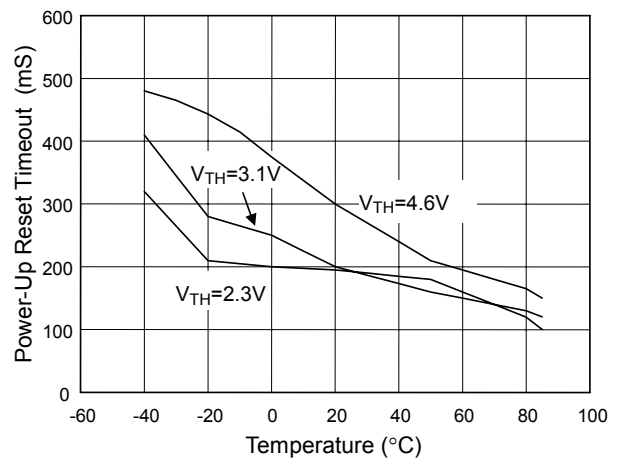
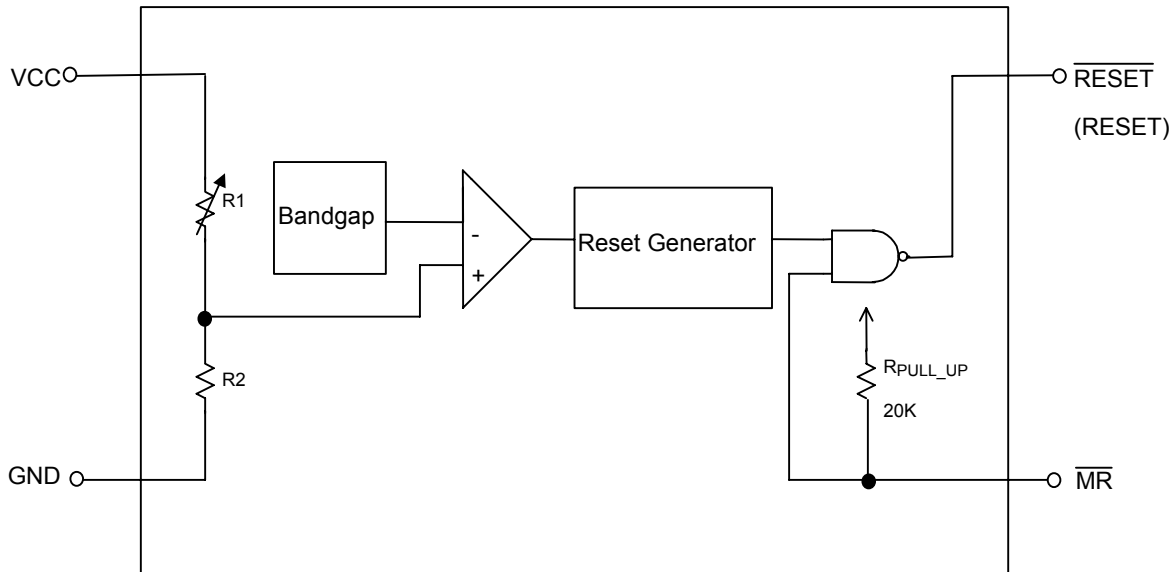


Fig 6 Power-Up Reset Timeout vs. Temperature

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

GND Pin : Ground.

$\overline{\text{RESET}}$ Pin (AIC811) : Active low output pin. $\overline{\text{RESET}}$ Output remains low while V_{cc} below reset threshold.

RESET Pin (AIC812) : Active high output pin. RESET output remains high while V_{cc} below reset threshold.

$\overline{\text{MR}}$ Pin : Logic low manual reset input. This active-low input has an internal 20k Ω pull-up resistor. It can be driven by a TTL or CMOS, or shorted to ground with a switch. Leave open when unused.

Vcc Pin : Supply voltage.

■ DETAILED DESCRIPTIONS OF TECHNICAL TERMS

RESET OUTPUT

μP will be activated at a valid reset state. These μP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ is guaranteed to be a logic low for $V_{TH} > V_{CC} > 0.9V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high.

If a brownout condition occurs (V_{CC} drops below the reset threshold), $\overline{\text{RESET}}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer is activated after V_{CC} returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

The manual reset input ($\overline{\text{MR}}$) can also initiate a reset. AIC812 has an active-high RESET output that is the inverse of AIC811's $\overline{\text{RESET}}$ output.

MANUAL RESET INPUT

Many μ P-based products require manual reset capability, allowing operators, test technicians, or external logic circuitry to initiate a reset. Logic low on $\overline{\text{MR}}$ asserts reset. Reset will remain asserted for the Reset Active Timeout Period (t_{RP}) after $\overline{\text{MR}}$ returns high. This input has an internal 20K Ω pull-up resistor, so it can be floating if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Another alternative is to connect a normal switch from $\overline{\text{MR}}$ to GND to create a manual reset function. Connecting a 0.1 μ F capacitor from $\overline{\text{MR}}$ to ground

can provide noise immunity to prevent noise caused by long cables of $\overline{\text{MR}}$ or noisy environment.

BENEFITS OF HIGHLY ACCURATE RESET THRESHOLD

AIC811/812 with specified voltage as $5\text{V}\pm 10\%$ or $3\text{V}\pm 10\%$ are ideal for systems using a $5\text{V}\pm 5\%$ or $3\text{V}\pm 5\%$ power supply. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range of the system ICs. The pre-trimmed thresholds are reducing the range over which an undesirable reset may occur.

APPLICATION INFORMATION**NEGATIVE-GOING VCC TRANSIENTS**

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, AIC811 series are relatively resistant to short-duration negative-going VCC transient.

ENSURING A VALID RESET OUTPUT DOWN TO VCC=0

When VCC falls below 0.9V, AIC811 $\overline{\text{RESET}}$ output no longer sinks current; it becomes an open circuit. In this case, high-impedance CMOS logic inputs connecting to $\overline{\text{RESET}}$ can drift to undetermined voltages. Therefore, AIC811/2 with CMOS is perfect for most applications of VCC below 0.9V. However in applications where

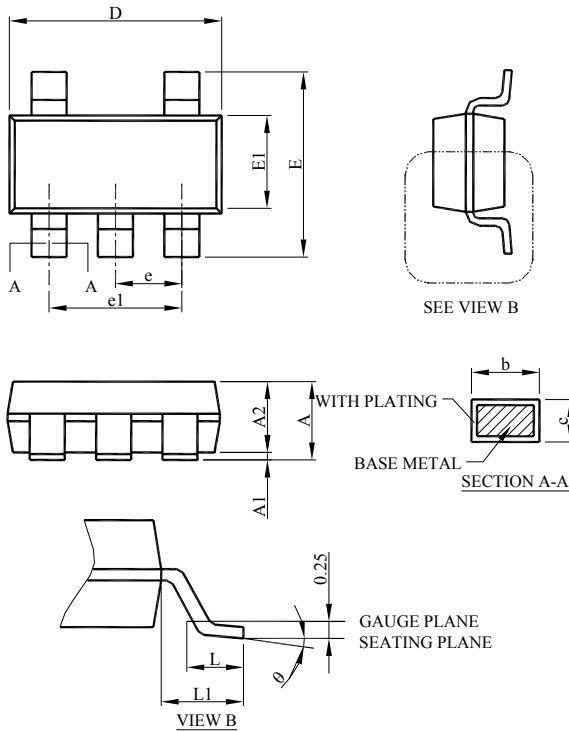
$\overline{\text{RESET}}$ must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ causes any leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low.

INTERFACING TO μ P WITH BIDIRECTIONAL RESET PINS

μ Ps with bidirectional reset pins can contend with AIC811/812 reset outputs. If AIC811 $\overline{\text{RESET}}$ output is asserted high and the μ P wants to pull it low, indeterminate logic levels may occur. To correct such cases, connect a resistor between AIC811 $\overline{\text{RESET}}$ (or AIC812 RESET) output and the μ P reset I/O. Buffer the reset output to other system components.

■ PHYSICAL DIMENSIONS (unit: mm)

● SOT-23-5



| SYMBOL | SOT-25 | |
|----------|-------------|------|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.95 | 1.45 |
| A1 | 0.05 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.30 | 0.50 |
| c | 0.08 | 0.22 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.70 |
| e | 0.95 BSC | |
| e1 | 1.90 BSC | |
| L | 0.30 | 0.60 |
| L1 | 0.60 REF | |
| θ | 0° | 8° |

Note:

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