

**GENERAL DESCRIPTION** 

mode SMPS ICs.

counterparts.

The TC35C25 family of PWM controllers are CMOS

These second generation CMOS devices employ

These controllers have separate supply pins for the

Other improved features include tighter hysteresis and

implementations of the industry standard 3525 voltage

TelCom Semiconductors' Tough BiCMOS<sup>™</sup> process for latch-up proof operation. They offer much lower power

consumption than any of their previous CMOS or bipolar

control and output sections of the circuit. This allows "boot-

strap" operation. The CMOS output stage allows the output

undervoltage start-up specifications over temperature, and

voltage to swing to within 25mV of either rail.

very low input bias current on all inputs.

## **BICMOS PWM CONTROLLERS**

#### FEATURES

- Low Power BICMOS Construction
- Low Supply Current at 20 kHz ...... 1.0mA Typ
- Latch-Up Immunity ......>500mA on Outputs
- Below Rail Input Protection .....- 5V
- Fast Rise/Fall Time ...... 50nsec @ 1000pF
- High Frequency Operation ..... Up to 1MHz
- Tri-state Sync Pin for Easy Parallel Operation
- Under Voltage Hysteresis Guaranteed
- Shutdown Pin Available
- Double-Ended
- Soft Start, With Small Cap

#### **ORDERING INFORMATION**

Part No.	Configuration	Pkg./Temperature
TC25C25EOE	Non-Inverting	16-Pin SOIC (Wide) - 40°C to +85°C
TC25C25EPE	Non-Inverting	16-Pin Plastic DIP (Narrow) $-40^{\circ}$ C to +85°C
TC35C25COE	Non-Inverting	16-Pin SOIC (Wide) 0°C to +70°C
TC35C25CPE	Non-Inverting	16-Pin Plastic DIP (Narrow) 0°C to +70°C

#### FUNCTIONAL BLOCK DIAGRAM

#### 35C25 V<sub>REF</sub> 0<sup>16</sup> 'v<sub>DD</sub> REFERENCE REGULATOR UNDER V<sub>IN</sub> 0<sup>15</sup> ா VOLTAGE GND 012 4V REF OSC OUT +61 SYNC O3 RT 06 FLIP FLOP osc с<sub>т 0</sub>5 DISCH OT Б COMP 09 PWM I ATCH IN<sup>-</sup> +6V $\cap$ IN+ **50**μA SOFT START C SHUTDOWN 010

#### **ABSOLUTE MAXIMUM RATINGS\***

Supply Voltage Maximum Chip Temperature Storage Temperature	150°C
Lead Temperature (10 sec)	
Package Thermal Resistance	
PDIP R <sub>0J-A</sub>	125°C/W
PDIP R <sub>0J-C</sub>	
SOIC R <sub>0J-A</sub>	
SOIC R <sub>0J-A</sub>	75°C/W

#### **Operating Temperature**

-	25C2x	$\dots - 40^{\circ}C \le T_A \le +85^{\circ}C$
	35C2x	$\dots 0^{\circ}C \le T_{\Delta} \le +70^{\circ}C$

\*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for –  $40^{\circ}C < T_A < 10^{\circ}$ +85°C for the TC25C25Exx; and 0°C <T\_A < +70°C for the TC35C25Cxx;  $V_{IN}$  and  $V_{DD}$  = 16V;  $R_T$  = 3.7k $\Omega$ ;  $C_T$  = 1000pF; RD = 760 $\Omega$ .

Parameter	Test Conditions	Min	Тур	Max	Units
Reference Section			· ·		
Output Voltage	$T_{\rm J} = 25^{\circ} {\rm C}, \ {\rm I}_{\rm O} = 1 {\rm mA}$	3.9	4	4.1	V
Line Regulation	V <sub>IN</sub> = 8V to 18V	_	±4	±10	mV
Load Regulation	I <sub>I</sub> = 1mA to mA	_	±4	±15	mV
Temp Coefficient	Note 1	_	±0.01	±0.4	mV/°C
V <sub>REF</sub>	Worst Case	3.85	4	4.15	V
Long Term Drift	T <sub>J</sub> = 25°C, (Note 1)	_	±50	_	mV/1000Hrs
Short Circuit	V <sub>REF</sub> to GND	20	40	70	mA
Output Noise	$T_J = 25^{\circ}C$ , 10 Hz $\leq f \geq$ 10 kHz, (Note 1)	_	21	_	μV(rms)
Oscillator Section					·
Initial Accuracy	T <sub>J</sub> = 25°C, at 97 kHz		±2	±3	%
Voltage Coefficient	$V_{IN} = 8V$ to $18V$	_	±0.01	±0.1	%/V
Temp Coefficient	Note 1	_	±0.025	±0.06	%/°C
OSC Ramp Amplitude		2.9	3.2	3.4	V
Reset Switch R <sub>DS (ON)</sub>	$T_J = 25^{\circ}C$	30	50	60	Ω
Clock Amplitude	$f_{osc} = 100 \text{kHz}, R_L = 1 M\Omega$ , (Note 1)	4.9	5.5	6.7	V
Clock Min Width	$T_J = 25$ °C, $R_D = 0\Omega$ , (Note 1) C <sub>T</sub> = 100pF, $R_T = 1\Omega$	_	170	200	nsec
Sync Threshold	$R_T$ Pin Tied to $V_{REF}$ , $C_T$ Pin at GND	1.8	2.2	2.8	V
Sync Input Current	Sync Voltage = $4V$ , $V(R_T) = 4V$	_	—	±1	μΑ
Min Sync Pulse Width	T <sub>J</sub> = 25°C, Sync Amplitude = 5V, (Note 1)	_	130	175	nsec
Max OSC Freq	$R_T = 1\Omega, C_T = 100 pF, R_D = 0\Omega, (Note 1)$	1.0	—	_	MHz
Error Amplifier Section (	V <sub>CM</sub> = 2.5V)				
Input Offset Voltage		_	±5	±15	mV
Input Bias Current	$T_J = 25^{\circ}C$	_	±50	±200	рА
Input Offset Current	$T_J = 25^{\circ}C$	_	±25	±100	рА
DC Open Loop Gain	$R_L = 100k\Omega$	70	85	_	dB
Gain Bandwidth Product	Note 1	0.7	0.9	1.2	MHz
Output Low Level	$R_L = 100 k\Omega$ (N Channel)	_	10	20	mV
Output High Level	$R_L = 100 k\Omega (NPN)$	4.9	5.4	5.9	V
CMRR	V <sub>CM</sub> = 0.5 to 4.7V	60	75	_	dB



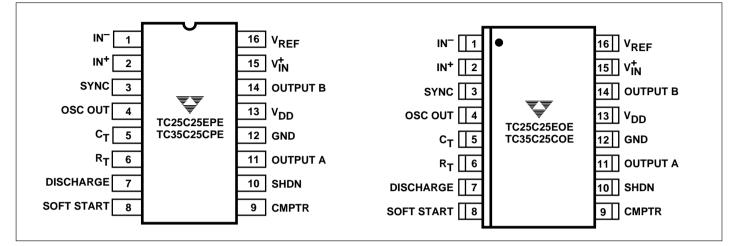
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for – 40°C < T<sub>A</sub> < +85°C for the TC25C25Exx; and 0°C <T<sub>A</sub> < +70°C for the TC35C25Cxx;  $V_{IN}$  and  $V_{DD} = 16V$ ;  $R_T = 3.7k\Omega$ ;  $C_T = 1000 \text{ pF}$ ;  $RD = 760 \Omega$ .

Parameter	Test Conditions	Min	Тур	Max	Units
Supply Voltage Rejection	V <sub>IN</sub> = 8V to 18V	90	120	_	dB
Slew Rate	$C_{LOAD} = 50 pF, ACL = 1$ V(EA+) = 1V to 3V Pulse, (Note 1)	_	1	_	V/µsec
Threshold Hysteresis		0.6	0.8	1	V
Total Standby Current		I			1
Supply Current			1.2	2.5	mA
Start-Up Current			250	350	μΑ
PWM Comparator					
Min. Duty Cycle	Note 1, T <sub>J</sub> = 25°C	_	_	0	%
Max Duty Cycle	T <sub>J</sub> = 25°C, f <sub>OSC</sub> = 100kHz, (Note 1)	45	49		%
Input Threshold	$V(C_{T}) = 0.6V$	0.5	0.6	0.7	V
Input Threshold	$V(C_{T}) = 3.6V$	3.4	3.6	3.7	V
Input Bias Current	Note 1, T <sub>J</sub> = 25°C	_	_	±1	μΑ
Soft Start Section				1	
Soft Start Current	V <sub>SHUTDOWN</sub> = 0V	30	46	75	μΑ
Soft Start Voltage	V <sub>SHUTDOWN</sub> = 3V	—	30	100	mV
Shutdown Input Current	V <sub>SHUTDOWN</sub> = 3V	—	±1	±100	nA
Min Shutdown Pulse Width	V <sub>SHUTDOWN</sub> = 5V, (Note 1)	—	20	40	nsec
Shutdown Delay	V <sub>SHUTDOWN</sub> = 5V, (Note 1)	130	140	220	nsec
Shutdown Threshold		1.5	2.4	3	V
Output Drivers (each output)					
Output Low Level RDS (ON)	I <sub>SINK</sub> = 20mA	—	13	25	Ω
Output High Level RDS (ON)	I <sub>SOURCE</sub> = 20mA	—	20	35	Ω
Rise Time	$C_L = 1_{nF}$ , (Note 1)	—	55	80	nsec
Fall Time	$C_L = 1_{nF}$ , (Note 1)	—	40	65	nsec
Power Supply					
Supply Current	f <sub>OSC</sub> = 100kHz	_	2	3	mA
UV Lockout Threshold		6.45	7	7.3	V
UV Lockout Hysteresis		1.7	2.2	2.5	V
Start-up Current			75	200	μΑ

NOTE: 1. Not Tested.

TelCom Semiconductor reserves the right to make changes in the circuitry or specifications detailed in this manual at any time without notice. Minimums and maximums are guaranteed. All other specifications are intended as guidelines only. TelCom Semiconductor assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

#### PIN CONFIGURATION (DIP AND SOIC)



#### **PIN DESCRIPTION**

Pin No.	Symbol	Description	
1	IN <sup>-</sup>	Error Amplifier inverting input for output voltage reference input and amplifier gain set.	
2	IN <sup>+</sup>	Error Amplifier, non-inverting input for output voltage feedback to regulate voltage.	
3	SYNC	Input pin for PWM controller oscillator synchronization of two or more controllers from an external clock output or from another PWM controller oscillator output.	
4	OSC OUT	Pin for output of the internal oscillator. This signal can be used as a master oscillator to sync other oscillators to run at the same timing period.	
5	CT	Pin is the capacitor timing input to set oscillator frequency in conjunction with pin 6 $R_T$ timing resistor.	
6	R <sub>T</sub>	Pin for timing resistor input to set oscillator frequency by setting the charge current into capacitor $C_T$ of pin 5.	
7	DISCHARGE	Pin for discharging the timing capacitor, C <sub>T</sub> of pin 5. During discharging time period, PWM controller output is disabled. This is called dead time. With a resistor between pin 7 and pin 5 the dead time can be controlled.	
8	SOFT START	Pin for soft starting the power supply. A capacitor from this pin to GND pin 12 will limit duty cycle till capacitor is charged above error amplifier output.	
9	CMPTR	Pin for compensation of the feedback loop response.	
10	SHDN	Pin for terminating both outputs of pins 11 and 14. This will shutdown the power supply outputs. A positive input with shutdown threshold of 2.4V is required for shutdown.	
11	OUTPUT A	Pin for output drive of phase A to drive push pull transistor A.	
12	GND	Pin for ground return for all inputs and output signals.	
13	V <sub>DD</sub>	Pin for power supply input to operate the output drivers A and B.	
14	OUTPUT B	Pin for output drive of phase B to drive push pull transistor B.	
15	V <sup>+</sup> <sub>IN</sub>	Pin for voltage bias supply input for all PWM controller functions except output drive circuits.	
16	V <sub>REF</sub>	Pin is the reference supply output voltage of 4.0 volts that may be used for any voltage reference purposes such as a reference to control output voltage.	

#### **OUTPUT SECTION**

The output stage of the TC35C25 is comprised of two pairs of complimentary CMOS drivers operating in a pushpull mode. Each output is capable of sinking or sourcing nearly 500mA of peak current. They are also capable of absorbing just as much "kick-back" current without latching.

#### SOFT START

A soft restart recovery rate may be selected by placing a capacitor from SOFT START (pin 8) to ground. The calculation for the recovery timing is approximately 60 msec/  $\mu F.$ 

SOFT START will mediate the start-up from under voltage recovery, power-on, or SHUTDOWN.

#### SHUTDOWN

There is a minimum delay, non-latching shutdown feature on the TC35C25 PWM controller. Both outputs may be turned off by applying a positive voltage to SHUTDOWN (pin 10). Typical shutdown threshold is 2.4V. Returning the pin back to ground will reinitialize the soft start cycle.

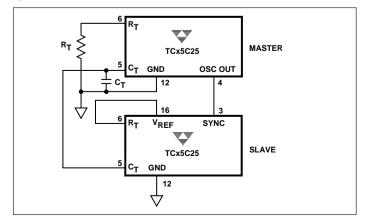
#### **OSCILLATOR SECTION**

A tri-state feature has been added to accommodate systems which require multiple controllers to be run in a "master/slave" configuration. The timing resistor pin ( $R_T$ , pin 6) may be tied to  $V_{REF}$  to place the sync pin (SYNC, pin 3) in a high impedance state. This will allow the chip to be clocked from an external source.

The sync output (OSC OUT, pin 4) of the TC35C25 can drive several sync inputs configured in this manner.

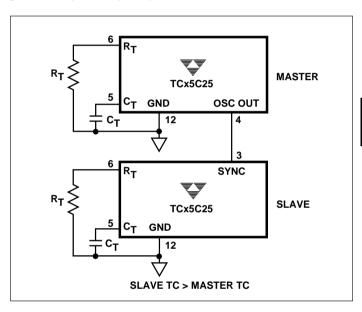
#### **OSCILLATOR SYNCHRONIZATION**

Synchronization of two TC35C25's can be done by making one PWM Controller as the master oscillator to synchronize the slave as follows:

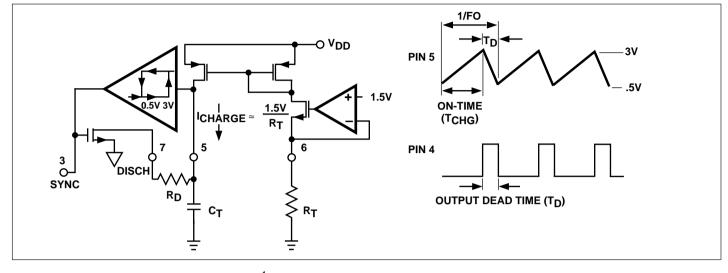


## OSCILLATOR SYNCHRONIZATION WITH SEPARATE RC TIMER

Synchronization can also be done by having a separate RC timing circuit on the slave oscillator that is slightly lower frequency than the master oscillator. The sync input will not be in a high impedance state so the number of slave oscillators is limited. This method of synchronization is useful when slave oscillator is located in a different location. When a separate RC timer is used in the slave controller, ground loop noise pickup in the oscillator is minimized.



#### OSCILLATOR FREQUENCY AND OUTPUT DEAD TIME



The oscillator frequency (F<sub>O</sub>) =  $\frac{1}{T_{CHG} + T_D}$ 

 $T_{CHG}$  is the charging duration of  $C_T$ . One of the PWM Controller output drivers is ON during charging of  $C_T$ .  $T_D$  is the output dead time when both of the output drivers are inactive. Resistor ( $R_T$ ) sets the Capacitor ( $C_T$ ) charging current.

To choose an oscillator frequency ( $F_O$ ), first select the period of dead time ( $T_D$ ) required. Calculate the capacitor charge time ( $T_{CHG}$ ).

$$T_{CHG} = \frac{1 - F_O \times T_C}{F_O}$$

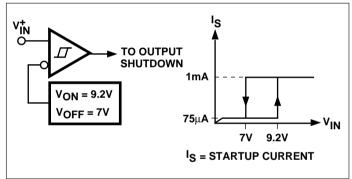
Select a capacitor in the range of 100 pF to 1000 pF for C<sub>T</sub>. See graph in Typical Characteristic Curve. Calculate capacitor charging current ( $I_{CHG}$ ).

$$I_{CHG} = \frac{2.5 \times C_{T}}{T_{CHG}}$$

 $C_{\mathsf{T}}$  in Farads,  $\mathsf{T}_{\mathsf{CHG}}$  in seconds,  $\mathsf{I}_{\mathsf{CHG}}$  in amperes, and  $\mathsf{R}_{\mathsf{T}}$  in ohms.

$$R_{T} = \frac{1.5}{I_{CHG}}$$

The resistor (R<sub>D</sub>) controls the period of dead time (T<sub>D</sub>). During dead time this resistor (R<sub>D</sub>) current is the sum of the C<sub>T</sub> discharge current and the I<sub>CHG</sub> current. The value for R<sub>D</sub> can range from >1 $\Omega$  to <900 $\Omega$ . Dead time increases when R<sub>D</sub> is increased. See graph in Typical Characteristic Curve for dead time resistor value.

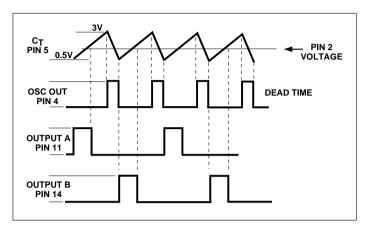


#### UNDERVOLTAGE LOCKOUT SECTION

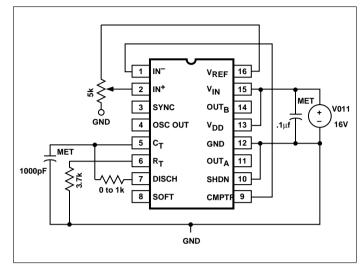
The typical turn on threshold is 9.2V for operation of this family of PWM Controllers. When supply voltage at pin 15 drops below 7V, after normal operation above 9.2V, lockout occurs and both output drives to pin 11 and 14 are terminated.

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# BENCH TEST OPERATIONAL SIMULATION WAVEFORMS



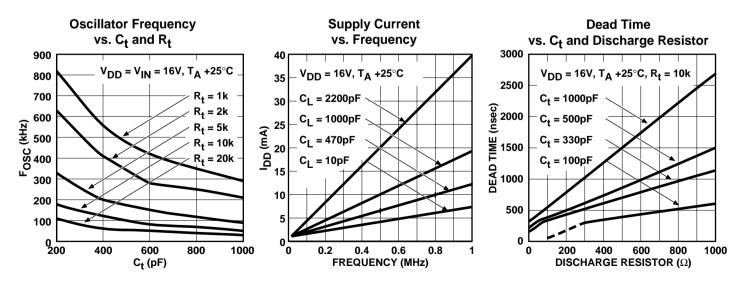
The 5k potentiometer sets a reference voltage at pin 2. When ramp voltage of pin 5 reaches this reference voltage, output drive pulse is active ON. Varying the discharge resistor will vary the dead time. Increasing the discharge resistor will effect an increase in the dead time.



#### **REPLACING BIPOLAR VERSIONS WITH CMOS**

Although the pin-out and functions are the same for both the Bipolar and CMOS versions, there are several differences that need to be taken into account. The reference voltage on the TC35C25 is 4V instead of 5V and the oscillator ramp is 3V, not 4V. The R<sub>T</sub> and C<sub>T</sub> values are different for any particular frequency and dead-time requirement.

The most important difference is that the absolute maximum rating of the V<sub>DD</sub> and V<sub>IN</sub> voltages for the TC35C25 is 18V, whereas the UC3525 is 40V.



#### **TYPICAL CHARACTERISTICS**

TELCOM SEMICONDUCTOR, INC.