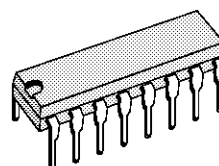


LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS

DESCRIPTION

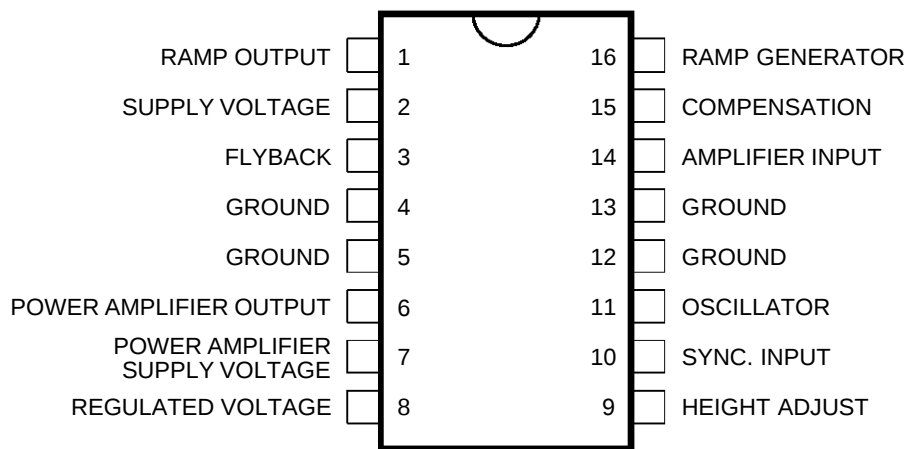
The TDA 1170D is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise makes this device particularly suitable for use in monitors.** The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.



DIP16
(Plastic Package)

ORDER CODE : TDA1170D

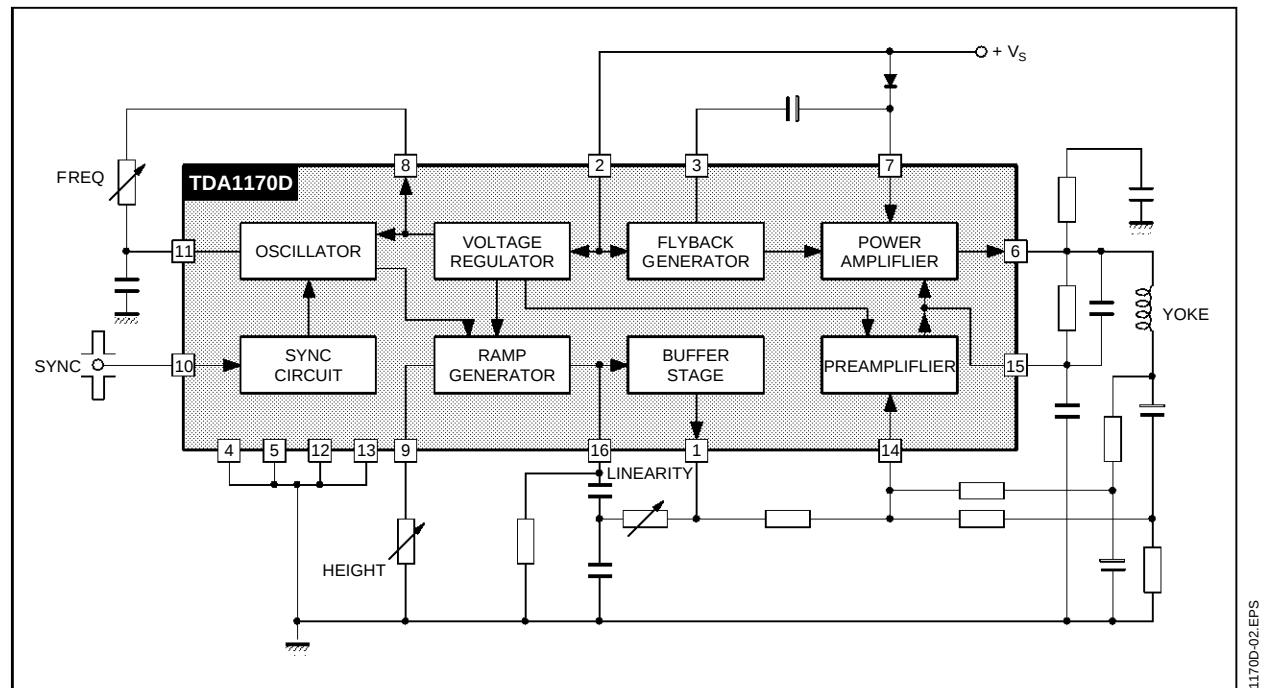
PIN CONNECTIONS



1170D-01.EPS

TDA1170D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_6, V_7	Flyback Peak Voltage	60	V
V_{14}	Power Amplifier Input Voltage	+ 10 - 0.5	V V
I_o	Output Peak Current (non repetitive) at $t = 2\text{msec}$	2	A
I_o	Output Peak Current at $f = 50\text{Hz}$ $t \leq 10\mu\text{sec}$	2.5	A
I_o	Output Peak Current at $f = 50\text{Hz}$ $t > 10\mu\text{sec}$	1.5	A
I_3	Pin 3 DC Current at $V_6 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for $f = 50\text{Hz}$, $t_{fly} \leq 1.5\text{msec}$	1.8	A
I_{10}	Pin 10 Current	± 20	mA
P_{tot}	Power Dissipation : at $T_{tab} = 90^\circ\text{C}$ at $T_{amb} = 70^\circ\text{C}$ (free air)	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	- 40 to 150	$^\circ\text{C}$

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal Resistance Junction-pins	14	$^\circ\text{C/W}$
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	80	$^\circ\text{C/W}^*$

* Obtained with pins 4, 5, 12, 13 soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS(refer to the test circuits, $V_S = 35V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)**DC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_7	Pin 7 Quiescent Current	$I_6 = 0$		8	17	mA	1b
$-I_{11}$	Oscillator Bias Current	$V_{11} = 1V$		0.1	1	μA	1a
$-I_{14}$	Amplifier Input Bias Current	$V_{14} = 1V$		1	10	μA	1b
$-I_{16}$	Ramp Generator Bias Current	$V_{16} = 0$		0.02	0.3	μA	1a
$-I_{16}$	Ramp Generator Current	$I_9 = 20\mu A$, $V_{16} = 0$	18.5	20	21.5	μA	1b
$\frac{\Delta I_{16}}{I_{16}}$	Ramp Generator Non-linearity	$\Delta V_{16} = 0$ to $12V$, $I_9 = 20\mu A$		0.2	1	%	1b
V_S	Supply Voltage Range		10		35	V	—
V_1	Pin 1 Saturation Voltage to Ground	$I_1 = 1mA$		1	1.4	V	—
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 10mA$		300	450	mV	1a
V_6	Quiescent Output Voltage	$V_S = 10V$ $R1 = 1k\Omega$, $R2 = 1k\Omega$	4.1	4.4	4.75	V	1a
		$V_S = 35V$ $R1 = 3k\Omega$, $R2 = 1k\Omega$	8.3	8.8	9.45	V	1a
V_{6L}	Output Saturation Voltage to Ground	$-I_6 = 0.1A$		0.9	1.2	V	1c
		$-I_6 = 0.8A$		1.9	2.3	V	1c
V_{6H}	Output Saturation Voltage to Supply	$I_6 = 0.1A$		1.4	2.1	V	1d
		$I_6 = 0.8A$		2.8	3.2	V	1d
V_8	Regulated Voltage at Pin 8		6.1	6.5	6.9	V	1b
V_9	Regulated Voltage at Pin 9	$I_9 = 20\mu A$	6.2	6.6	7	V	1b
$\frac{\Delta V_8}{\Delta V_S}, \frac{\Delta V_9}{\Delta V_S}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_S = 10$ to $35V$		1		mV/V	1b
V_{14}	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	—
R_{10}	Pin 10 Input Resistance	$V_{10} \leq 0.4V$	1			$M\Omega$	1a

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TDA1170D

Figure 1 : DC Test Circuit

Figure 1a

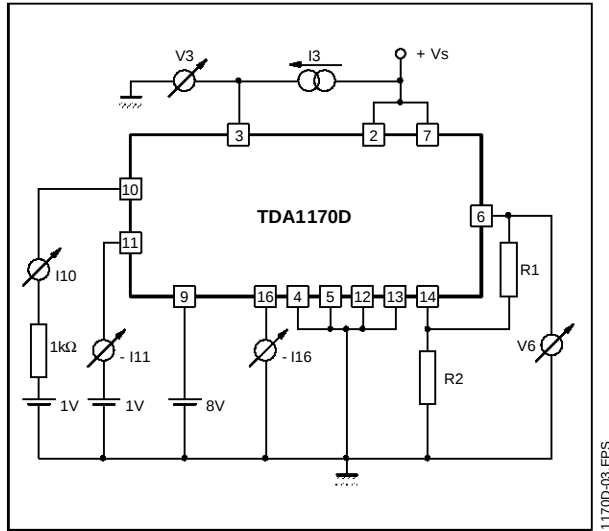


Figure 1b

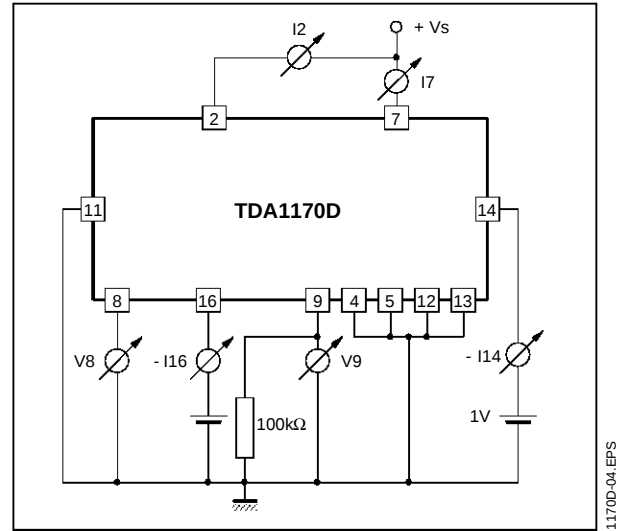


Figure 1c

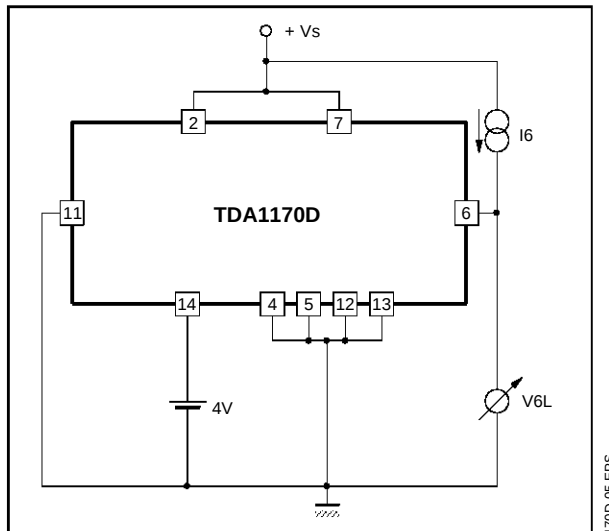
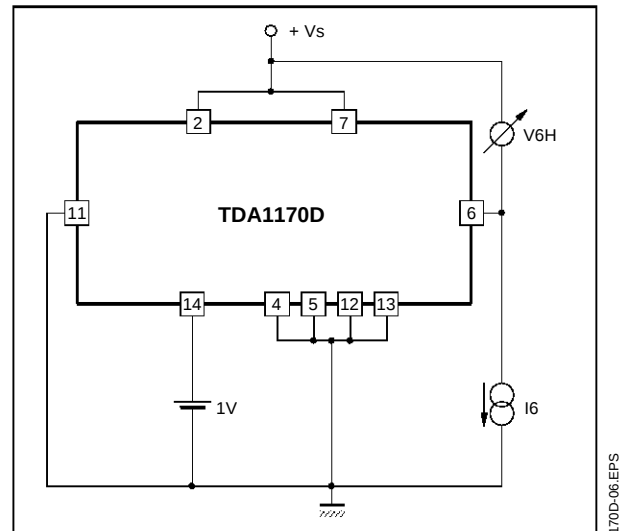


Figure 1d

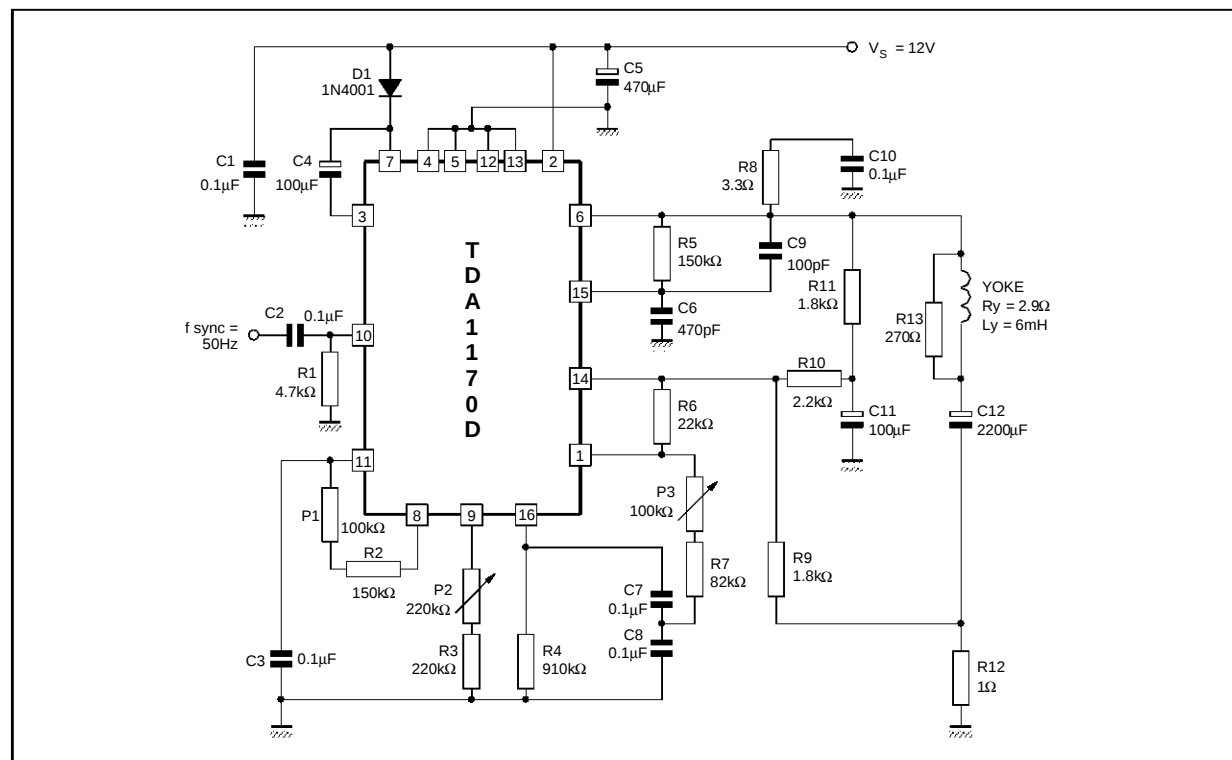


AC CHARACTERISTICS

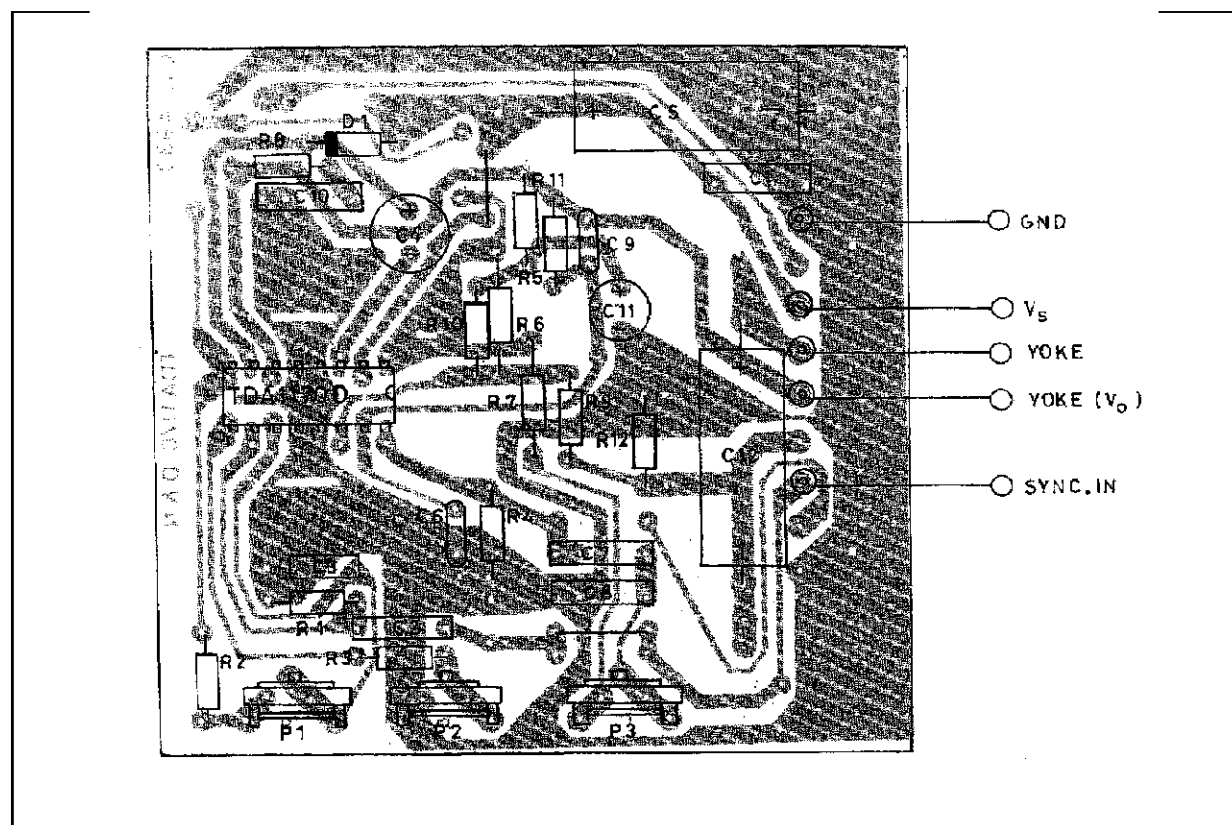
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _s	Supply Current	I _y = 1App		140		mA
I ₁₀	Sync. Input Current (positive or negative)		500			μA
V ₆	Flyback Voltage	I _y = 1App		45		V
t _{fly}	Flyback Time	I _y = App		0.7		ms
V _{ON}	Peak to Peak Output Noise	Pin 11 Connected to GND			40	mV _{PP}
f ₀	Free Running Frequency	(P1 = R1) = 260kΩ, C2 = 0.1μF (P1 = R1) = 300kΩ, C2 = 0.1μF		48.5 42.2		Hz Hz
Δf	Synchronization Range	I ₈ = 0.5mA	14			Hz
$\frac{\Delta f}{\Delta V_S}$	Frequency Drift with Supply Voltage	V _s = 10 to 35V		0.005		Hz/V
$\frac{\Delta f}{\Delta T_{pins}}$	Frequency Drift vs. Pins 4, 5, 12 and 13 Temp.	T _{pins} = 40 to 120°C		0.01		Hz/°C

1170D-04.TBL

170D-07.EPS

Figure 3 : Typical Application Circuit for Small Screen B/W TV SET ($R_y = 2.9\Omega$, $L_y = 6mH$, $I_y = 1.1App$)

1170D-08.EPS

Figure 4 : P.C. Board and Components Layout of the Circuit of Fig. 3 (1 : 1 scale)

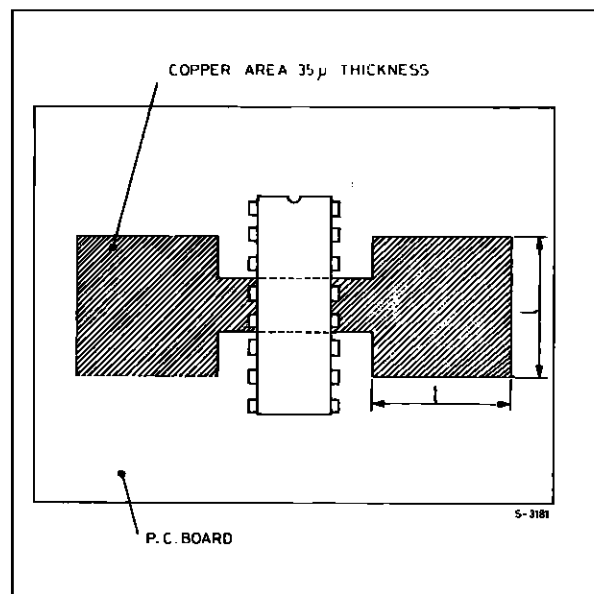
1170D-09.TIF

MOUNTING INSTRUCTION

The $R_{th\ j-amb}$ of the TDA 1170D can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 5) or to an external heatsink (fig. 6).

The diagram of figure 7 shows the maximum dissippable power P_{tot} and the $R_{th\ j-amb}$ as a function of

Figure 5 : Example of P.C. Board Copper Area which is Used as Heatsink



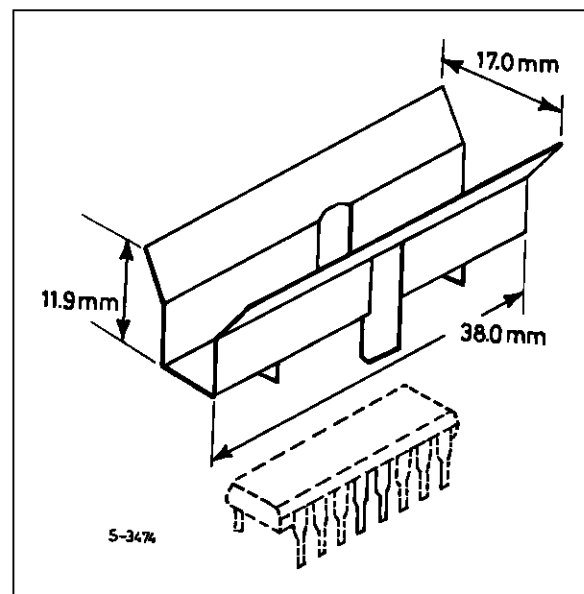
1170D-10.EPS

the side "l" of two equal square copper areas having a thickness of $35\ \mu$ (1.4 mils).

During soldering the pins temperature must not exceed $260\ ^\circ\text{C}$ and the soldering time must not be longer than 12 seconds.

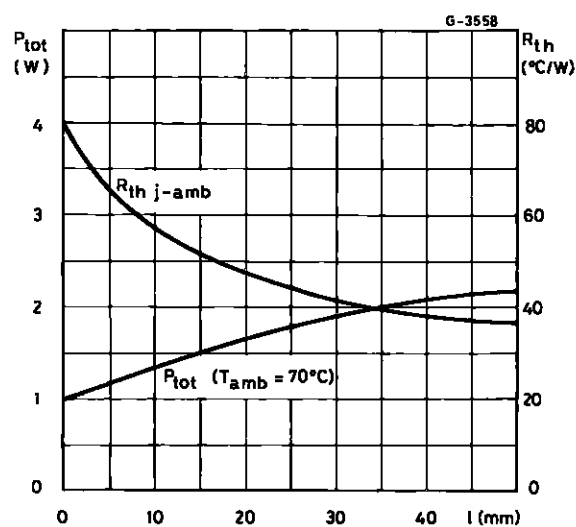
The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 6 : External Heatsink Mounting Example



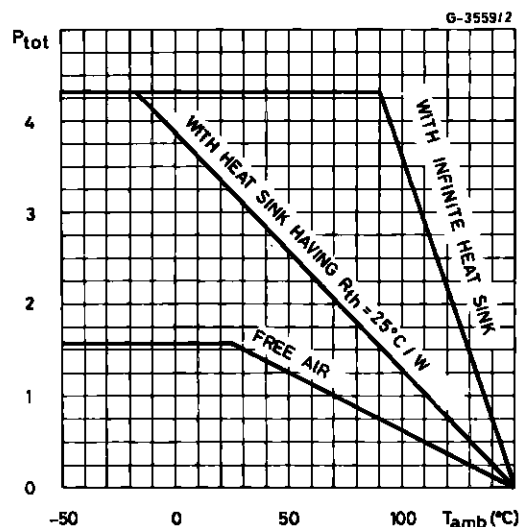
1170D-11.EPS

Figure 7 : Maximum Dissippable Power and Junction-Ambient Thermal Resistance versus Side "l"



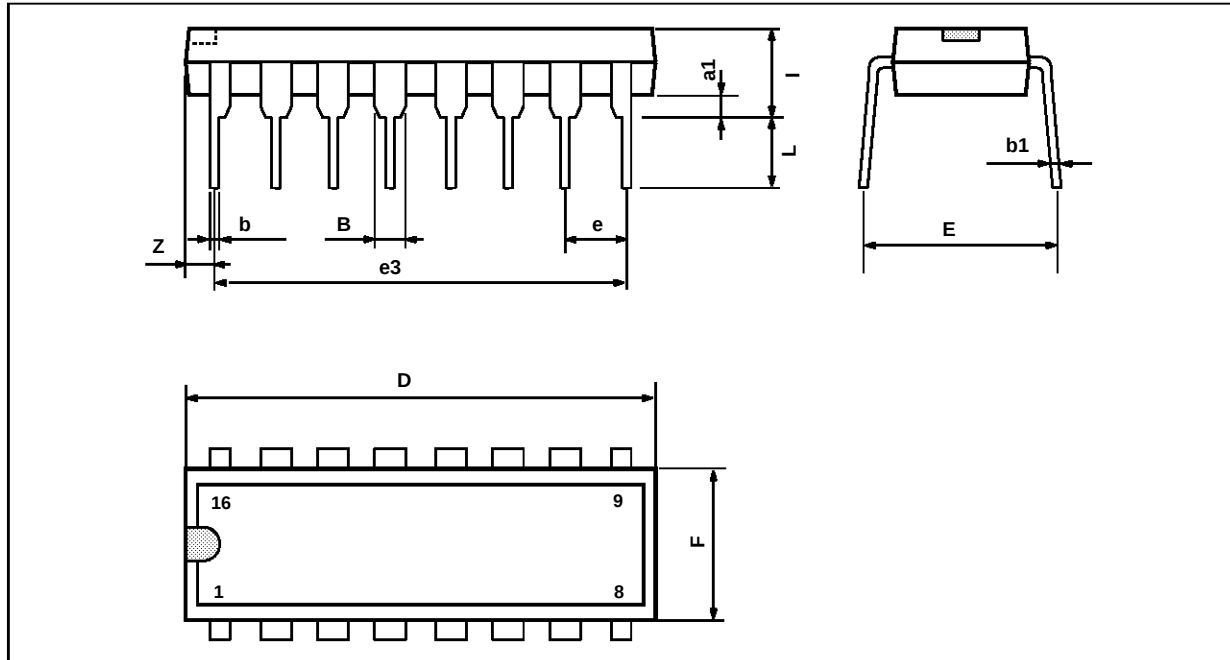
1170D-12.EPS

Figure 8 : Maximum Allowable Power Dissipation versus Ambient Temperature



1170D-13.EPS

PACKAGE MECHANICAL DATA **16 PINS - PLASTIC PACKAGE**



PM-DIP16.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

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