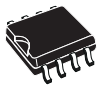
STSR2

FORWARD SYNCHRONOUS RECTIFIERS SMART DRIVER

- SUPPLY VOLTAGE RANGE: 4.5V TO 5.5V
- TYPICAL PEAK OUTPUT CURRENT: SOURCE -2A, SINK 3.5A
- OPERATING FREQUENCY: 20 TO 750 KHZ
- SMART TURN-OFF ANTICIPATION TIMING
- OPERATION INDEPENDENT FROM THE FORWARD MAGNETIC RESET TECHNIQUE
- POSSIBILITY TO OPERATE IN DISCONTINUOUS MODE



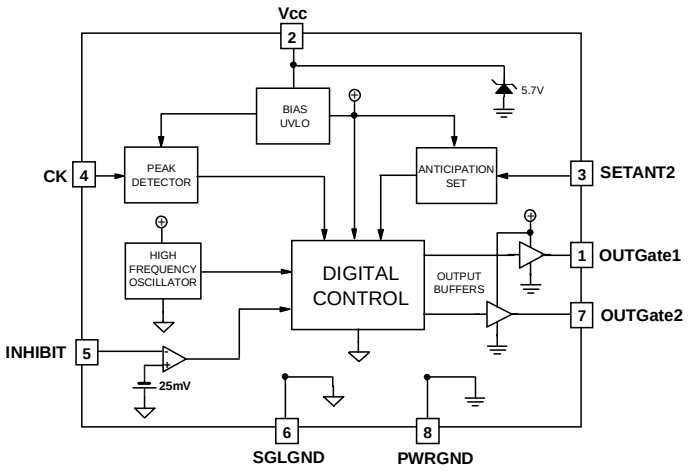
SO-8

DESCRIPTION

STSR2 Smart Driver IC provides two complementary high current outputs to drive Power Mosfets. The IC is dedicated to properly drive secondary Synchronous Rectifiers in medium power, low output voltage, high efficiency Forward Converters. From a synchronizing clock input, STSR2 generates two driving signals with the self-setting of dead time between complementary pulses. The IC operation prevents secondary side shoot-through conditions providing proper timing at the outputs turn-off transition. This smart function operates through a fast cycle-after-cycle control logic mechanism based on an internal high frequency oscillator, synchronized by the clock signal. A fixed anticipation in turning-off the OUT_{GATE1} with respect to the clock signal transition is provided, while the anticipation in turning off the OUT_{GATE2} can be set through external components. The adopted transitions revelation mechanism makes circuit operation independent by the forward magnetic reset technique used, avoiding most of the common problems inherent in self-driven synchronous rectifiers. A special Inhibit function allows the shut-off of OUT_{GATE2}. This feature makes discontinuous conduction mode possible and prevents the freewheeling mosfet from sinking current from the output.

STSR2 automatically turns off the outputs when duty-cycle is lower than 13%, while STSR2M works even at very low duty-cycle values.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Input Voltage		-0.3 to 6	V
$V_{OUTGATE}$	Max Gate Drive Output Voltage		-0.3 to V_{CC}	V
$V_{INHIBIT}$	Max INHIBIT Voltage (*)		-0.6 to V_{CC}	V
V_{CK}	Clock Input Voltage Range (*)		-0.3 to V_{CC}	V
I_{LX}	Switching Peak Current		2	A
P_{TOT}	Continuous Power Dissipation at T_A=105°C without heatsink		270	mW
ESD	Human Body Model	Pins 1,,2, 4, 5, 6, 7, 8	±1	KV
		Pin 3	±0.9	KV
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_{op}	Operating Junction Temperature Range		-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) A higher positive voltage level can be applied to the pin with a resistor which limits the current flowing into the pin to 10mA maximum

THERMAL DATA

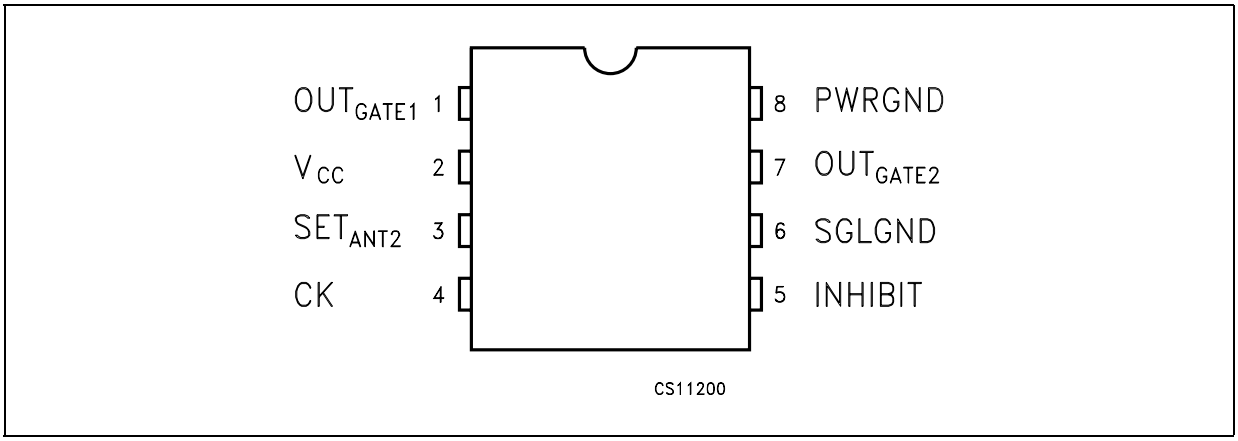
Symbol	Parameter	SO-8	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-case	40	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (*)	160	°C/W

(*) This value is referred to one layer pcb board with minimum copper connections for the leads. a minimum value of 120 °C/W can be obtained improving thermal conductivity of the board

ORDERING CODES

TYPE	SO-8	SO-8 (T&R)
STSR2	STSR2CD	STSR2CD-TR
STSR2M	STSR2MCD	STSR2MCD-TR

CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

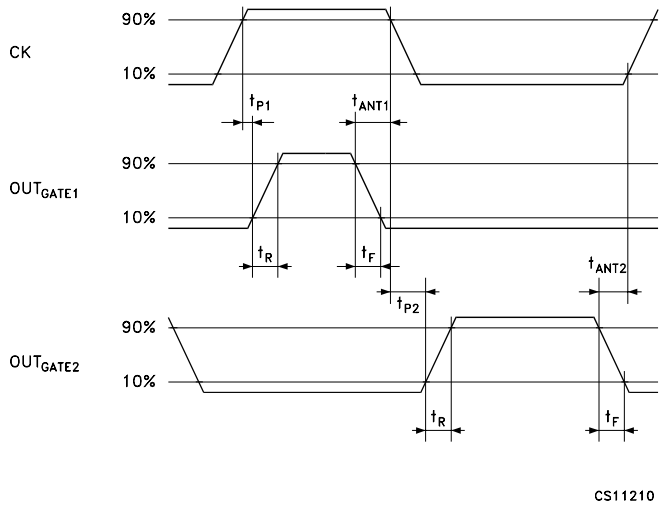
Pin N°	Symbol	Name and Function
1	OUT_{GATE1}	Gate Drive signal for Rectifier MOSFET. Anticipation (t_{ANT1}) in turning off OUT_{GATE1} is provided when the clock input goes to low level.
2	V_{CC}	The supply voltage range from 4.5V to 5.5V allows applications with logic gate threshold mosfets. UVLO feature guarantees proper start-up while it avoids undesirable driving during eventual dropping of the supply voltage.
3	SET_{ANT2}	The voltage on this pin sets the anticipation (t_{ANT1}) in turning off the OUT_{GATE2}. It is possible to choose among three different anticipation times by discrete partitioning of the supply voltage.
4	CK	This input provides synchronization for IC's operations, being the transitions between the two output conditions based on a positive threshold, equal for the two slopes. A smart internal control logic mechanism using a 15MHz internal oscillator generates proper anticipation timing at the turn-off of each output. This feature allows safe turn-off of Synchronous Rectifiers avoiding any eventual shoot-through situation on secondary side at both transitions. Smart clock revelation mechanism makes these operations independent by false triggering pulses generated in light load conditions and by particular demagnetization techniques.Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
5	INHIBIT	This input enables OUT_{GATE2} to work when its voltage is lower than the negative threshold voltage ($V_{INHIBIT}<V_H$). If $V_{INHIBIT}>V_H$ the OUT_{GATE2} will be high for a minimum conduction time ($t_{ON(GATE2)}$). In typical forward converter application, it is possible to turn off the freewheeling MOSFET when the current through it tends to reverse, allowing discontinuous conduction mode and providing protection to the converter from eventual sinking current from the load.Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
6	SGLGND	Reference for all the control logic signals. This pin is completely separated from the PWRGND to prevent eventual disturbances to affect the control logic.
7	OUT_{GATE2}	Gate Drive signal for Freewheeling MOSFET. Anticipation [t_{ANT2}] in turning off OUT_{GATE2} is provided when the clock input goes to high level.
8	PWRGND	Reference for power signals, this pin carries the full peak currents for the two outputs.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, CK= 250kHz, $V_{INHIBIT}$ =-200mV, T_J =-40 to 125°C, unless otherwise specified.)

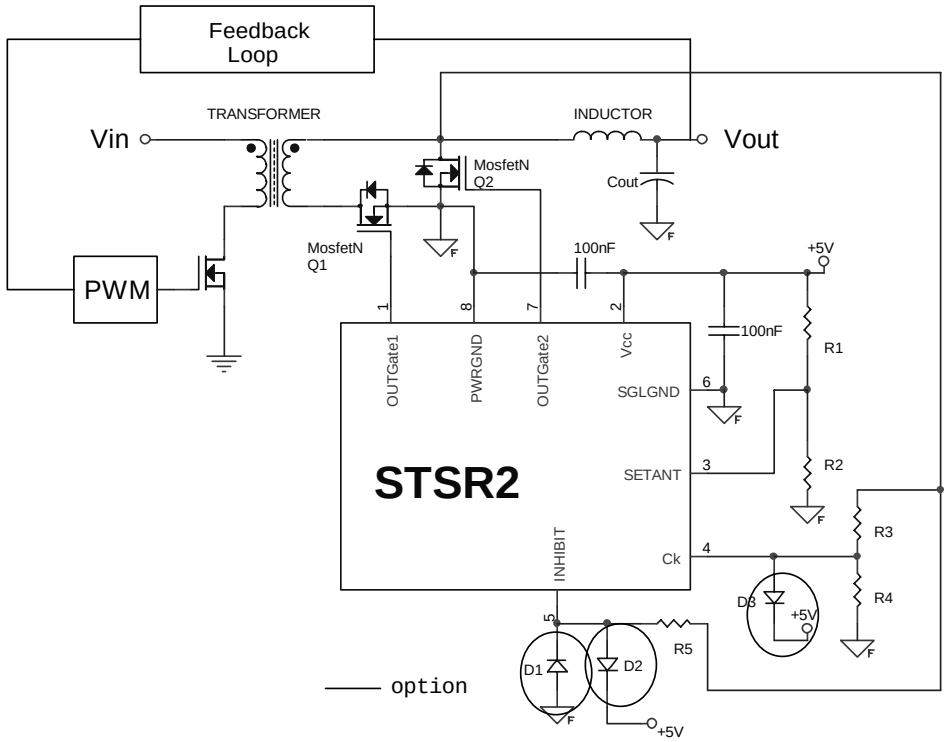
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT AND UNDER VOLTAGE LOCK OUT						
V_{CCON}	Start Threshold			3.8	4	V
V_{CCOFF}	Turn OFF Threshold After Start		3.5	3.6		V
V_Z	Zener Voltage	CK=0V I_Z = 2mA	5.5	5.8	6	V
I_{CC}	Unloaded Supply Current	$OUT_{GATE1,2}$= no load		22	30	mA
		CK=0V $OUT_{GATE1,2}$= no load		3	5	
GATE DRIVER OUTPUTS						
V_{OL}	Output Low Voltage	$I_{OUTGATE1,2}$=-200mA		0.10	0.16	V
V_{OH}	Output High Voltage	$I_{OUTGATE1,2}$=200mA	4.70	4.85		V
I_{OUT}	Output Source Peak Current			2		A
	Output Sink Peak Current			3.5		
R_{OUT}	Output Series Source Resistance	$I_{OUTGATE1,2}$=-200mA		0.75	1.5	Ω
	Output Series Sink Resistance	$I_{OUTGATE1,2}$=200mA		0.5	0.8	
t_R	$OUT_{GATE1,2}$ Rise Time	C_{LOAD}=5nF (Note 1)		40		ns
t_F	$OUT_{GATE1,2}$ Fall Time	C_{LOAD}=5nF (Note 1)		30		ns
t_{P1}	Clock Propagation Delay to Turn ON of OUT_{GATE1}	No Load		130		ns
t_{P2}	Clock Propagation Delay to Turn ON of OUT_{GATE2}	No Load		50		ns
TURN-OFF ANTICIPATION TIME						
t_{ANT1}	OUT_{GATE1} Turn-off Anticipation Time	No Load		20		ns
t_{ANT2}	OUT_{GATE2} Turn-off Anticipation Time	V_{ANT2} = 0 to 1/3V_{CC}; no load		75		ns
		V_{ANT2} = 1/3V_{CC} to 2/3V_{CC}; no load		150		
		V_{ANT2} = 2/3V_{CC} to V_{CC}; no load		225		
$I_{SETANT2}$	Leakage Current (Note 2)		-0.1		0.1	µA
INHIBIT OUT_{GATE2} ENABLE						
V_H	Threshold Voltage	T_J = 25°C	-30	-25		mV
I_H	Leakage Current (Note 2)	$V_{INHIBIT}$ = 200mV		-400		nA
		$V_{INHIBIT}$ = -200mV			1	µA
$t_{ON(GATE2)}$	OUT_{GATE1} Turn-off Anticipation Time	$V_{INHIBIT}$ = 200mVNo Load		250		ns
V_{CK}	Reference Voltage	T_J = 25°C		2.6	2.8	V
I_{CK}	LX Leakage Current				600	µA
D_{OFF}	Duty Cycle Shut Down	T_J = 25°C for STSR2	13	14		%
	Duty Cycle Turn ON after Shut Down	T_J = 25°C for STSR2		18	20	
t_{PW}	Minimum Pulse Width	STSR2M			200	ns

Note1: t_R is measured between 10% and 90% of the final voltage; t_F is measurerd between 90% and 10% on the initiual voltage
Note2: Parameter guaranteed by design

TIMING DIAGRAM



APPLICATION INFORMATION : STSR2 IN FORWARD CONVERTER SECONDARY SIDE



NOTES
1) Ceramic Capacitors C1 and C2 must be placed very close to the IC;
2) R1 and R2 set the anticipation time by partitioning the Vcc voltage;
3) R3 and R4 is a resistor divider meant to provide the correct Ck voltage range;
4) R5 limits the current flowing through diode D2 when Freewheeling drain voltage is high;
5) D1 could be necessary to protect INHIBIT pin from negative voltages.
6) D2 could be necessary to protect INHIBIT pin from voltages higher than Vcc
7) D3 could be necessary to protect CK pin from voltages higher than Vcc.
8) SGLGND layout trace must not include $OUT_{GATE1,2}$ current paths.
9) A capacitor in parallel with R4 could be necessary to eliminate turn off voltage spike.

EXAMPLE OF COMPONENTS SELECTION FOR A FORWARD CONVERTER

Forward Specification:

V_{IN}=36-72V

V_{OUT}=3.3V

n=Np/Ns=4.5

R_3 and R_4 are calculated assuring a minimum voltage of 2.8V at Ck pin. At 36V input, the voltage on the secondary winding is 36/4.5=8V. Choosing R_3=1.5KΩ, R_4 results to be:

$$R_4 \geq \frac{V_{CK} + I_{CK(2.8)} \times R_3}{V_{IN} - I_{CK(2.8)} \times R_3 - V_{CK}} = 1k\Omega \times \frac{2.8V + 220\mu A \times 1.5k\Omega}{8V - 220\mu A \times 1.5k\Omega - 2.8V} = 965\Omega$$

R_4=1kΩ is chosen. At 72V input the current at Ck pin is calculated as:

$$I_{CK} = \frac{V_{IN(max)} - V_{CC} - 0.3}{R_3} = \frac{16 - 5 - 0.3}{1.5k\Omega} = 7.13mA$$

This value is below the maximum allowable current flowing into the Ck pin (10mA). If the 10mA value is exceeded an external diode connected to V_{CC} must be added (D3).

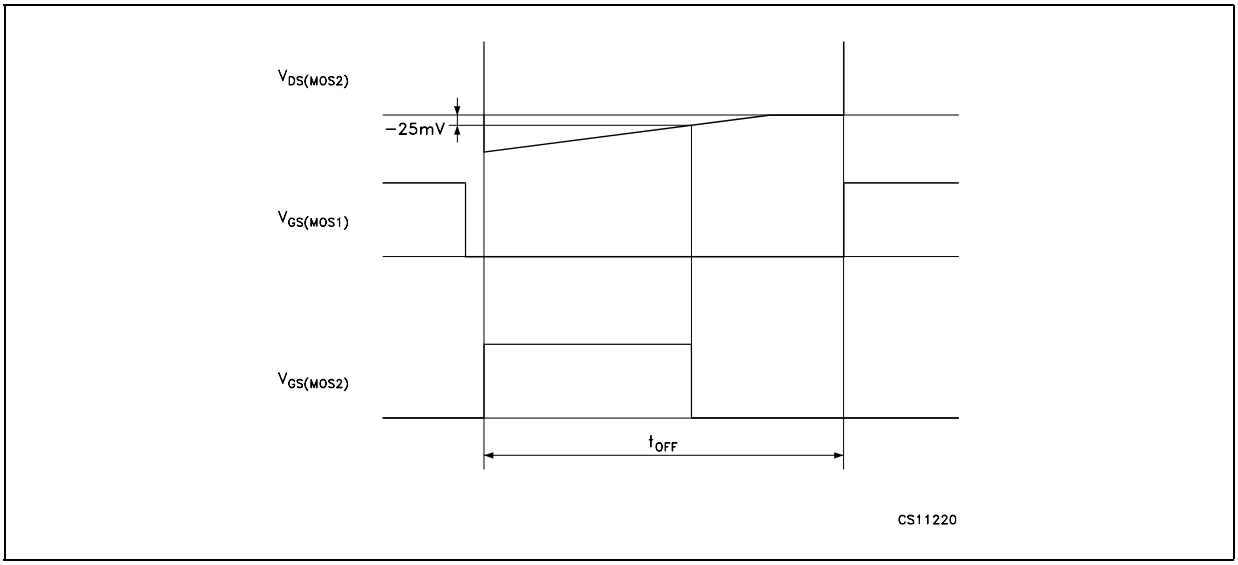
R_1 and R_2 values set the anticipation time for OUT_{GATE2}. For R_1=∞ and R_2=0, t_{ANT2}=75ns; for R_1=R_2=10kΩ, t_{ANT2}=150ns; for R_1=0 and R_2=∞, t_{ANT2}=225ns.

The RC group composed by R_5 and the parasitic capacitance of Inhibit pin (typically 5pF) delays the signal on Inhibit comparator. This delay must be lower than 200ns. This condition imposes a maximum value for R_5 of about 20kΩ.

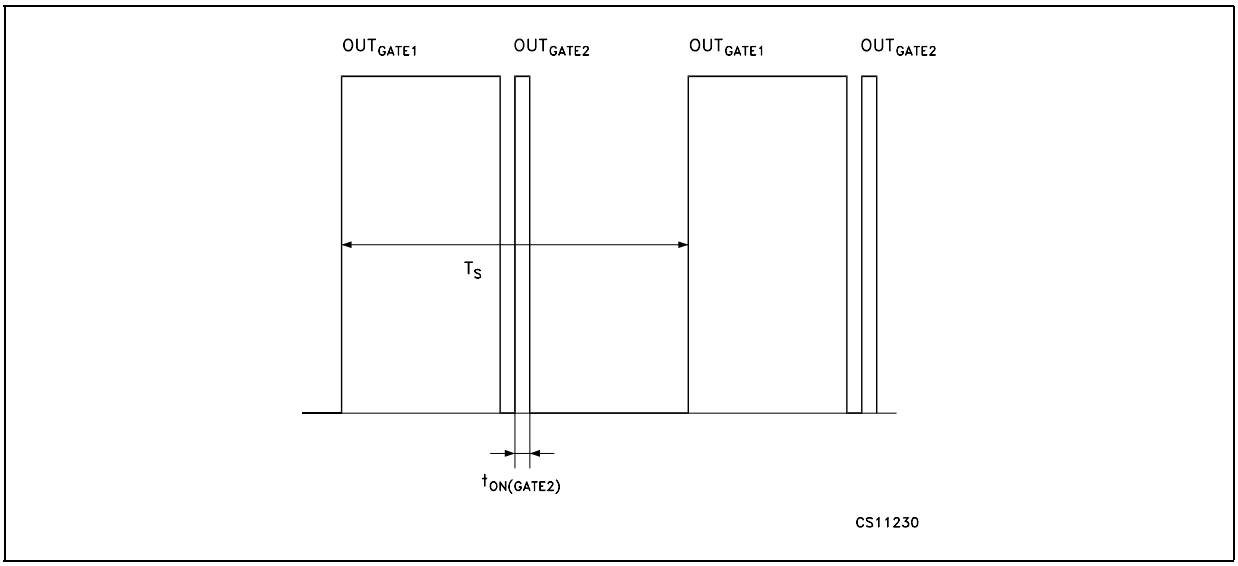
In general a suggested value for R_5 is 10kΩ. At 72V input, the secondary voltage is 16V, so the maximum current flowing into Inhibit pin is 16V/10kΩ=1.6mA which is below the maximum allowable current for the pin (10mA). If the 10mA value is exceeded an external diode (D2) connected to V_{CC} must be added.

The maximum negative voltage of –0.6V must be guaranteed for the Inhibit pin. If this negative voltage is exceeded the current must be limited to 50mA. If necessary, a diode (D1) connected to SGLGND can be added to satisfy this specification.

INHIBIT OPERATION OF OUT_{GATE2} IN DISCONTINUOUS CONDUCTION MODE



INHIBIT OPERATION OF OUT_{GATE2}



NOTE: $V_{INHIBIT}$ =+200mV

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j = 25°C

Figure 1 : Zener Characteristics

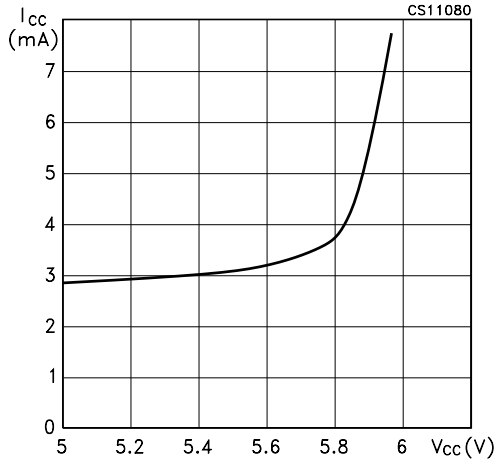


Figure 2 : Rise and Fall Time vs Load Capacitor

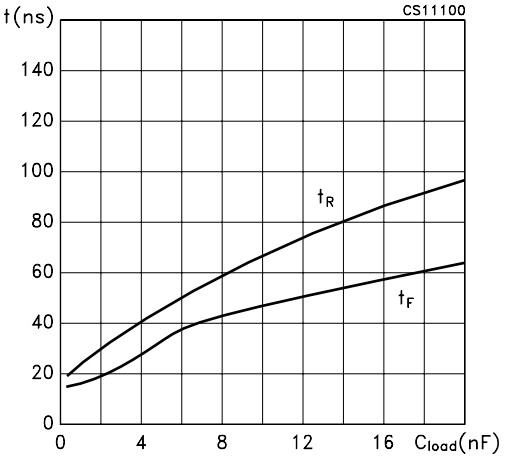


Figure 3 : $OUT_{GATE1,2}$ vs Characteristics

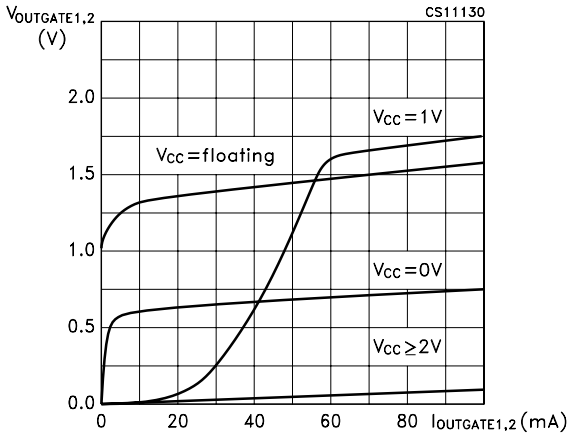


Figure 4 : Sink-Source ON Resistance vs Temperature

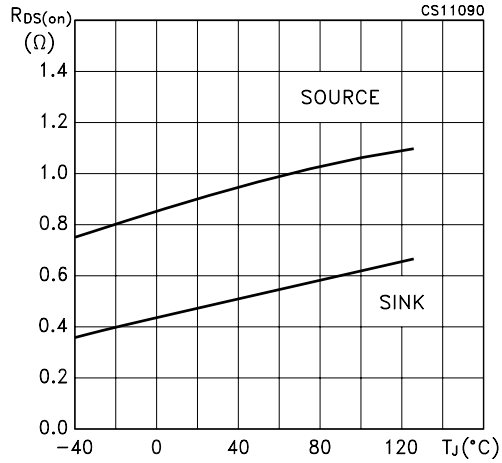


Figure 5 : Clock Threshold Voltage vs Temperature

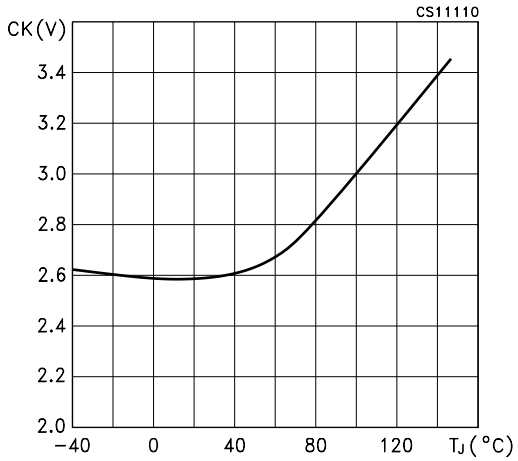


Figure 6 : INHIBIT Threshold Voltage vs Temperature

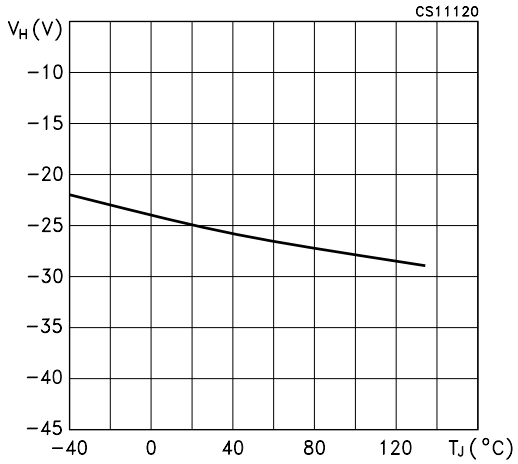


Figure 7 : Supply Current vs Load Capacitor (each output)

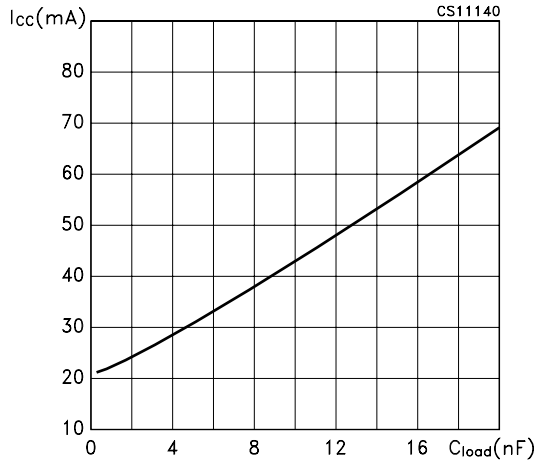


Figure 8 : Supply Current vs Clock Frequency

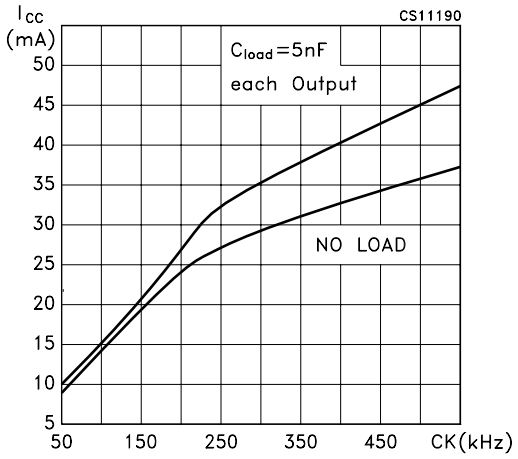


Figure 9 : $T_{ON(GATE2)}$ vs Temperature

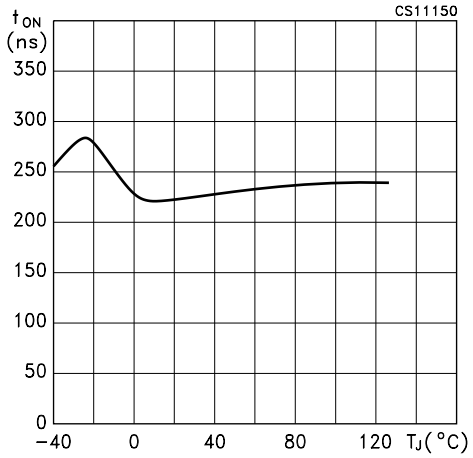


Figure 10 : Duty Cycle Shut Down vs Temperature

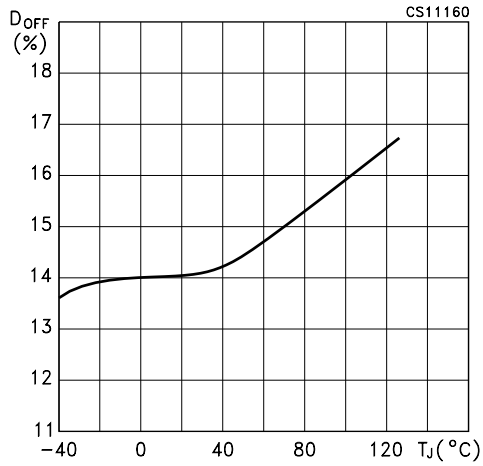


Figure 11 : Duty Cycle Turn ON After Shut Down vs Temperature

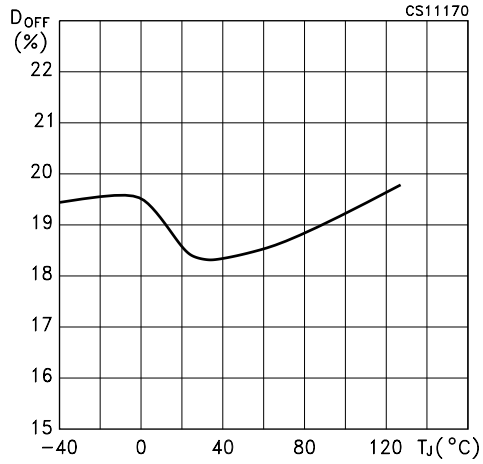
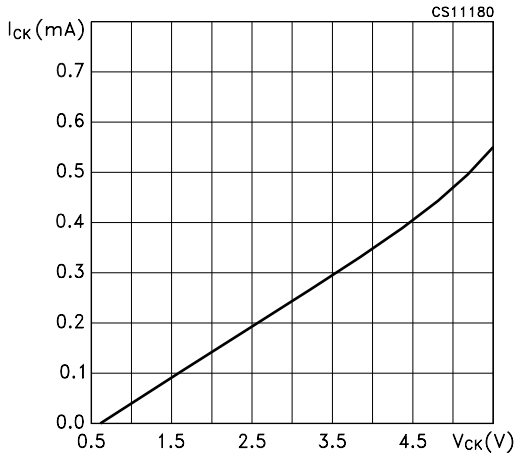
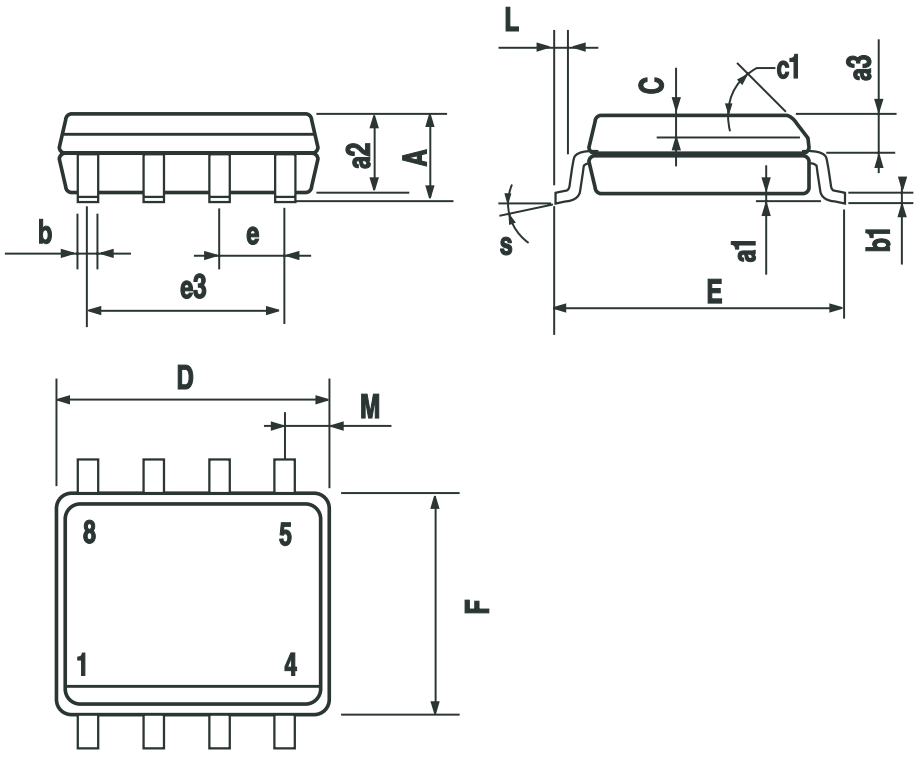


Figure 12 : Clock Leakage Current vs Clock Voltage



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.189		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.149		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



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