凌陽科技
SUNPLUS

Preliminary

SPR1024A

128Kx8 BITS BUS FLASH

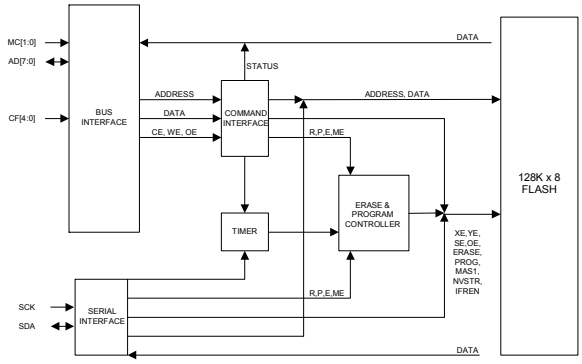
GENERAL DESCRIPTION

SPR1024A is a high-performance 1M-bit bus FLASH organized as 128k-byte. With an embedded Bus Memory Interface (BMI) and a Serial interface, SPR1024A allows CPU to access FLASH through 8-bit parallel mode or 1-bit serial mode. To support different access modes of SPDC series CPU, SPR1024A can be defined as 8 configuration types. With 2.7V to 3.6V power supply voltage, SPR1024A can operate up to 4.0MHz. Maximum read current is 1mA and maximum program/erase current is 4mA.

FEATURES

- 1M-bit (128k x 8 bits)
- 128 separate pages for erase operation
- Supply voltage: 2.7V - 3.6V
- Operating frequency: 4.0MHz
- Operating current: read 1mA(Max.), program/erase 4mA(Max)
- Standby current: 1μA (Max.)
- TTL-compatible I/O
- Bus memory interface or Serial interface

BLOCK DIAGRAM



BLOCK DESCRIPTION

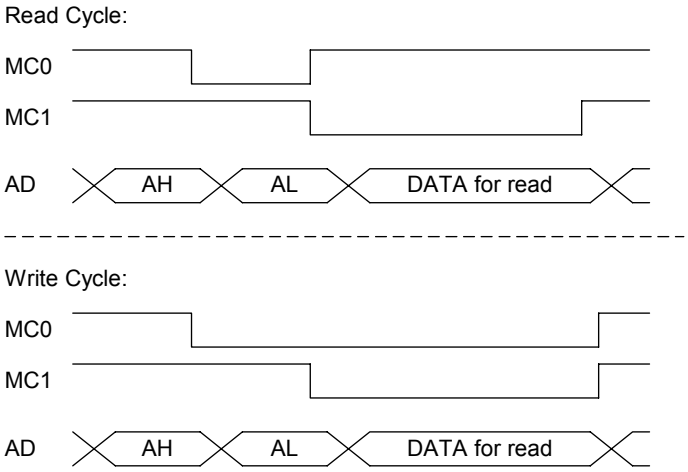
This device contains six components: Bus Interface (BIF), Serial Interface (SIF), Command Interface (CIF), timer, erase & program controller (EPCON) and a 1Mb FLASH. TMODE, ENZ and CF3 - 0 define the CPU types and access modes. When BIF is chosen, MC0 and MC1 act as the Read/Write control signal and AD7 - 0 are the bi-directional Address/Data bus. BIF processes these signals and generates chip enable ($\overline{CE}$), output enable ($\overline{OE}$), write enable ($\overline{WE}$) and FLASH's address in READ mode. In WRITE mode, BIF generates FLASH's data also. CIF interprets signals generated by BIF. If CIF receives READ command, it reads from FLASH directly. If CIF receives PROGRAM, ERASE or MASS ERASE, it forwards these commands to EPCON to accomplish them. When SIF is chosen, SCK acts as serial clock and SDA acts as 1-bit serial I/O. If READ command is received, SIF can read from flash directly. But if PROGRAM, ERASE or MASS ERASE is received, SIF also forwards these commands to EPCON. When EPCON is active, it needs a 200 kHz clock which is provided by the TIMER block shown in block diagram.

BMI DESCRIPTION

BMI is an interface between SPDC series CPU and its memory. It provides flexible and efficient memory management. CPU can access up to 4M-bit FLASH via BMI. BMI contains an 8-bits bi-directional Address/Data bus, AD bus, which is multiplexed by 2 control signals, MC0 and MC1. MC0 decides operation mode (Read or Write), and MC1 decides AD bus to be address or data bus. MC0 and MC1 decode table list as below:

MC1	MC0	AD BUS	Bus ROM Power
L	L	Data for Write	Standby
L	H	Data for Read	Active
H	L	AL	
H	H	AH	Standby

The simple timing relation is as follows:



According to memory mapping strategy, SPDC series CPUs are classified into two groups. First group includes SPDC1016, SPDC1064 and SPDC4000 series. Second group includes SPDC256 - 2000.

■ BMI MEMORY MAPPING FOR SPDC1016, SPDC1064 & SPDC4000

The BMI uses CPU address from 4000h to FFFFh and duplicates some CPU registers in BMI as bank switch to map up to total 4M-bits FLASH.

The register usage and mapping table is as below:

Register[bits]	Alias	Usage
0000 [7:0]	BSW[7:0]	4000-BFFF memory bank switch (8 bits)
000A[7]	ROA	4000-BFFF ROM/RAM select (0:ROM / 1:RAM)
000A[3:0]	BBS[3:0]	C000-DFFF BIOS bank switch
000D[1:0]		Volume ID
001A[7]	CVOL0	0: C000-FFFF Volume 0, 1: C000-FFFF depend on Volume select

	TYPE A, C, E (ROM)												TYPE B, D, F (RAM)					
4000	xrm 04	Xmn 00C	xmn 014	xmn 01C	xmn 024		xmn 3F4	xmn 3FC	xmn 404		xmn 7F4	xmn 7FC	xrm 04	xrm 0C	xrm 14		xrm 7F4	xrm 7FC
6000	xrm 06	Xmn 00E	xmn 016	xmn 01E	xmn 026		xmn 3F6	xmn 3FE	xmn 406		xmn 7F6	xmn 7FE	xrm 06	xrm 0E	xrm 16		xrm 7F6	xrm 7FE
8000	xmn 000	Xmn 008	xmn 010	xmn 018	xmn 020		xmn 3F0	xmn 3F8	xmn 400		xmn 7F0	xmn 7F8	xrm 00	xrm 08	xrm 10		xrm 7F0	xrm 7F8
A000	xmn 002	Xmn 00A	xmn 012	xmn 01A	xmn 022		xmn 3F2	xmn 3FA	xmn 402		xmn 7F2	xmn 7FA	xrm 02	xrm 0A	xrm 12		xrm 7F2	xrm 7FA
ROA	0	0	0	0	0		0	0	0		0	0	1	1	1		1	1
BSW	00	01	02	03	04		7E	7F	80		FE	FF	00	01	02		FE	FF

C000	xmn 004	Xrm 06	xmn 000	xmn 002	xmn 00C	xmn 00E	xmn 008	xmn 00A	xmn 014	xmn 016	xmn 010	xmn 012	xmn 01C	xmn 01E	xmn 018	xmn 01A
BBS	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

E000	xmn 006

Note1: The blocks of same shadow color are double mapping.

Note2: xmn means expanded bus memory.

Note3: The size of each block is 128k-bits.

Note4: The digit in every block multiplied by 1000 represent the physical address of memory.

For example:

C000	xmn 008	8000	xmn 008

BBS = 6 ROA = 0

BSW = 01

That means if CPU accesses to [C000-DFFF when BBS = 6] or [8000-9FFF when ROA = 0 and BSW = 01] (double mapping), BMI will map these address to the physical address 008000-009FFF of FLASH.

■ BMI MEMORY MAPPING FOR SPDC256-2000

The BMI uses CPU address from 4000h to FFFFh and duplicates some CPU registers in BMI as bank switch to map address. When CPU address is between 4000h to BFFFh, if bank switch is from 00 to 7Fh, then the mapping address locate in internal ROM which is built in CPU. If Bank switch is from 80h to FFh, then the mapping address locate in expanded memory (FLASH or ROM). When CPU address is between C000h to FFFFh, If EXC = 0, the mapping address locate in internal ROM. Otherwise, if EXC = 1, it is in expanded memory, which is double mapped to address from 4000h to 7FFFh at BSW = 80. The register usage and mapping table is as below.

Register[bits]	Alias	Usage
0000 [7:0]	BSW[7:0]	4000-BFFF memory bank switch (8 bits)
0007[7]	MEXT	1: bus memory enable
000B[1]	EXC	0:C000-FFFF internal, 1:C000-FFFF
000D[2:0]		Volume ID
001A[7]	CVOL0	0: C000-FFFF Volume 0, 1: C000-FFFF depend on Volume select

Address									Type G						
4000	rom 04	rom 00C	rom 014	rom 01C	rom 024		rom 3F4	rom 3FC	xmn 404	xmn 40C	xmn 414	xmn 424		xmn 7F4	xmn 7FC
6000	rom 06	rom 00E	rom 016	rom 01E	rom 026		rom 3F6	rom 3FE	xmn 406	xmn 40E	xmn 416	xmn 426		xmn 7F6	xmn 7FE
8000	rom 000	rom 008	rom 010	rom 018	rom 020		rom 3F0	rom 3F8	xmn 400	xmn 408	xmn 410	xmn 420		xmn 7F0	xmn 7F8
A000	rom 002	rom 00A	rom 012	rom 01A	rom 022		rom 3F2	rom 3FA	xmn 402	xmn 40A	xmn 412	xmn 422		xmn 7F2	xmn 7FA
BSW	00	01	02	03	04		7E	7F	80	81	82	83		FE	FF

address	(Type G)
C000	rom/xmn 404
E000	rom/xmn 406

Note1: xmn means expanded bus FLASH.

Note2: rom means internal ROM

Note3: The digit in every block multiplied by 1000 represent the physical address of FLASH.

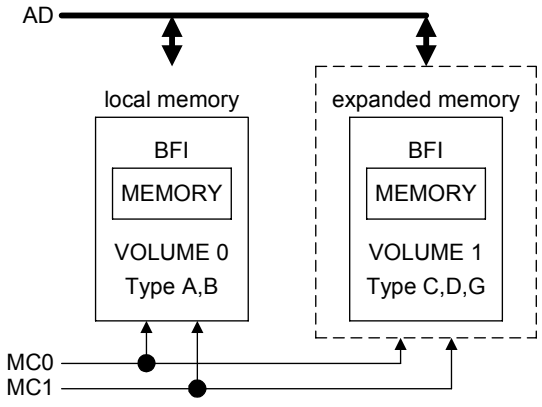
ACCESS MODE DESCRIPTION

There're two ways for hardware to identify the local memory and the expanded memory. It's defined by the configuration control signal:

■ CASCADE MODE (TYPE A, B, C, D, G):

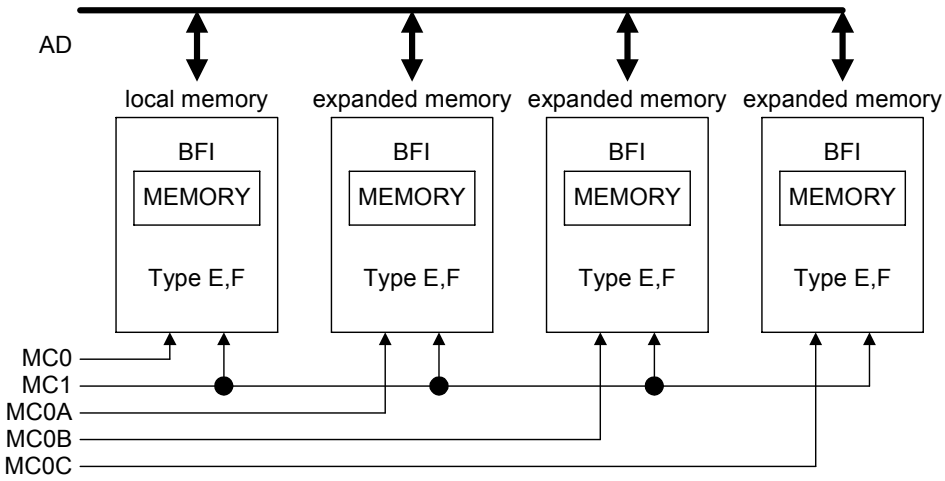
For SPDC older version CPU and considered only expand to volume 1.

(The build in volume ID is fixed to 1 for type C, D, and G)



■ CHIP SELECT MODE (TYPE E, F):

MC0 is decoded by volume to MC0A, MC0B, and MC0C.



CONFIGURATION MODE SUMMARY

CPU	Type	Decode mode	Bank switch	CF8-CF3*	Volume ID	Volume select	type
SPDC1016	Volume 0 ROA = 0		00-03	00	0	0-3	A
			40-43	01			
			80-83	02			
			7C-7F	3D	0	0-3	
			BC-BF	3E			
			FC-FF	3F			
	Volume 0 ROA = 1		00-03	00	0	0-3	B
			40-43	01			
			80-83	02			
			BC-BF	3E	0	0-3	
			FC-FF	3F			
SPDC1016	Volume 1 ROA = 0		00-03	00	1	0-3	C
			40-43	01			
			80-83	02			
			BC-BF	3E	1		
			FC-FF	3F			
	Volume 1 ROA = 1		00-03	00	1	0-3	D
			40-43	01			
			80-83	02			
			BC-BF	3E	1		
			FC-FF	3F			

CPU	Type	Decode mode	Bank switch	CF8-CF3*	Volume ID	Volume select	type
SPDC1064 SPDC4000	ROA=0	Chip select	00-03	00		0-3	E
			40-43	01			
			80-83	02			
			BC-BF	3E			
			FC-FF	3F			
	ROA=1	Chip select	00-03	00		0-3	F
			40-43	01			
			80-83	02			
			BC-BF	3E			
			FC-FF	3F			
SPDC256-2000	Built in		00-7F		0		
	Extended ROM	Cascade (CI/CO)	80-83	20	1	0-7	G
			84-87	21			
			FC-FF	3F	1	0-7	

* For the reason to cost down, only 2 bit (CF3 & CF4) is selected to configure the mapping.

CONFIGURATION PINS DEFINE:

Type		CF2	CF1	CF0
BUS MODE	A	0	0	0
	B	0	0	1
	C	0	1	0
	D	0	1	1
	E	1	0	0
	F	1	0	1
	G	1	1	0
SERIAL MODE		1	1	1

CF3 & CF4 are used to define the starting bank:

Type	CF4	CF3	Bank switch	Multi-mapping				
A, B, C, D, E, F	0	0	00-03 (00-3F)	00-03	04-07	08-0B		3C-3F
	0	1	40-43 (40-7F)	40-43	44-47	48-4B		7C-7F
	1	0	80-83 (80-BF)	80-83	84-87	88-8B		BC-BF
	1	1	C0-C3 (C0-FF)	F0-F3	F4-F7	F8-FB		FC-FF
G	1	0	80-83 (80-BF)					
	1	1	C0-C3 (C0-FF)					

BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0
CF4	CF3	X	X	X	X		

PIN DESCRIPTION

Mnemonic	PIN No.	Type	Description
CF4 - 1 CF0	16 - 13 19	I	Configuration Inputs
AD7 - 0	9 - 2	I/O	Address/Data I/O
MC1 - 0	21 - 20	I	Control signal
$\overline{\text{RESET}}$	22	I	Reset
ENZ	23	I	Bus Interface/Serial Interface selector
VDD	17, 1	I	Power Supply
VSS	11	I	Ground
SDA	10	I/O	Serial Interface data I/O
SCK	18	I	Serial Interface Clock
TEST	12	I	TEST MODE
NC	0	I	No connection

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
Supply Voltage to Ground Potential	VDD	-0.5V~4.5V
Ambient Operating Temperature	T_A	-10℃~ 80℃
Storage Temperature	T_{STG}	-65℃~150℃
Output Voltage	V_{OUT}	-0.5V~VDD+0.5V
Input Voltage	V_{IN}	-0.5V~VDD+0.5V

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

RECOMMENDED DC OPERATING CONDITIONS (VDD =2.7V - 3.6V, T_A = 0 - 70℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Supply Voltage	VDD	2.7	3.0	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.4	V

DC ELECTRICAL CHARACTERISTICS (VDD = 2.7 - 3.6V, T_A = 0 - 70℃)

Characteristic	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	2.3	-	-	V	I_{OH} = -1.0mA
Output Low Voltage	V_{OL}	-	-	0.3	V	I_{OL} = 1.0mA
Input Leakage Current	$I_{I(L)}$	-	-	1.0	µA	
Output Leakage Current	$I_{O(L)}$	-	-	1.0	µA	
Operating Supply Current (f = 4.0MHz), C_L = 80pF	I_{CC}	-	-	4.0	mA	
Standby Current (CMOS)	I_{SB}	-	-	1.0	µA	MC0 = MC1 = VDD AD[0:7] = VSS

AC OPERATING CHARACTERISTICS (VDD = 2.7 - 3.6V, T_A = 0 - 70℃) for Bus Interface

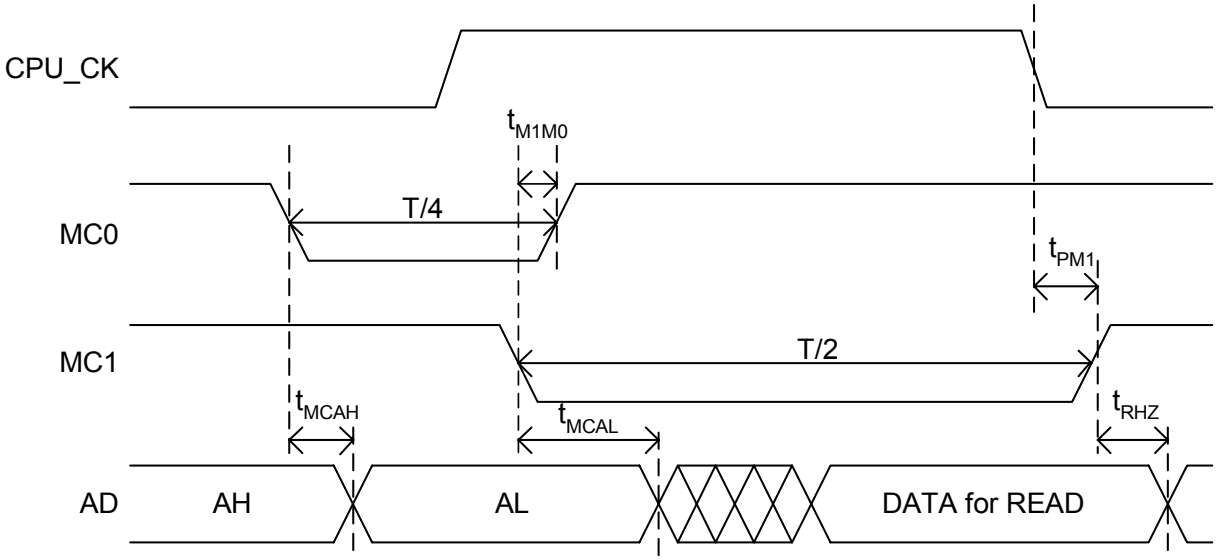
Characteristic	Symbol	Min.	Max.	Unit
Read cycle				
Read cycle period	T	250	-	ns
MC0 falling to AH end	t_{MCAH}	15	-	ns
MC1 falling to MC0 rising	t_{M1M0}	-20	10	ns
MC1 falling to AL end	t_{MCAL}	-	35	ns
Data latch to MC1 falling	t_{PM1}	20	35	ns
MC1 rising to AD Hi-Z	t_{RHZ}	-	5.0	ns
Write Cycle				
MC0 rising to MC1 rising	t_{MCW}	15	20	ns
MC1 rising to AD Hi-Z	t_{RHZ}	15	-	ns

AC TEST CONDITION

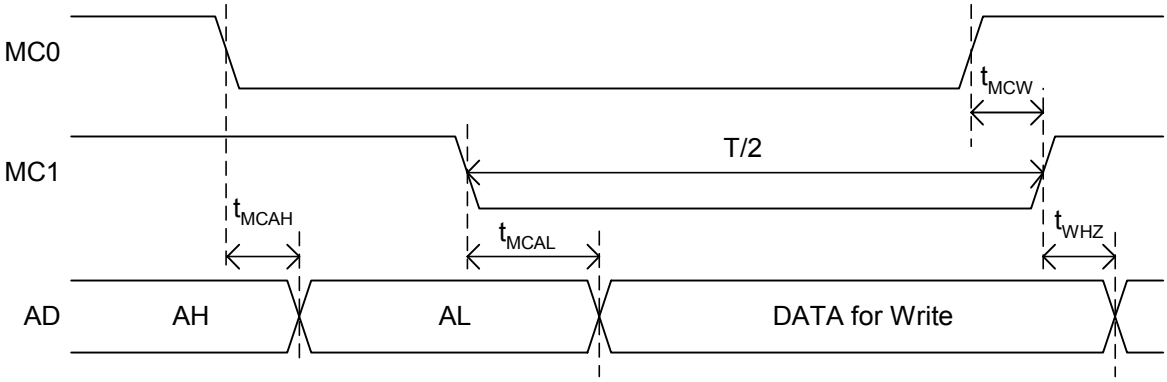
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	10ns
Input and Output Timing Level	1.5V
Output Load	C_L = 80pF

TIMING WAVEFORMS FOR BUS INTERFACE

■ READ CYCLE



■ WRITE CYCLE



ADDRESS MAPPING FOR FLASH CONTROL

Software command sequence: CPU should write the Volume ID and BANK00 or BBS0A before those command sequences. That will detect which chip is selected. Address in the following table indicates FLASH's physical address. ***BSW, BBS, and address must be set to the physical address of the FLASH!***

The BANK00 should be set to

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CF4	CF3	X	X	X	X	BS1	BS0

CF4 & CF3 for selecting starting address (banks)

CF4 - 3	00	01	10	11
Bank (00H)	00-03	40-43	80-83	C0-C3

BANK00[b7:b6] assign to [CF4:CF3]. BANK00[b5:b0] set to the bank which is going to be read, programmed or erased.

Command sequence	Bus cycle											
	1nd		2rd		3th		4th		5th		6th	
	Addr	data	addr	data	addr	data	Addr	data			addr	data
S/W ID entry	5555h	AAh	AAAAh	55h	5555h	90h	8000h/ 8001h	ID (read)				
Read status	5555h	AAh	AAAAh	55h	5555h	70h	Any addr.	Status(6)				
Return to normal mode (RESET)	XXXX	F0h										
Main memory												
Read	RA	RD (read)										
Byte program	5555h	AAh	AAAAh	55h	5555h	A0h	PA(3)	PD(4)				
Page Erase	5555h	AAh	AAAAh	55h	5555h	80h	5555h	AAh	AAAAh	55h	EA(5)	30h
Mass erase	5555h	AAh	AAAAh	55h	5555h	80h	5555h	AAh	AAAAh	55h	5555h	10h

Command sequence	Bus cycle											
	1nd		2rd		3th		4th		5th		6th	
	Addr	data	addr	data	addr	data	Addr	data			addr	data
Information block												
I-Read	5555h	AAh	AAAAh	55h	5555h	78h	RA	RD (read)				
I-Byte program	5555h	AAh	AAAAh	55h	5555h	A8h	PA(3)	PD(4)				
Inf. erase(1)	5555h	AAh	AAAAh	55h	5555h	88h	5555h	AAh	AAAAh	55h	5555h	30h
Bmass erase(2)	5555h	AAh	AAAAh	55h	5555h	88h	5555h	AAh	AAAAh	55h	5555h	10h

(1) Only erase information block.

(2) Erase both main block and information block.

(3) PA: program byte address

(4) PD: program data

(5) EA: page erase address (gray bits in next table)

(6) Status: b7 for 0/1: busy/ready, b3 for 0/1: fail/success

■ PRODUCT IDENTIFICATION TABLE

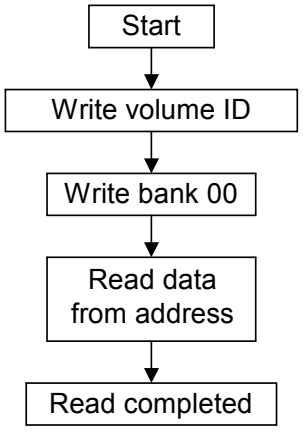
	Address	Data
Manufacture's code	00000h	C7h
Device code	00001h	D5h

■ **ADDRESS SUMMARY**

Flash ADDR.			CPU mapping	CPU mapping
Main	Inform.		4000h – BFFFh	C000h - DFFFh
		CF4	BS7	0
		CF3	BS6	0
X9	x	FA16	BS1	BBS3
X8	x	FA15	BS0	BBS2
X7	x	FA14	A14	BBS1
X6	x	FA13	A13	BBS0
X5	x	FA12	A12	A12
X4	x	FA11	A11	A11
X3	x	FA10	A10	A10
X2	0	FA9	A9	A9
X1	0	FA8	A8	A8
X0	X0	FA7	A7	A7
Y6	Y6	FA6	A6	A6
Y5	Y5	FA5	A5	A5
Y4	Y4	FA4	A4	A4
Y3	Y3	FA3	A3	A3
Y2	Y2	FA2	A2	A2
Y1	Y1	FA1	A1	A1
Y0	Y0	FA0	A0	A0

The addresses in gray shadow are page erase addresses.

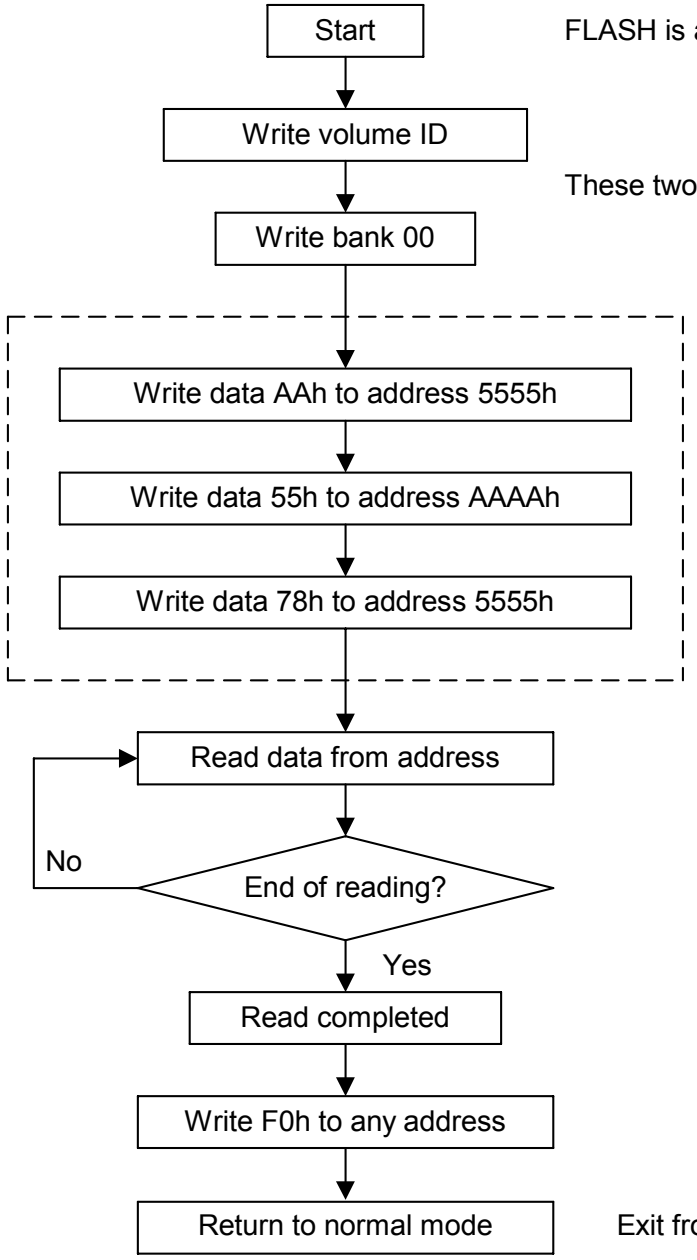
READ SEQUENCE (MAIN BLOCK)



FLASH is already at normal operation

These two steps will detect which chip is selected

READ SEQUENCE (INFORMATION BLOCK)



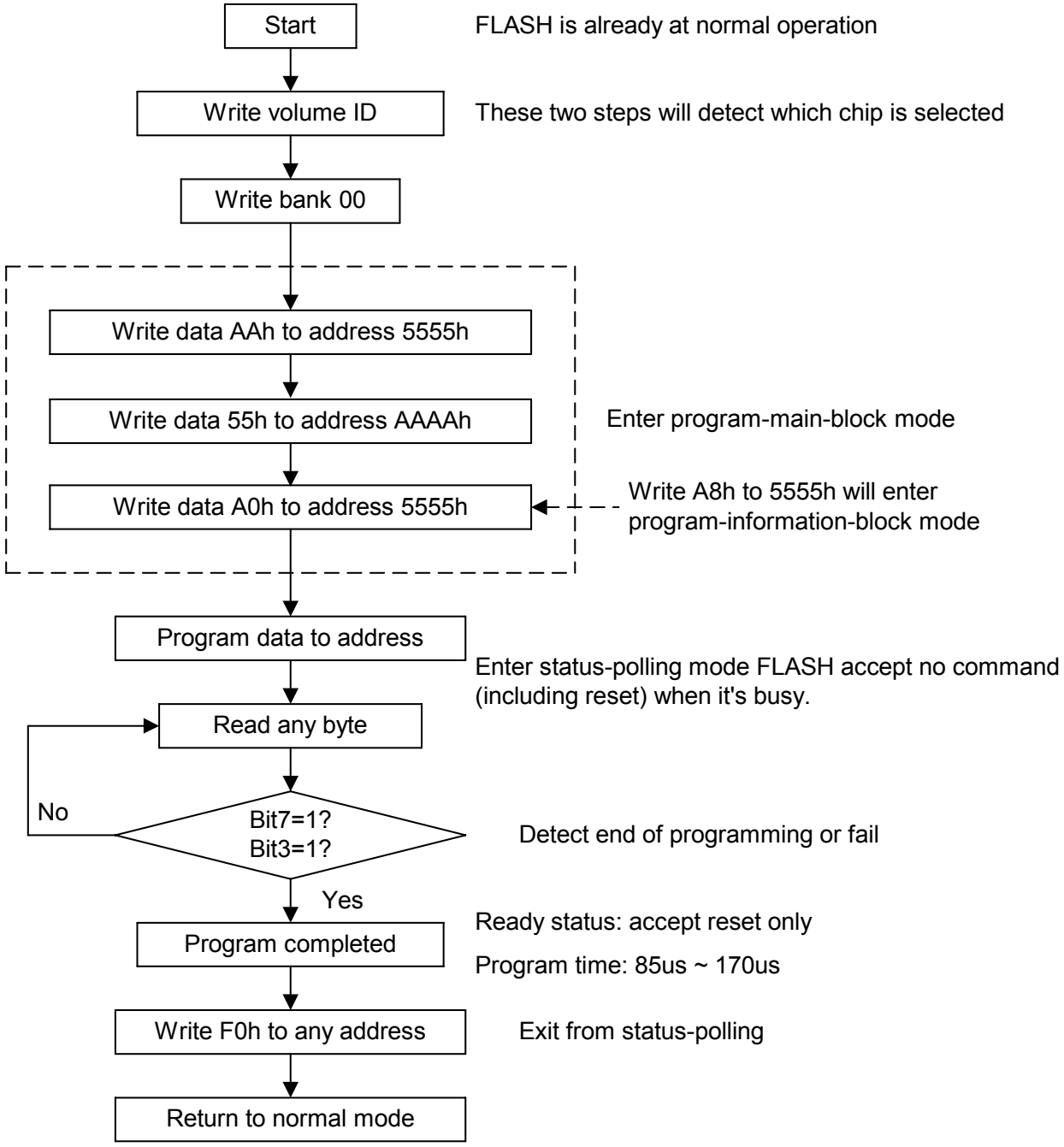
FLASH is already at normal operation

These two steps will detect which chip is selected

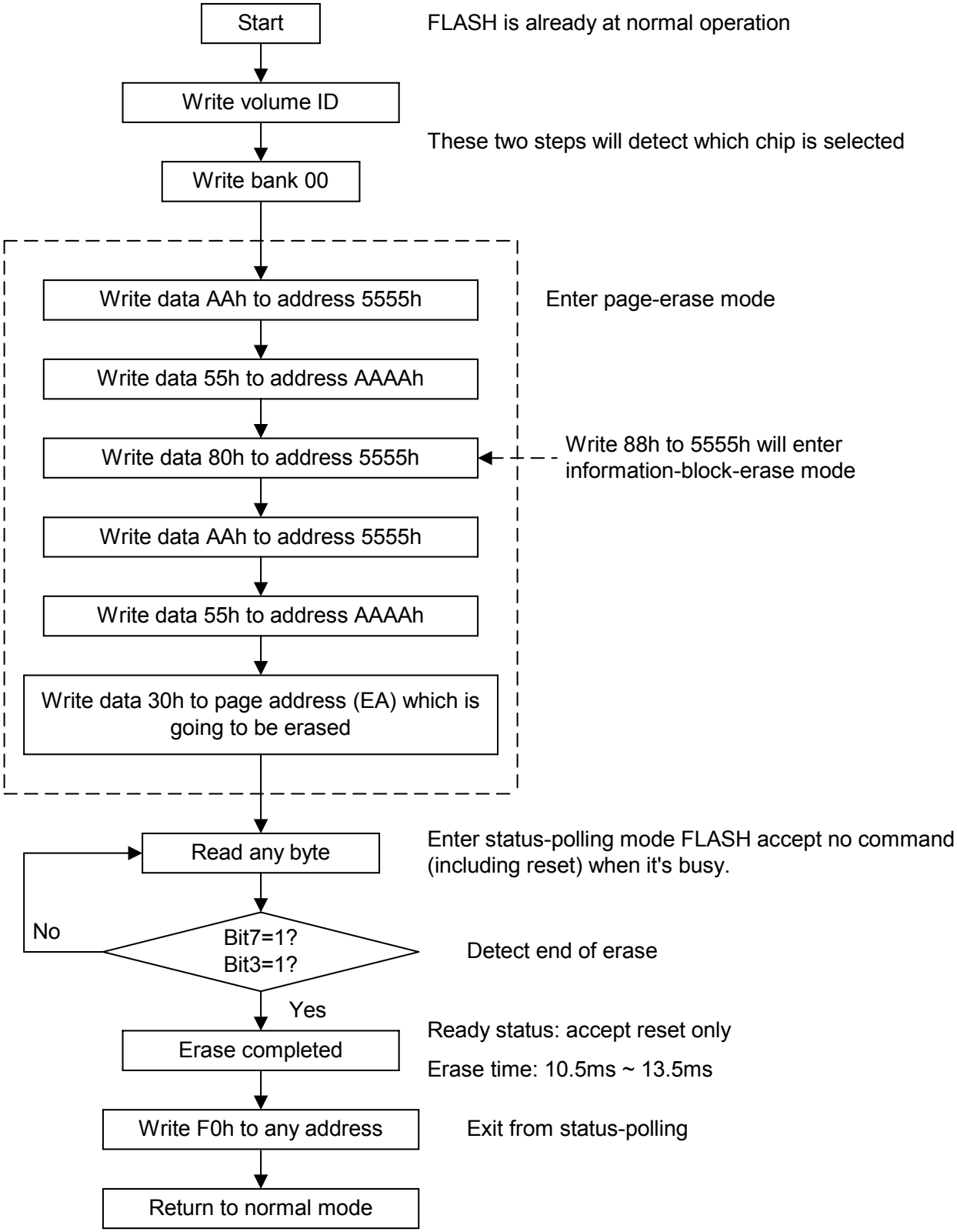
Enter read-information-block mode

Exit from information block

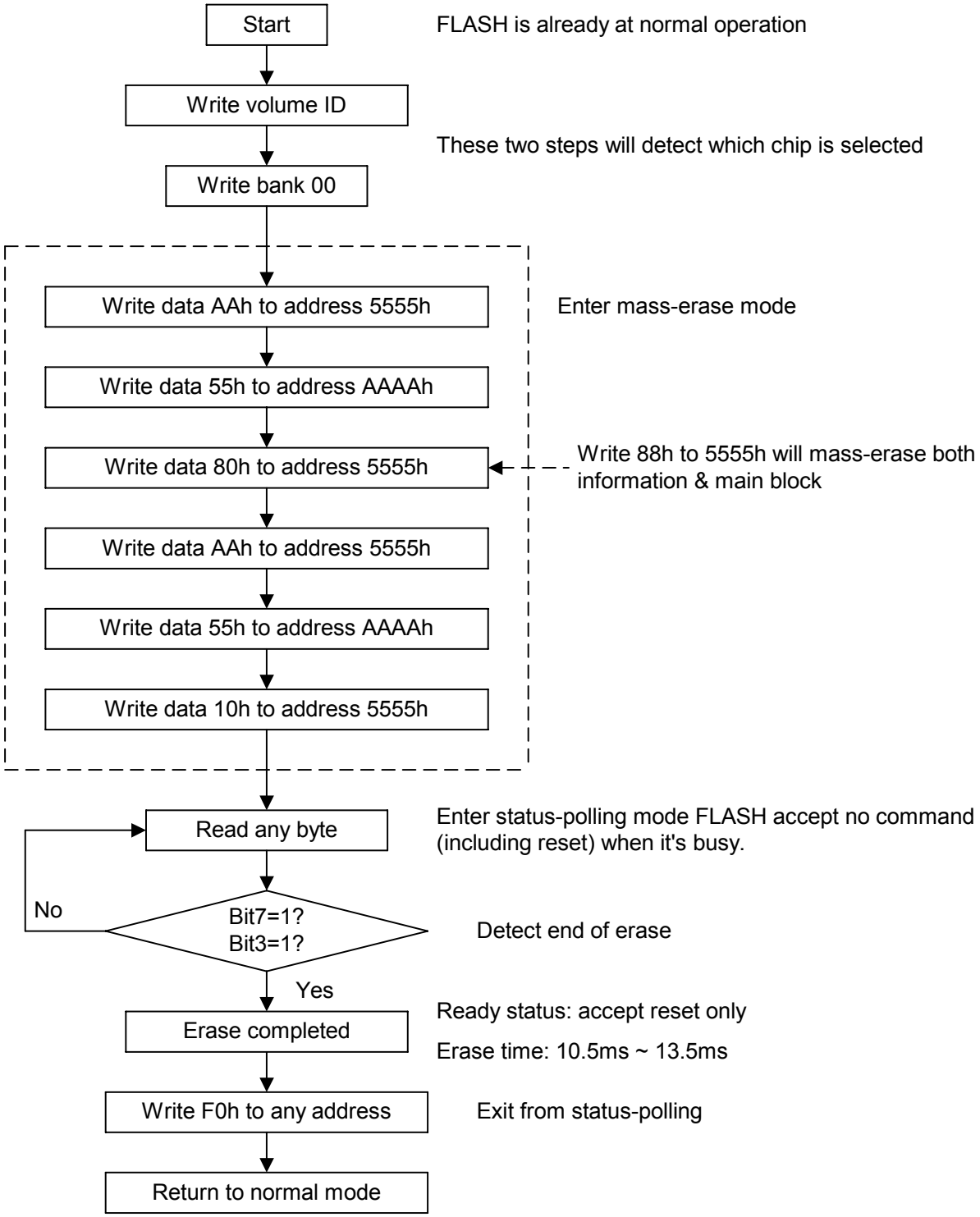
BYTE PROGRAM SEQUENCE



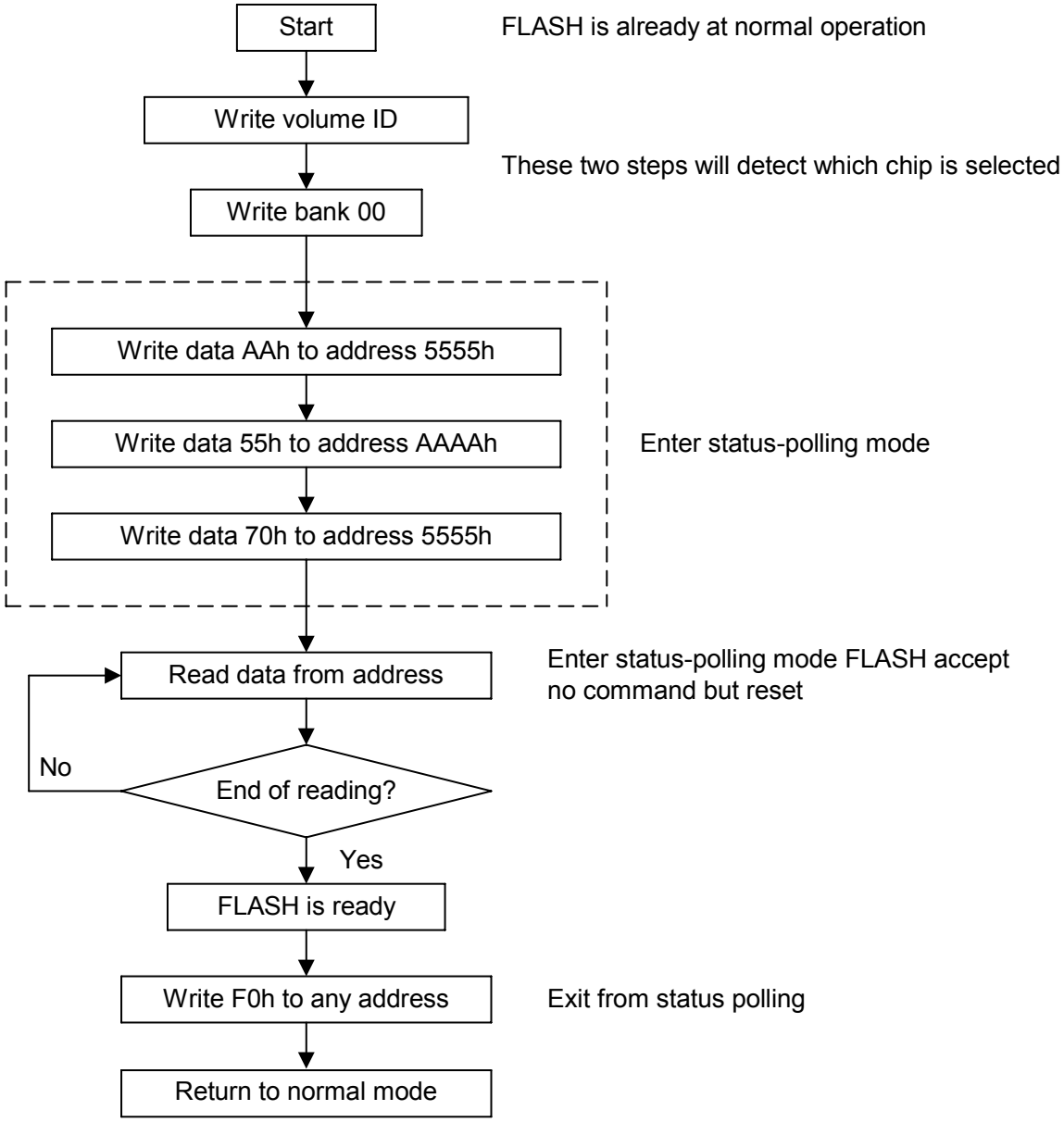
PAGE ERASE SEQUENCE



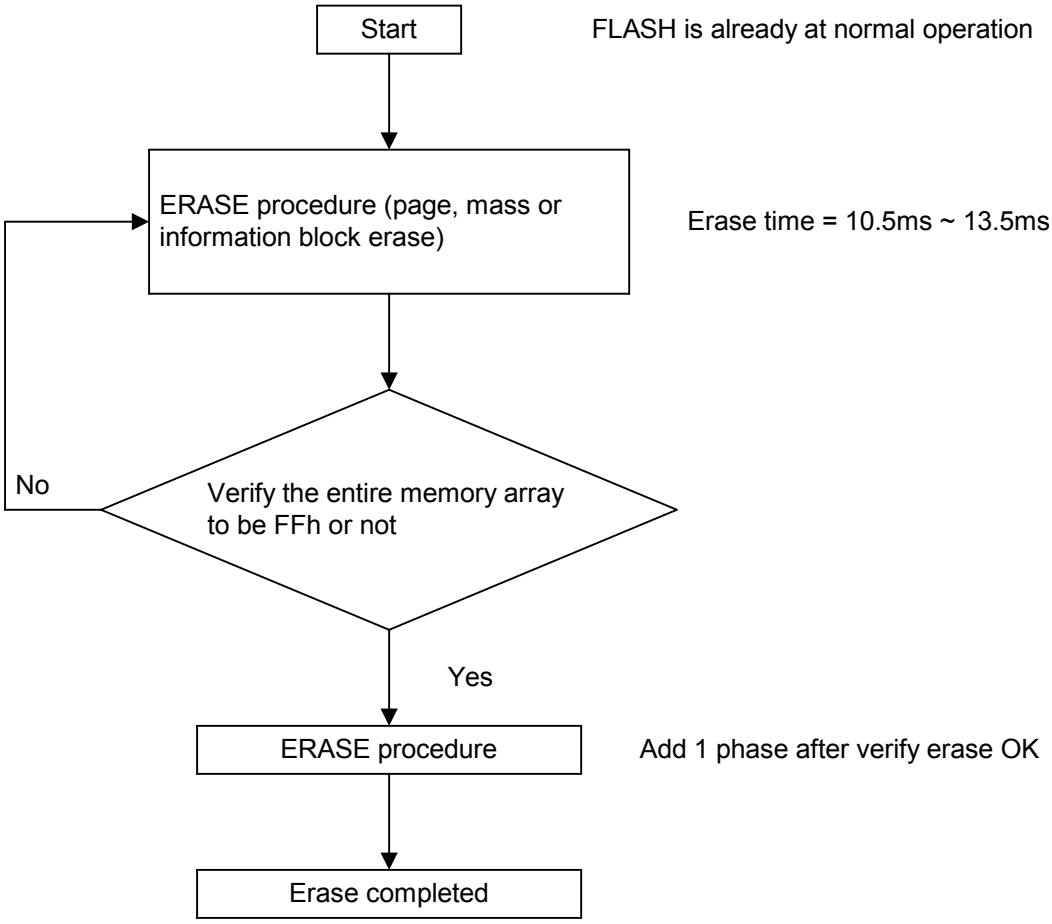
MASS ERASE SEQUENCE



ENTER STATUS-POLLING MODE FROM NORMAL MODE



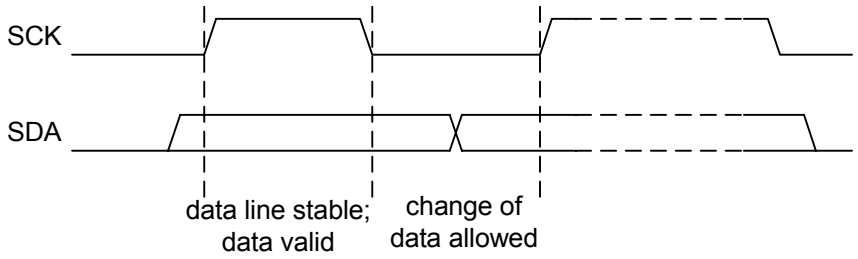
ERASE ALGORITHM FOR IMPROVING ENDURANCE PERFORMANCE



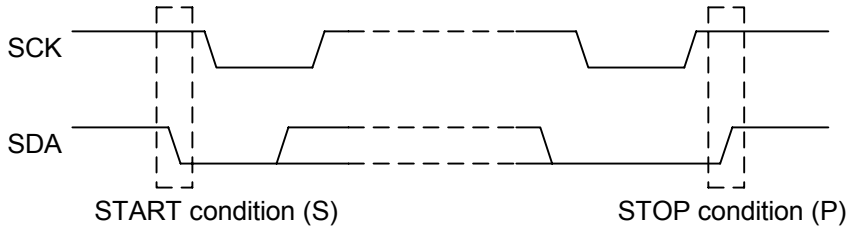
SERIAL INTERFACE

■ BIT TRANSFER

One clock pulse is generated for each data bit transferred. The data on SDA line must be stable during the HIGH period of clock. The HIGH or LOW states of the data line can only change when the clock signal on the SCK line is LOW.



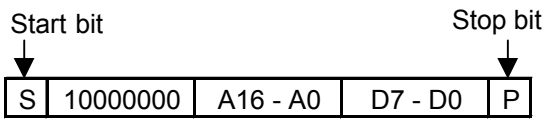
Within the procedure of the SPSI serial interface, unique situations arise which are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on SDA line while SCK is HIGH indicates a START condition. A LOW to HIGH transition on SDA line while SCK is HIGH defines a STOP condition.



■ INSTRUCTION SET

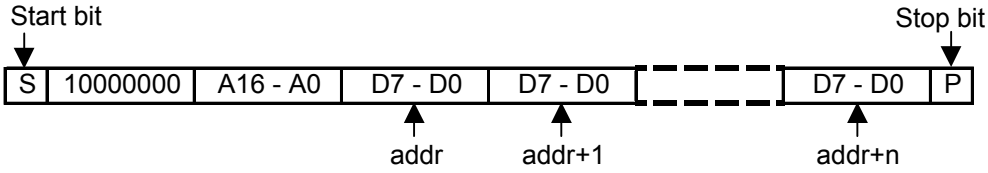
(1) Main block READ with random address access:

Main block READ command is a start bit followed by an 8-bit opcode (A[24:17]=10000000) and a 17-bit address (A[16:0]). After receiving main block READ command, the SDA line should be set to the high-impedance state. SPR1024A will begin shifting out the data addressed (MSB first) on the falling edge of the SCK clock and the output data bit will be stable after the specified time delay (t_{ACC}). After 8 data bits are shifted out, a stop bit is needed to terminate the command.



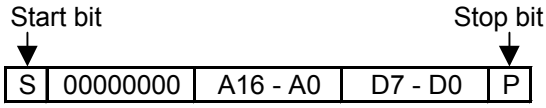
(2) Main block READ with auto-address-count:

Main block READ with auto-address-count command is the same as main block READ except that after first 8 data bits are shifted out, no stop bit is inserted before the next SCK falling edge. SPR1024A will automatically increase the address by 1 and its data content will be shifted out by the clock cycle that followed. The procedure will continue until a stop bit is received.



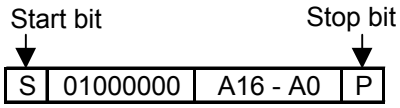
(3) Main block BYTE PROGRAM:

Main block BYTE PROGRAM command is a start bit followed by an 8-bit opcode (A[24:17]=00000000), a 17-bit address (A[16:0]) and an 8-bit data (D[7:0]). After receiving main block BYTE PROGRAM command, a specified interval (t_{PGM}) is needed to program data into the FLASH. Then, a stop bit terminates the command.



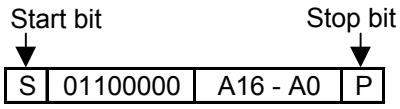
(4) Main block PAGE ERASE:

Main block PAGE ERASE command is a start bit followed by an 8-bit opcode (A[24:17]=01000000) and a 17-bit address (A[16:0]). A16 to A10 are used to select which page to be erased. A9 to A0 are DON'T CARE. After receiving main block PAGE ERASE command, a specified interval (t_{ERASE}) is needed to erase the selected page of the FLASH. Then, a stop bit terminates the command.



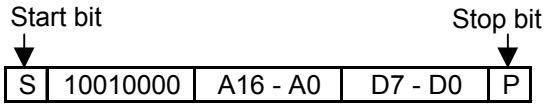
(5) Main block MASS ERASE:

Main block MASS ERASE command is a start bit followed by an 8-bit opcode (A[24:17]=01100000) and a 17-bit address (A[16:0]). A16 to A0 are DON'T CARE. After receiving main block MASS ERASE command, a specified interval (t_{ERASE}) is needed to erase the main block of the FLASH. Then, a stop bit terminates the command.



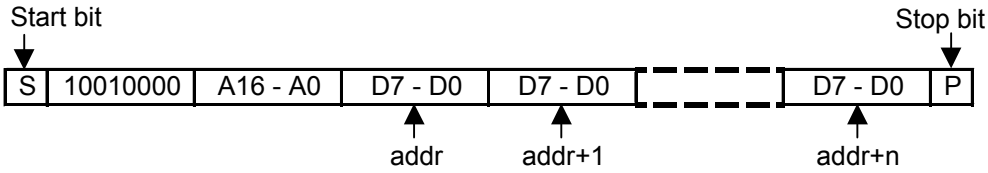
(6) Information block READ:

The command is the same as main block READ except the opcode changes to (10010000) and the active region changes to information block.



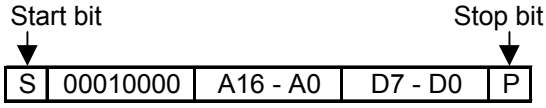
(7) Information block READ with auto-address-count:

The command is the same as main block READ with auto-count except the opcode changes to (10010000) and the active region changes to information block.



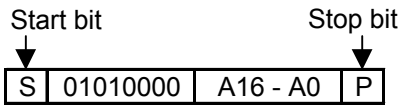
(8) Information block BYTE PROGRAM:

The command is the same as main block BYTE PROGRAM except the opcode changes to (00010000) and the active region changes to information block.



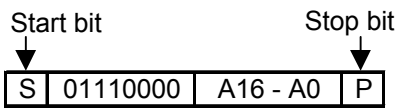
(9) Information block PAGE ERASE:

The command is the same as main block PAGE ERASE except the opcode changes to (01010000) and the active region changes to information block. There is only one page in information block. All of the bits in information block are erased at the same time.



(10) Both blocks MASS ERASE:

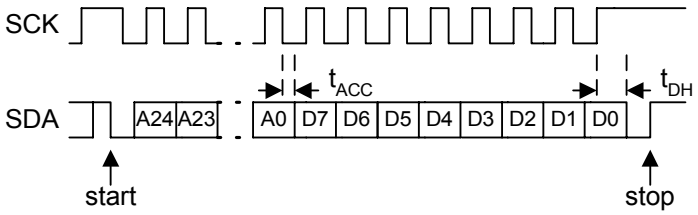
The command is the same as main block MASS ERASE except the opcode changes to (01110000) and both main block and information block will be erased.



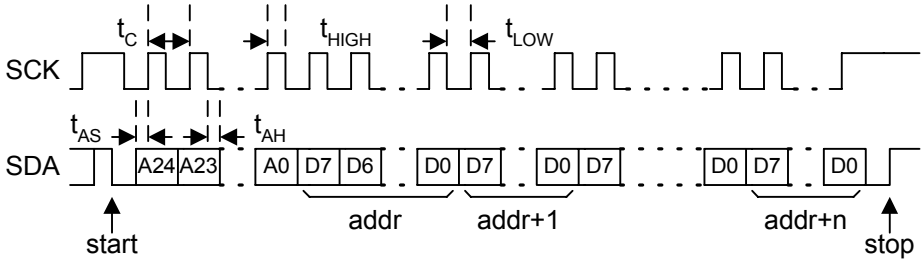
AC CHARACTERISTICS (VDD = 2.7 - 3.6V, T_A = 0 - 70℃)

Characteristic	Symbol	Max.	Min.	Unit
Period of SCL	t_C	-	400	ns
Low period of SCL clock	t_{LOW}	-	170	ns
High period of SCL clock	t_{HIGH}	-	170	ns
Address setup time	t_{AS}	-	100	ns
Address hold time	t_{AH}	-	20	ns
READ access time	t_{ACC}	100	-	ns
READ data hold time	t_{DH}	-	20	ns
PROGRAM data setup time	t_{PDS}	-	100	ns
PROGRAM data hold time	t_{PDH}	-	20	ns
PROGRAM time	t_{PGM}	-	125	us
ERASE time	t_{ERASE}	-	13.5	ms
Rise time of SCL	t_{RSC}	15	-	ns
Fall time of SCL	t_{FCL}	15	-	ns
Rise time of SDA	t_{RDA}	15	-	ns
Fall time of SDA	t_{FDa}	15	-	ns

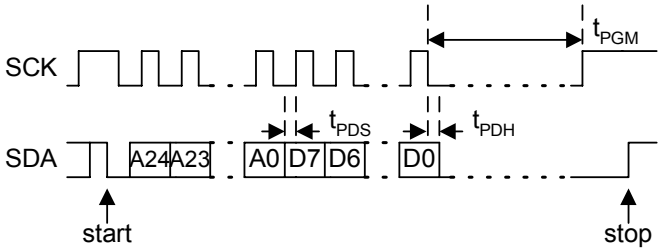
READ COMMAND



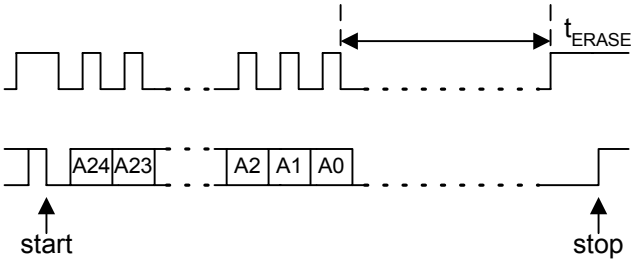
READ COMMAND WITH AUTO-ADDRESS-COUNT



PROGRAM COMMAND

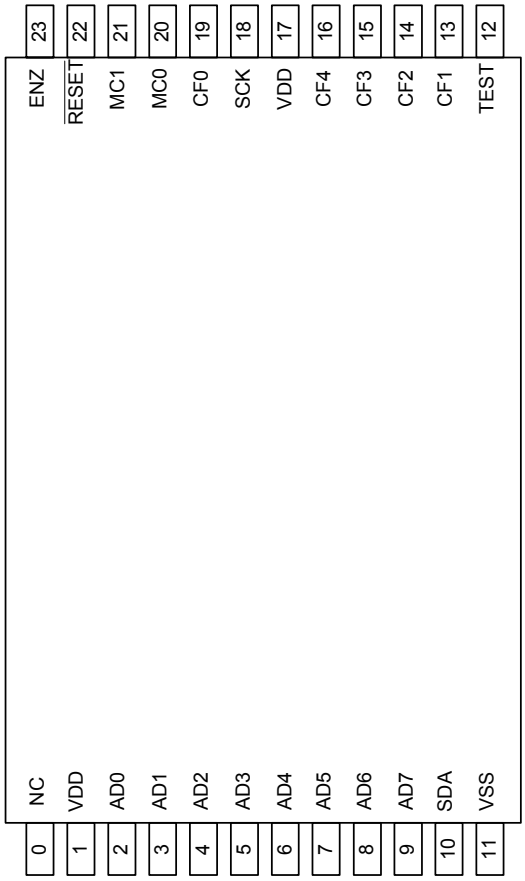


PAGE ERASE AND MASS ERASE COMMAND



PAD ASSIGNMENT AND LOCATIONS

■ PAD ASSIGNMENT



Chip Size: 1590μm x 3110μm

This IC substrate should be connected to VSS

Note: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Ordering Information

Product Number	Package Type
SPR1024A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance to supply the best possible product.

■ PAD LOCATIONS

Pad No	Pad Name	X	Y
0	NC	-718	-1455
1	VDD	-559	-1445
2	AD0	-439	-1445
3	AD1	-319	-1445
4	AD2	-199	-1445
5	AD3	-79	-1445
6	AD4	41	-1445
7	AD5	161	-1445
8	AD6	281	-1445
9	AD7	401	-1445
10	SDA	521	-1445
11	VSS	641	-1445
12	TEST	635	1444
13	CF1	515	1444
14	CF2	395	1444
15	CF3	275	1444
16	CF4	155	1444
17	VDD	35	1444
18	SCK	-85	1444
19	CF0	-205	1444
20	MC0	-325	1444
21	MC1	-445	1444
22	$\overline{\text{RESET}}$	-565	1444
23	ENZ	-685	1444

Note: When bus interface is selected: ENZ, SDA, SCK -> GND, TEST -> NC

When serial interface is selected: AD[7:0], CF[4:3], MC[1:0] -> GND, CF[2:0], ENZ -> VDD, TEST -> NC

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