MOTOROLA

MC13141

Product Preview

Low Power DC - 1.8 GHz LNA and Mixer

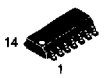
LOW POWER DC – 1.8 GHz LNA AND MIXER

SEMICONDUCTOR TECHNICAL DATA

The MC13141 is intended to be used as a first amplifier and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Local Oscillator amplifier (LO_{amp}), a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide Mixer Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–100 MHz
- Low Power: 7.7 mA @ V_{CC} = 2.7–6.5 V
- High Mixer Linearity: $Pi_{1.0\ dB}$ = –2.0 dBm, IP_{3in} = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} (Not Available in SOIC8) Up to +20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Single–Ended 800 Ω Mixer Output
- Single–Ended 50 Ω LO Input

D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

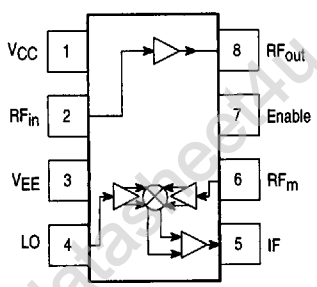
FTB SUFFIX
PLASTIC PACKAGE
CASE 976
(Thin QFP)

ORDERING INFORMATION

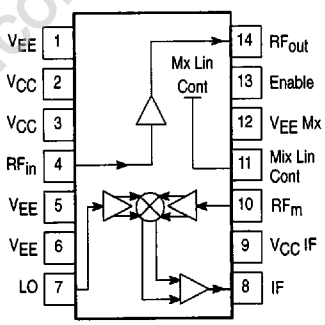
Device	Operating Temperature Range	Package
MC13141D1	T_A = –40° to +85°C	SO–8
MC13141D		SO–14
MC13141FTB		TQFP–20

PIN CONNECTIONS

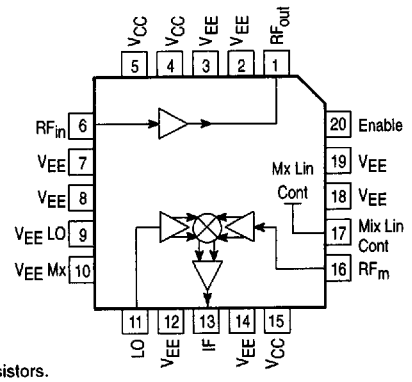
SO–8



SO–14



TQFP–20



This device contains 161 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	2.7–6.5	Vdc

ELECTRICAL CHARACTERISTICS (SOIC8 Package, V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	I_{CC}	–	100	–	pA
Supply Current (Power Up)	I_{CC}	–	7.7	–	mA
Amplifier Gain (50 Ω Insertion Gain)	S21	–	12	–	dB
Amplifier Reverse Isolation	S12	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{-1.0\ dB}$	–	–15	–	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	– 5.0	–	dBm
Amplifier Gain @ N.F. (Application Circuit)	G_{NF}	–	17	–	dB
Amplifier Noise Figure (50 Ω)	NF	–	1.8	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	15	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	7.0	–	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	16.0	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{-1.0\ dBM}$	–	–10	–	dBm
Mixer Input Third Order Intercept	$IP3_{inM}$	–	–3.0	–	dBm
Mixer 3 dB RF Bandwidth	$M_{x-3\ dBBW}$	–	1.8	–	GHz
LO Drive Level	LO_{In}	–	–10	–	dBm
LO Input Match	$\Gamma_{in\ LO}$	–	–20	–	dB
RF_{in} Feedthrough to RF_m	$P_{RFin–RFin}$	–	–13	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–30	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–25	–	dB
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–30	–	dB
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–50	–	dB
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–50	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

8

CIRCUIT DESCRIPTION

General

The MC13141 is a low power LNA, double–balanced mixer. This device is designated for use as the front–end section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto preset or auto program the mixer dynamic range, an enable function and buffered IF output for increased overall gain. Further details are covered in the Pin Function Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the the enable function in which "high" powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. Input and output matching may be achieved at various frequencies using few external components (see Application Circuit). Matching the LNA for maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure. Typical performance at 1.0 GHz is 17 dB gain and 1.8 dB noise figure for Vcc at 3.0 to 5.0 Vdc.

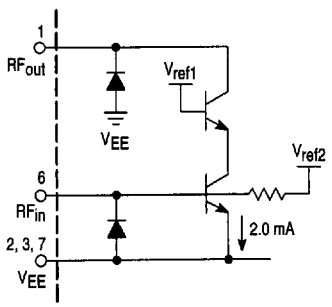
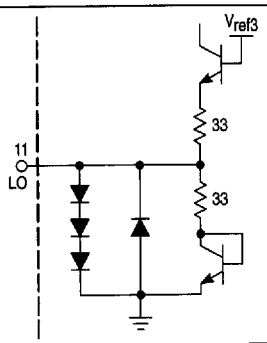
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and IF output buffer amplifier. The linear gain of the mixer is approximately 7.0 dB with a SSB noise figure of 16 dB.

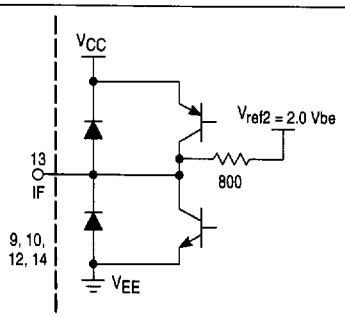
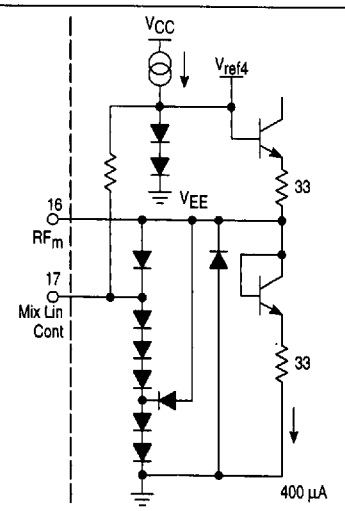
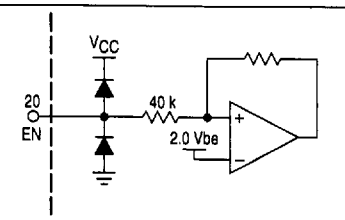
Local Oscillator

It requires an external local oscillator source at –10 dBm input level to maximize the mixer gain.

PIN FUNCTION DESCRIPTION

14 Pin SOIC	20 Pin TQFP	Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Functional Description/External Circuit Requirements
4	6	RF_{in}		**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
2, 3	4, 5	V_{CC}		**V_{CC} – Positive Supply Voltage** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
1, 5	2, 3, 7 and 8	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
14	1	RF_{out}		**RF Output** The output is from the collector of the LNA. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
7	11	LO		**Local Oscillator Input** 50 Ω single–ended buffered LO input.

PIN FUNCTION DESCRIPTION (continued)

14 Pin SOIC	20 Pin TQFP	Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Functional Description/External Circuit Requirements
5, 6	9, 10, 12, 14	V_{EE}		**V_{EE} – Negative Supply** These pins are V_{EE} supply for the IF and LO. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
8	13	IF		**IF Output** The IF is a 800 Ω single–ended output which must be externally matched to 50 Ω for optimal performance.
10	16	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic. The pin dc bias is set at 1.0 Vbe.
11	17	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current). The pin dc bias is set at 2.0 Vbe.
12	18, 19	V_{EE}		**V_{EE} – Negative Supply** These pins are V_{EE} supply for the mixer input.
13	20	EN		**Enable** The device is enabled by pulling up to V_{CC} or greater than 2.0 Vbe.

APPLICATIONS INFORMATION

Evaluation PC Board

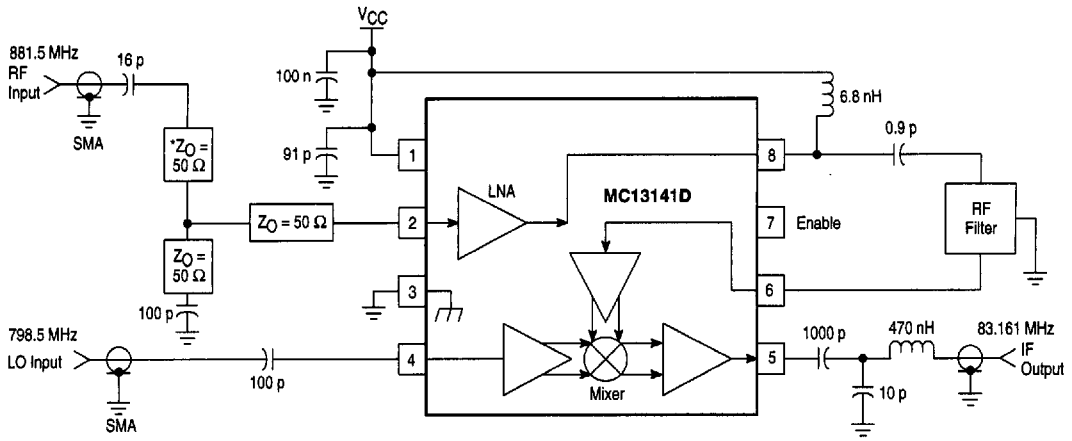
The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give similar results.

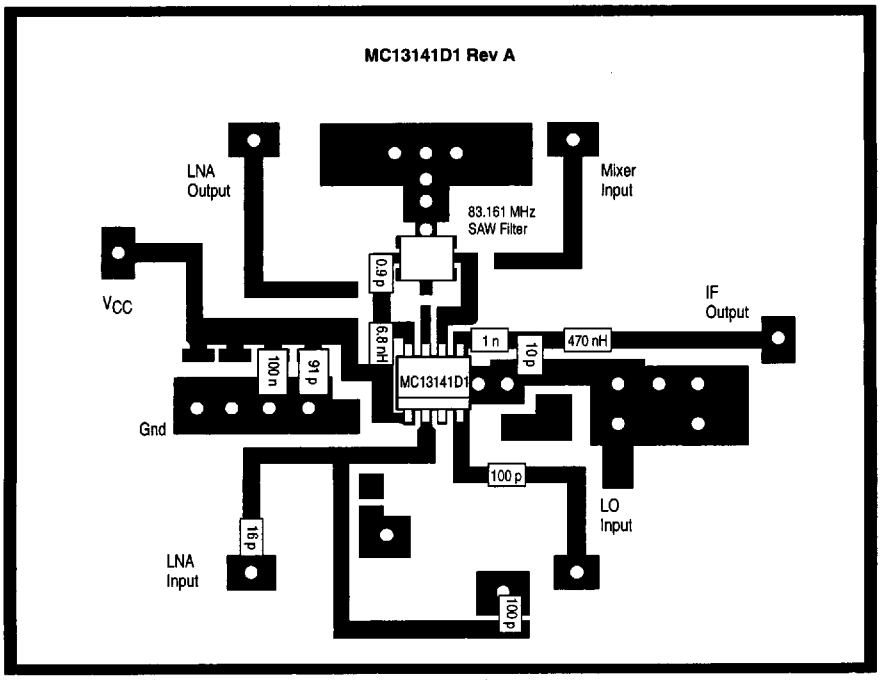
8

Figure 1. MC13141D1 Application Circuit (881.5 MHZ)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. Circuit Side Component Placement View

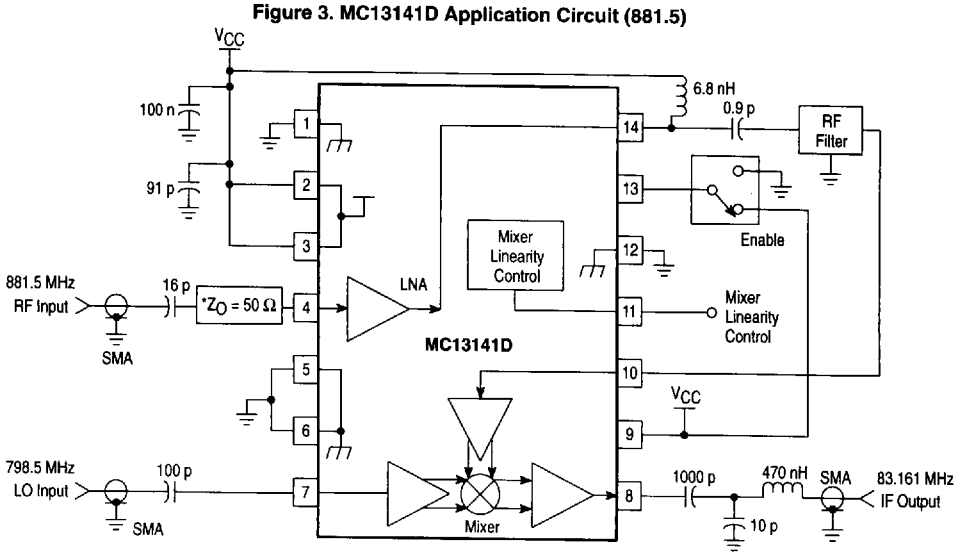


NOTES: 881.5 MHz SAW filter in the ceramic surface mount package is available from several sources: Siemens part # B39881–B4608–Z010 is an example. Other suppliers include Toko and Murata.

The PCB accommodates ceramic dielectric filters for applications in Cellular, DECT, PHS and ISM bands at 902–928 and 2.4–2.5 GHz. Toko makes a full line–up covering the above bands.

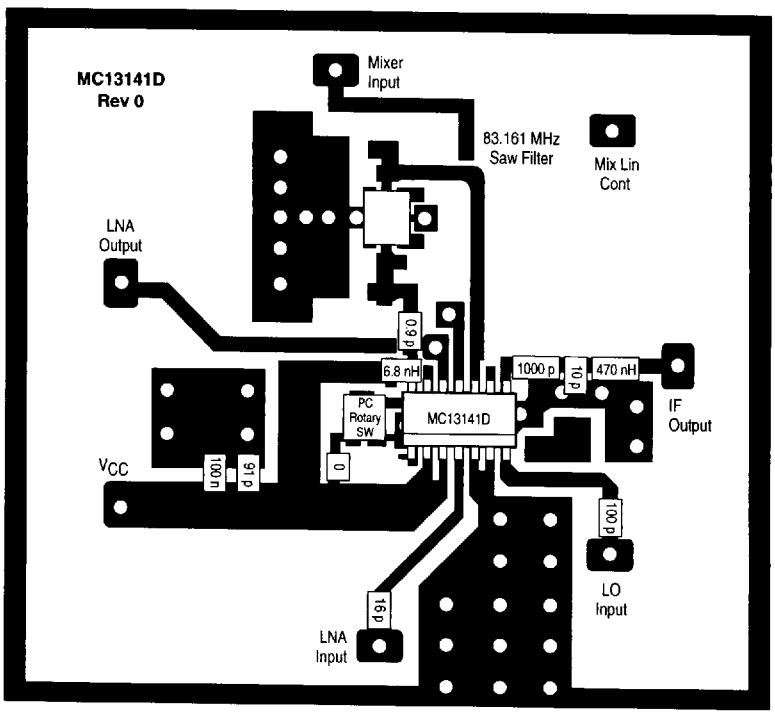
The PCB may be used without an image filter; ac couple the LNA to the mixer. Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used in the 881.5 MHz application circuit. It is necessary to cut a section in the trace before placing the 0.9 pF capacitor. Capacitors should be 0805 size; the 6.8 nH inductor is a Toko type LL2012.

Figure 3. MC13141D Application Circuit (881.5)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 4.

Figure 4. Circuit Side Component Placement View



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Input Matching/Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata. Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

The LNA is conjugately matched to 50 Ω input and output at 3.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 881.5 MHz. The mixer measures 7.0 dB gain and 16 dB noise figure as shown in the application circuit. Typical insertion loss of the Siemens SAW filter is 3.0 dB.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13141 in the front–end receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

$$F_{system} = F1 + [(F2 - 1)/G1] + [(F3 - 1)] / [(G1)(G2)]$$

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$F = Log^{-1}$ [(NF in dB)/10] and similarly

$G = Log^{-1}$ [(Gain in dB)/10]

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51 ; G1 = 50.11
F2 = 1.99 ; G2 = 0.5
F3 = 39.8

Thus, substituting in the equation for subsystem noise factor:

$F_{subsystem}$ = 3.08 ; $NF_{subsystem}$ = 4.9 dB
Overall Subsystem Gain = 21 dB

Figure 5. Front–End Subsystem Block Diagram for Noise Analysis

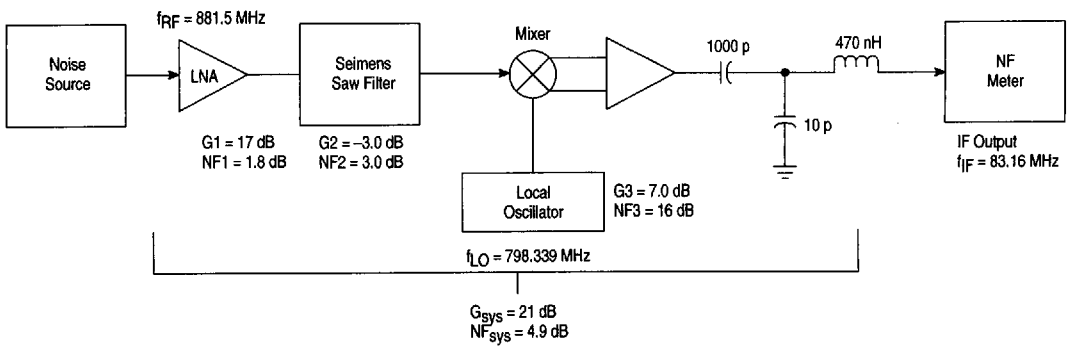

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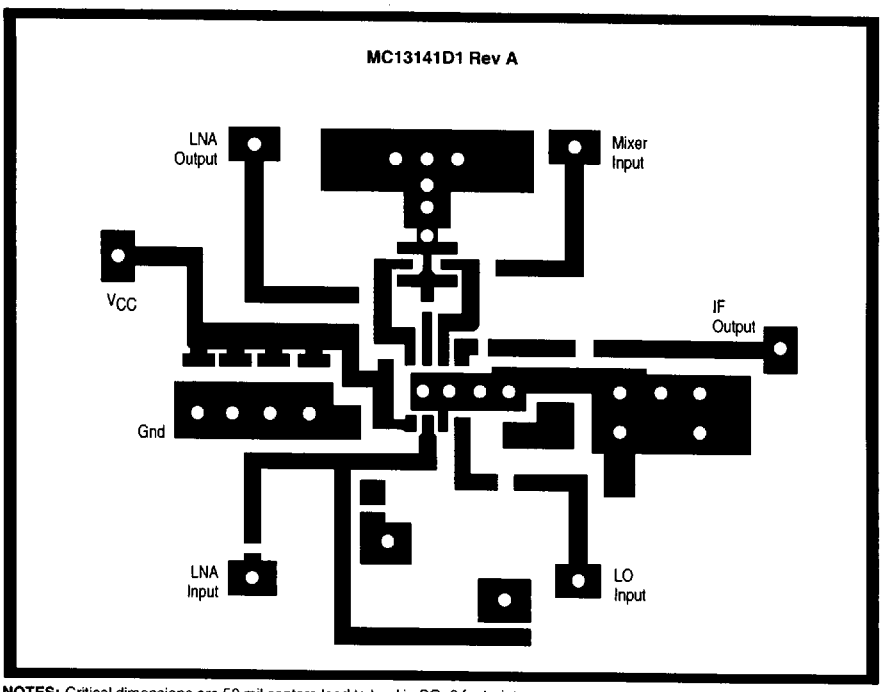
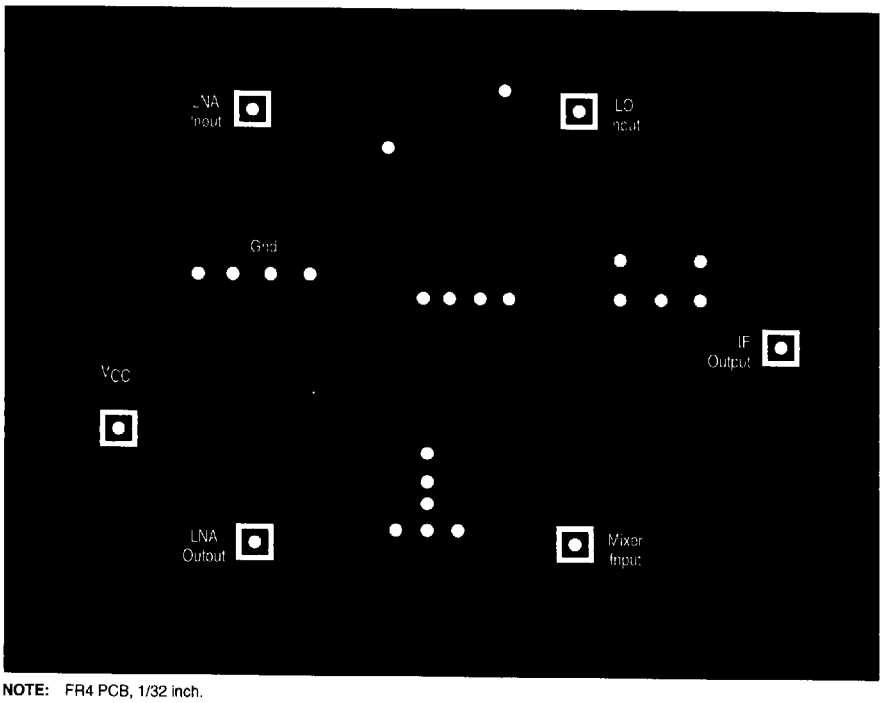
Figure 6. Circuit Side View



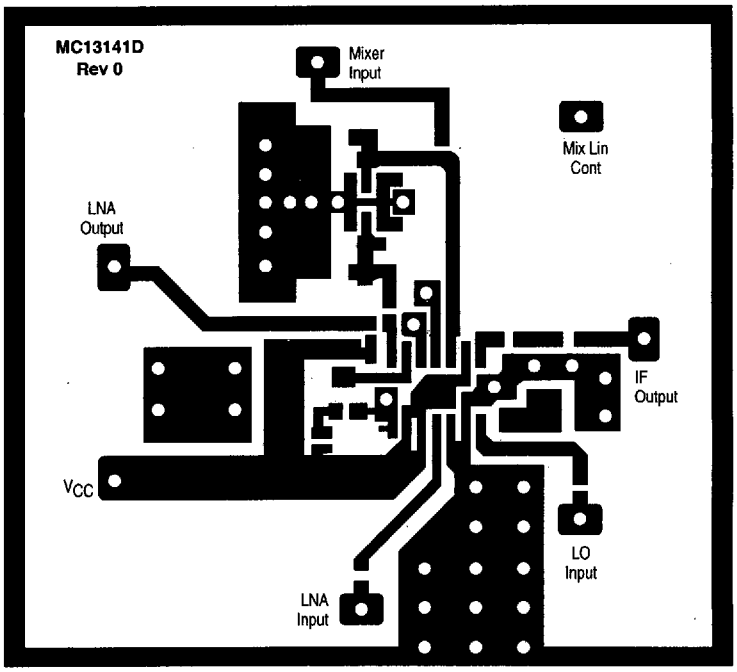
NOTES: Critical dimensions are 50 mil centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 7. MC13141D1 Rev A – Ground Side View



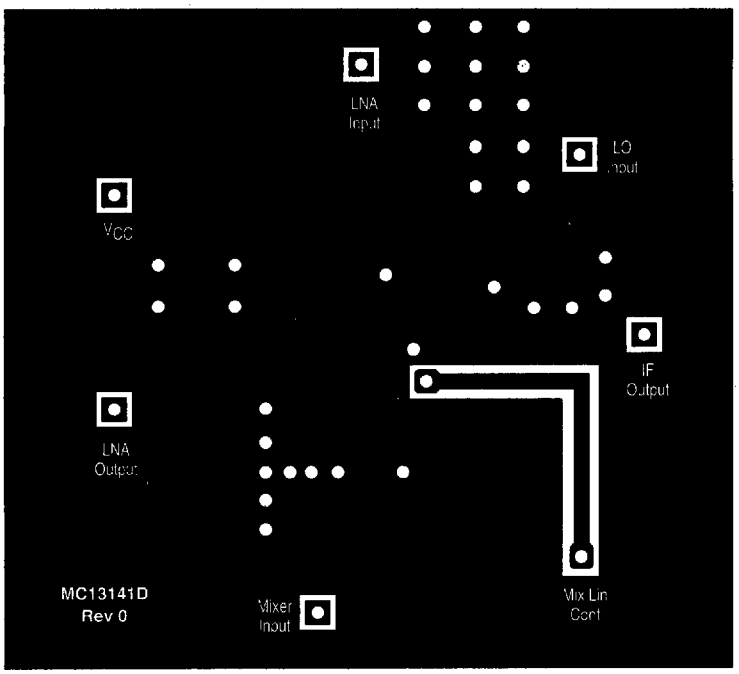
NOTE: FR4 PCB, 1/32 inch.

Figure 8. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–14 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 9. Ground Side View



NOTE: FR4 PCB, 1/32 inch.