

**Document Title****2M x16 bit Super Low Power and Low Voltage Full CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	Initial draft	January 31, 2002	Preliminary
0.1	Revised - Changed Icc2 from 35mA to 40mA for 55ns product from 25mA to 35mA for 70ns product - Changed I <sub>SB1</sub> from 30μA to 40μA - Changed I <sub>DR</sub> from 15μA to 20μA	July 30, 2002	Preliminary
1.0	Finalize	December 18, 2002	Final

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## 2M x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 2M x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs
- Package Type: 55-TBGA-7.50x12.00

### GENERAL DESCRIPTION

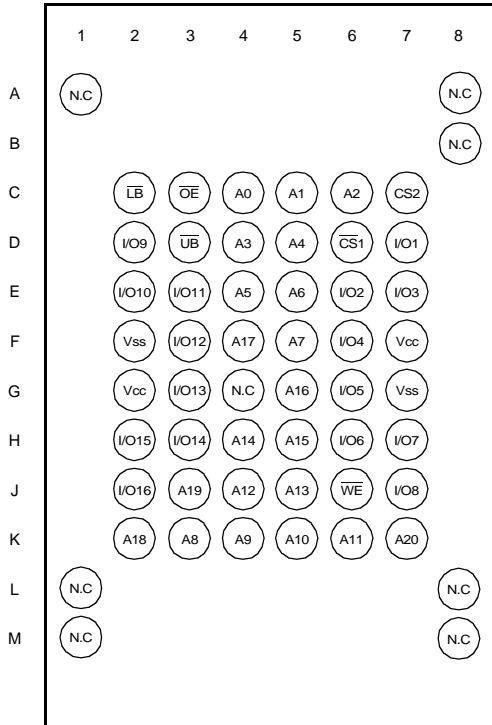
The K6F3216U6M families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max.)	Operating (I <sub>CC1</sub> , Max)	
K6F3216U6M-F	Industrial(-40~85°C)	2.7~3.3V	55 <sup>1)</sup> /70ns	40μA	7mA	55-TBGA-7.50x12.00

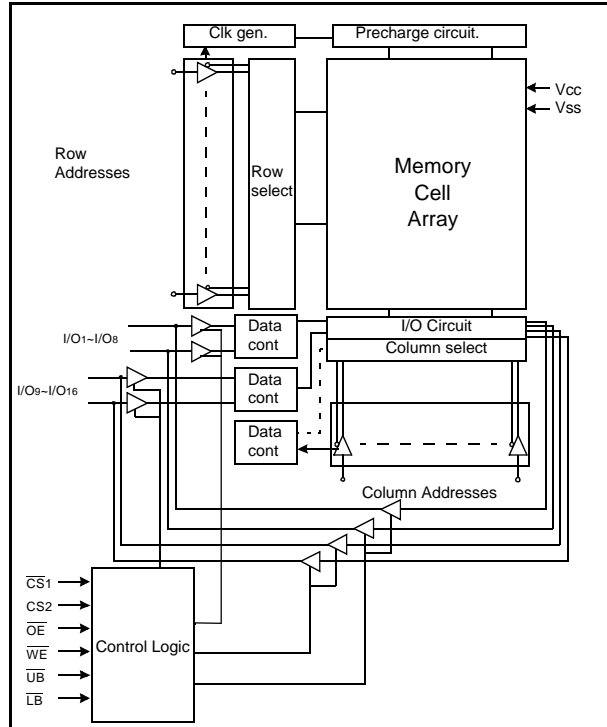
1. The parameter is measured with 30pF test load.

### PIN DESCRIPTION



55-TBGA: Top View (Ball Down)

### FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS1}$ , $CS2$	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O <sub>9-16</sub> )
A <sub>0</sub> -A <sub>20</sub>	Address Inputs	$\overline{LB}$	Lower Byte(I/O <sub>1-8</sub> )
I/O <sub>1</sub> -I/O <sub>16</sub>	Data Inputs/Outputs	N.C	No Connection

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**PRODUCT LIST**

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F3216U6M-EF55 K6F3216U6M-EF70	55-TBGA, 55ns, 3.0V 55-TBGA, 70ns, 3.0V

**FUNCTIONAL DESCRIPTION**

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O <sub>1-8</sub>	I/O <sub>9-16</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X <sup>1)</sup>	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X <sup>1)</sup>	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X <sup>1)</sup>	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X <sup>1)</sup>	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

**ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>**

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.2 to V <sub>CC</sub> +0.3V(Max. 3.6V)	V
Voltage on V <sub>CC</sub> supply relative to Vss	V <sub>CC</sub>	-0.2 to 3.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended period may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.3	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.3 <sup>3)</sup>	-	0.6	V

Note:

1. T<sub>A</sub>=-40 to 85°C, otherwise specified
2. Overshoot: V<sub>CC</sub>+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and Undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ <sup>1)</sup>	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1 \leq 0.2V$ , $\overline{LB} \leq 0.2V$ or/and $\overline{UB} \leq 0.2V$ , $CS_2 \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	7	mA
	I <sub>CC2</sub>	Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	70ns 55ns	- -	35 40	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	-	-	V
Standby Current (CMOS)	I <sub>SB1</sub>	Other input =0~V <sub>CC</sub> 1) $\overline{CS}_1 \geq V_{CC}-0.2V$ , $CS_2 \geq V_{CC}-0.2V$ ( $\overline{CS}_1$ controlled) or 2) $0V \leq CS_2 \leq 0.2V$ ( $CS_2$ controlled)	-	-	40	μA

1. Typical values are measured at V<sub>CC</sub>=3.0V, T<sub>A</sub>=25°C and not 100% tested.

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

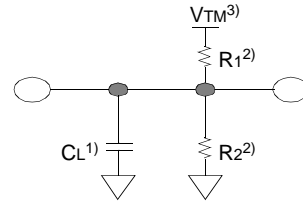
Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right):  $C_L=100\text{pF}+1\text{TTL}$

$C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

2.  $R_1=3070\Omega$ ,  $R_2=3150\Omega$

3.  $V_{TM}=2.8\text{V}$

## AC CHARACTERISTICS ( $V_{CC}=2.7\sim 3.3\text{V}$ , Industrial product: $T_A=-40$ to $85^\circ\text{C}$ )

Parameter List		Symbol	Speed				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	ns
	Chip select to output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	55	-	70	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ valid to data output	t <sub>BA</sub>	-	55	-	70	ns
	Chip select to low-Z output	t <sub>LZ1</sub> , t <sub>LZ2</sub>	10	-	10	-	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ enable to low-Z output	t <sub>BLZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ1</sub> , t <sub>HZ2</sub>	0	20	0	25	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ disable to high-Z output	t <sub>BHZ</sub>	0	20	0	25	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	20	0	25	ns
Output hold from address change	t <sub>OH</sub>	10	-	10	-	ns	
Write	Write cycle time	t <sub>WC</sub>	55	-	70	-	ns
	Chip select to end of write	t <sub>CW1</sub> , t <sub>CW2</sub>	45	-	60	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Valid to End of Write	t <sub>BW</sub>	45	-	60	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	50	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	20	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns

## DATA RETENTION CHARACTERISTICS

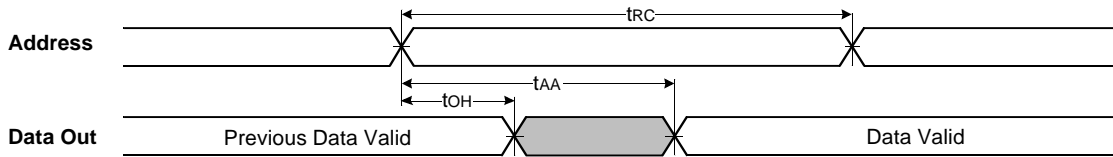
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	VDR	$\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{(1)}$ , $V_{IN} \geq 0\text{V}$	1.5	-	3.3	V
Data retention current	IDR	$V_{CC}=1.5\text{V}$ , $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{(1)}$ , $V_{IN} \geq 0\text{V}$	-	-	20	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ns
Recovery time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

1. 1)  $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}$ ,  $\text{CS}_2 \geq V_{CC}-0.2\text{V}$  ( $\overline{\text{CS}}_1$  controlled) or

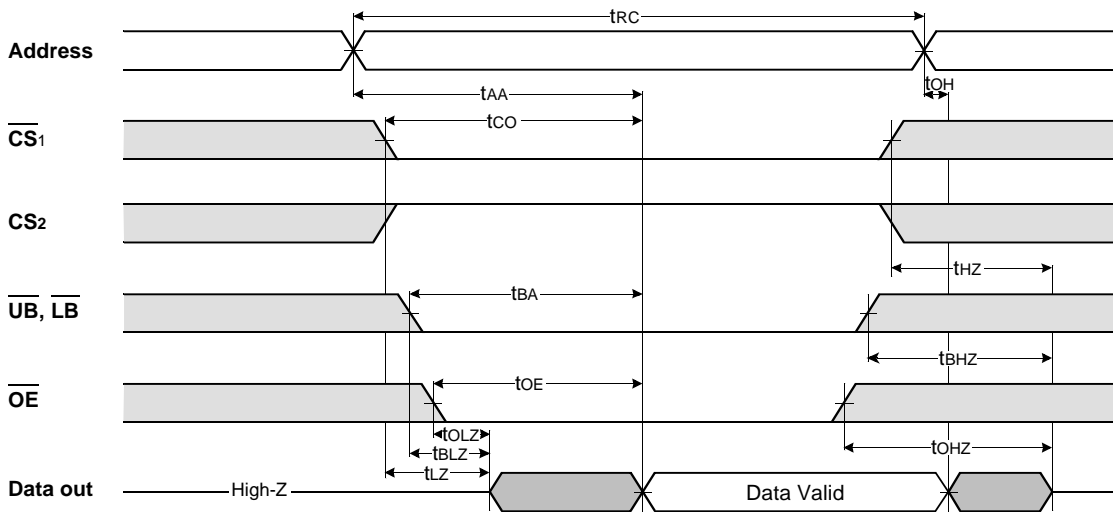
2)  $0 \leq \text{CS}_2 \leq 0.2\text{V}$  ( $\text{CS}_2$  controlled)

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



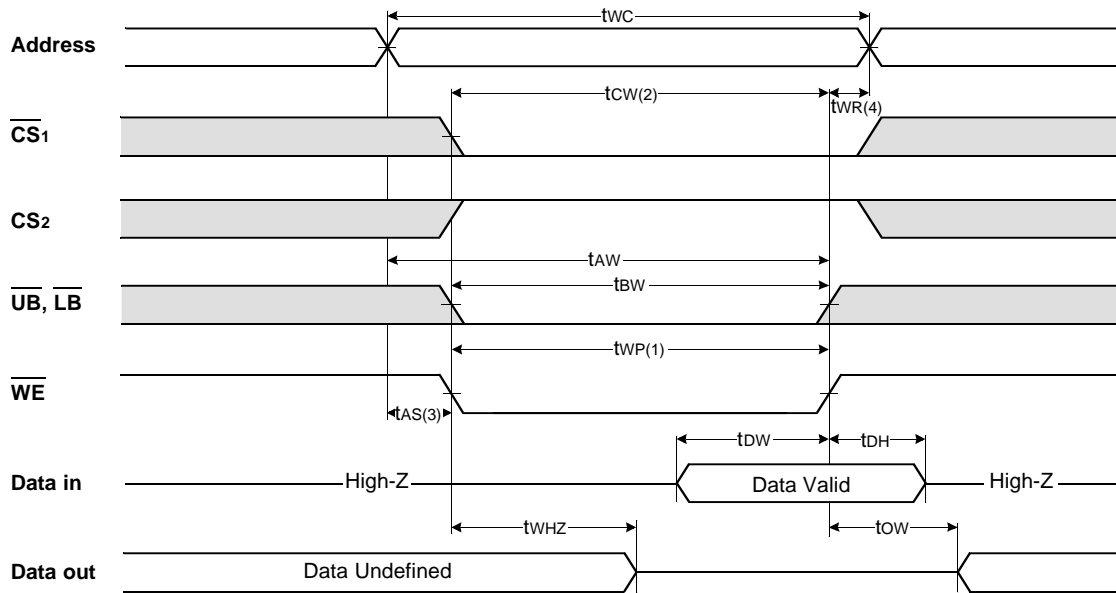
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



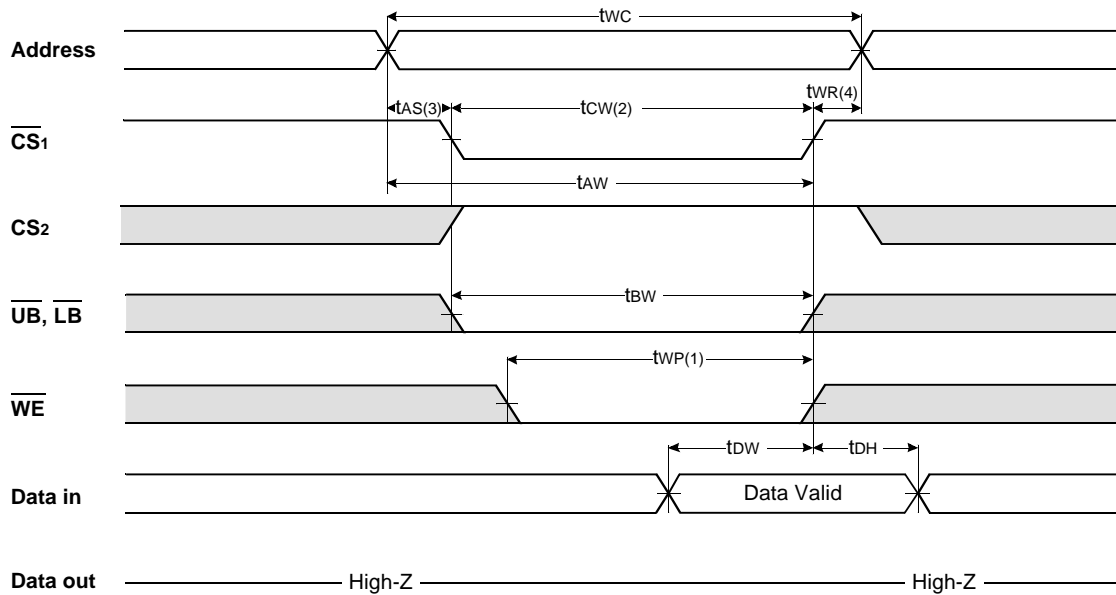
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

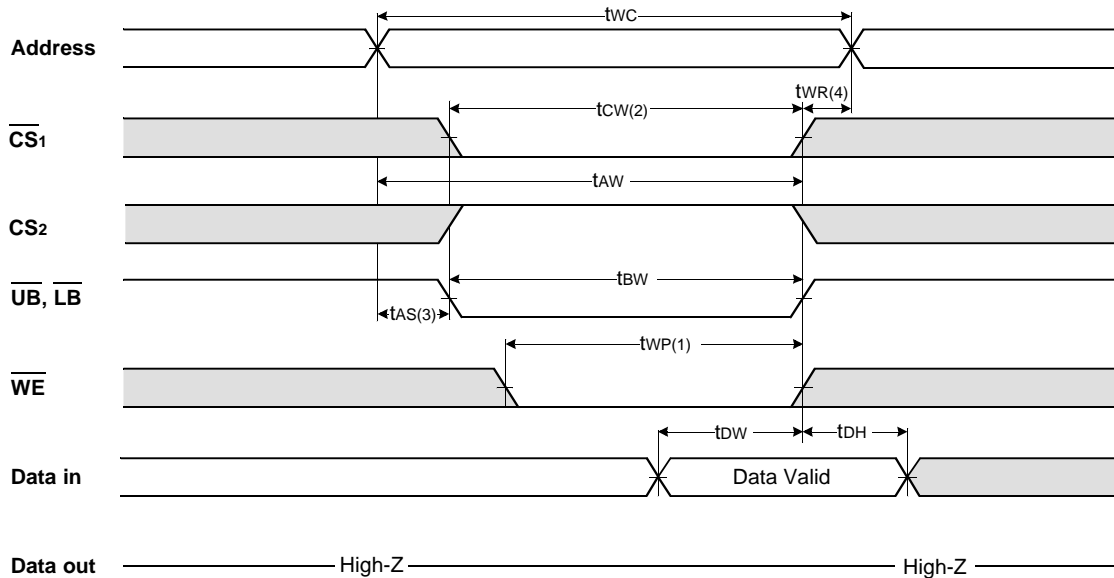
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)

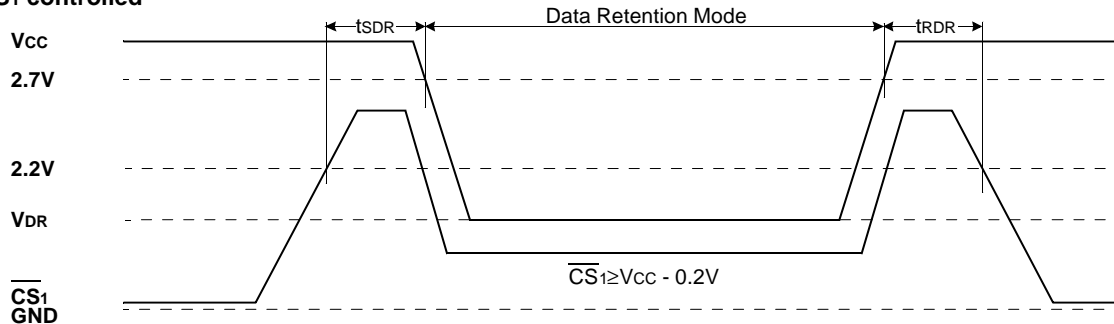


NOTES (WRITE CYCLE)

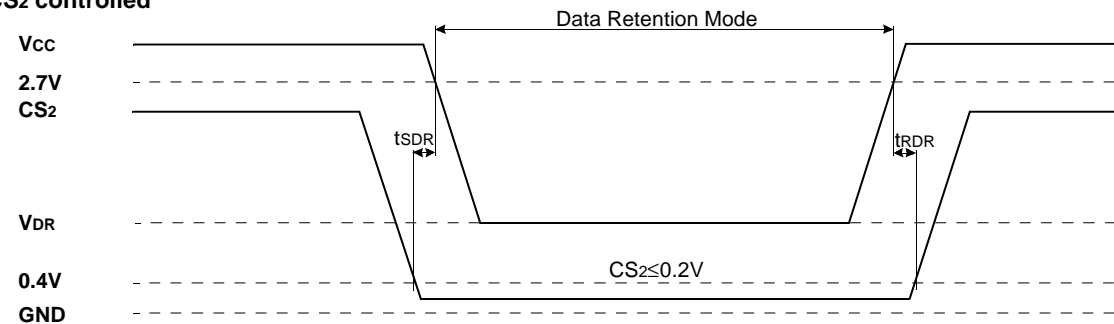
1. A write occurs during the overlap ( $t_{WP}$ ) of low  $\overline{CS1}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS1}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS1}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS1}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends with  $\overline{CS1}$  or  $\overline{WE}$  going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$  controlled



$CS2$  controlled

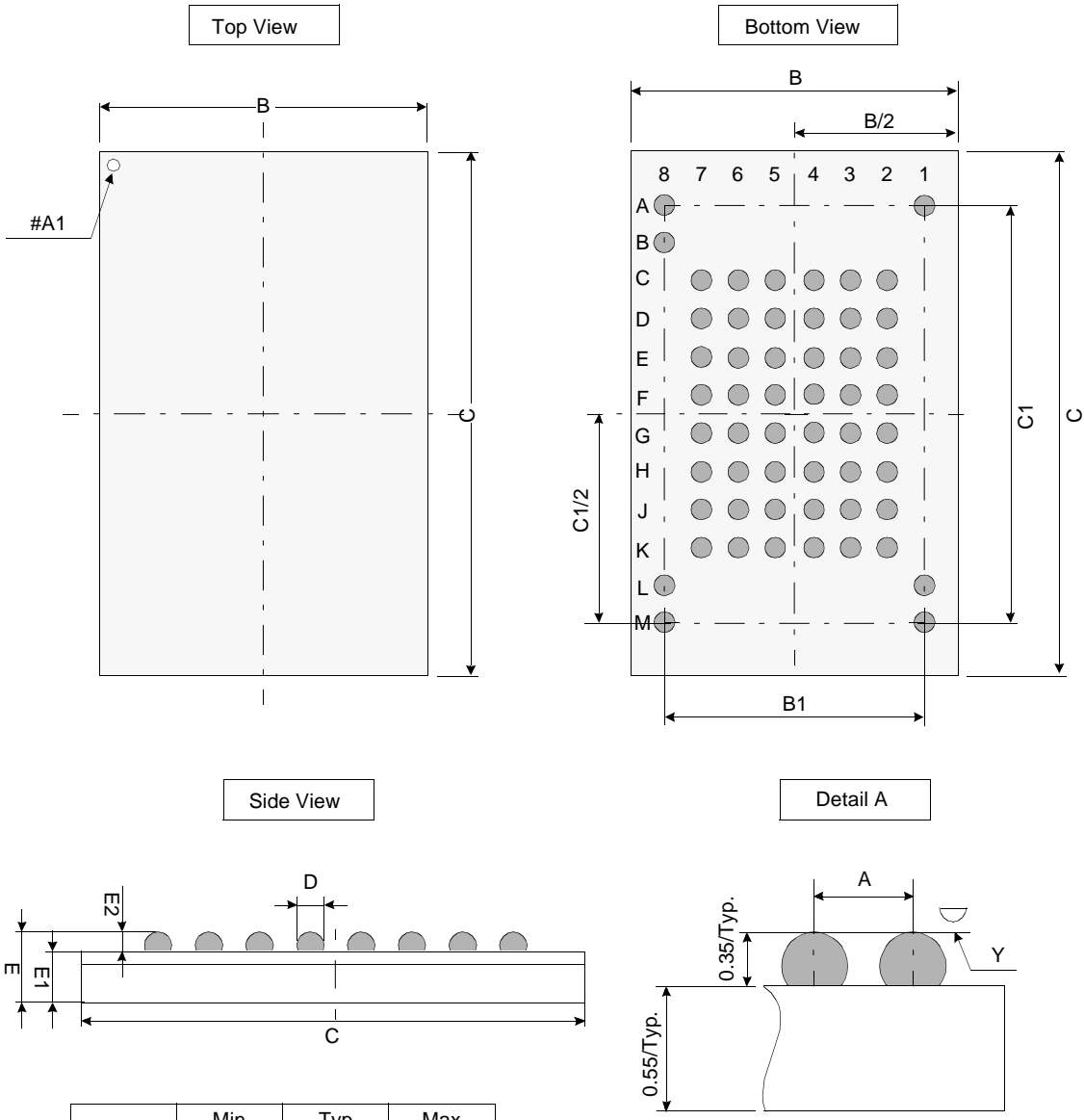




## PACKAGE DIMENSION

Unit: millimeters

55 BALL TAPE BALL GRID ARRAY(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	7.40	7.50	7.60
B1	-	5.25	-
C	11.90	12.00	12.10
C1	-	8.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

**Notes.**

1. Bump counts: 55(12 row x 8 column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are  $\pm 0.050$  unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)