intersil

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HA-5104/883 or 5962-8850201

HA-5134/883

July 2001

Precision Quad Operational Amplifier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Offset Voltage (+25°C). . . . . .200µV (Max)**
  (Full Temp.) . . . . .350µV (Max)
- **Low Offset Voltage Drift at Temp. . . . . 2µV/°C (Max)**
- **Offset Voltage Match . . . . .350µV (Max)**
- **High Channel Separation . . . . .120dB (Min)**
- **Low Noise (f ≥ 100Hz) . . . . 10nV/√Hz (Max)**
- **Wide Bandwidth . . . . .4MHz (Typ)**
- **High CMRR/PSRR .100dB (Min)**
- **High Voltage Gain . . . . 800kV/V (Min)**
- **Dielectric Isolation**

Applications

- **Instrumentation Amplifiers**
- **State-Variable Filters**
- **Precision Integrators**
- **Threshold Detectors**
- **Precision Data Acquisition Systems**
- **Low-Level Transducer Amplifiers**

Description

The HA-5134/883 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741/883. Each amplifier features guaranteed maximum values for offset voltage of 350µV, offset voltage drift of 2µV/°C (max), and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and open loop gain is guaranteed above 500kV/V from -55°C to +125°C. Room temperature specifications exceed these values such as an offset voltage matching specification between channels of 200µV (max) at +25°C.

Precision performance of the HA-5134/883 is enhanced by a noise voltage density of 7nV/√Hz at 1kHz (typ), noise current density of 2pA/√Hz at 1kHz and channel separation of 120dB (min). Each of the four unity gain stable amps on the quad are electrically isolated, having only supply lines in common and are fabricated using Dielectric Isolation to insure quality performance in the most demanding applications.

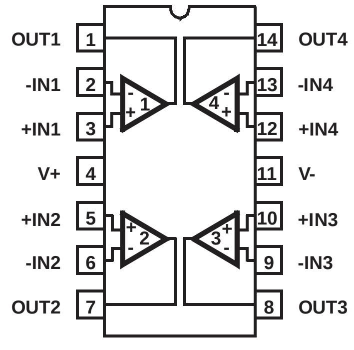
The HA-5134/883 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low level transducer amplifiers. Other applications include precision data acquisition systems, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

Part Number Information

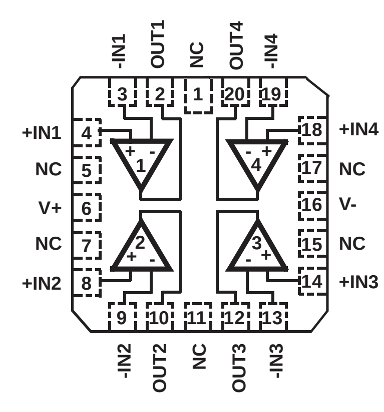
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5134/883	-55°C to +125°C	14 Lead CerDIP
HA4-5134/883	-55°C to +125°C	20 Lead Ceramic LCC

Pinouts

HA-5134/883
(CERDIP)
TOP VIEW



HA-5134/883
(CLCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 6V
Voltage at Either Input Terminal . . . . V+ to V-
Input Current. 25mA
Output Current .Full Short Circuit Protection
Output Current Duration . . . . Indefinite
(One Amplifier Shorted to Ground)
Junction Temperature. . . . . +175^{o}C
Storage Temperature Range . . . . -65^{o}C to +150^{o}C
ESD Rating. . . . . <2000V
Lead Temperature (Soldering 10s) . . . . +300^{o}C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	75^{o}C/W	20^{o}C/W
Ceramic LCC Package	65^{o}C/W	15^{o}C/W

Package Power Dissipation Limit at +75^{o}C for $T_J \leq$ +175^{o}C
CerDIP Package 1.33W
Ceramic LCC Package 1.54W
Package Power Dissipation Derating Factor Above +75^{o}C
CerDIP Package . . . . 13.3mW/^{o}C
Ceramic LCC Package . . . . 15.4mW/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range. . . . . -55^{o}C to +125^{o}C
Operating Supply Voltage . . . . ±15V
$V_{INCM} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 2kΩ

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25^{o}C	-200	200	µV
			2, 3	+125^{o}C, -55^{o}C	-350	350	µV
Offset Voltage Match	ΔV_{IO}	$\lvert V_{IO}$ (Max) - V_{IO} (Min)$\rvert$	1	+25^{o}C	-	200	µV
			2, 3	+125^{o}C, -55^{o}C	-	350	µV
Input Bias Current	$+I_B$	V_{CM} = 0V, $+R_S$ = 10kΩ, $-R_S$ = 50Ω	1	+25^{o}C	-50	50	nA
			2, 3	+125^{o}C, -55^{o}C	-75	75	nA
	$-I_B$	V_{CM} = 0V, $+R_S$ = 50Ω, $-R_S$ = 10kΩ	1	+25^{o}C	-50	50	nA
			2, 3	+125^{o}C, -55^{o}C	-75	75	nA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S$ = 10kΩ, $-R_S$ = 10kΩ	1	+25^{o}C	-50	50	nA
			2, 3	+125^{o}C, -55^{o}C	-75	75	nA
Common Mode Range	+CMR	V+ = +5V, V- = -25V	1	+25^{o}C	10	-	V
			2, 3	+125^{o}C, -55^{o}C	10	-	V
	-CMR	V+ = +25V, V- = -5V	1	+25^{o}C	-	-10	V
			2, 3	+125^{o}C, -55^{o}C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, R_L = 2kΩ	4	+25^{o}C	800	-	kV/V
			5, 6	+125^{o}C, -55^{o}C	500	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, R_L = 2kΩ	4	+25^{o}C	800	-	kV/V
			5, 6	+125^{o}C, -55^{o}C	500	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = 10V, V+ = +5V, V- = -25V, V_{OUT} = -10V	1	+25^{o}C	100	-	dB
			2, 3	+125^{o}C, -55^{o}C	94	-	dB
	-CMRR	ΔV_{CM} = 10V, V+ = +25V, V- = -5V, V_{OUT} = +10V	1	+25^{o}C	100	-	dB
			2, 3	+125^{o}C, -55^{o}C	94	-	dB
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25^{o}C	12	-	V
			5, 6	+125^{o}C, -55^{o}C	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25^{o}C	-	-12	V
			5, 6	+125^{o}C, -55^{o}C	-	-12	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	15	-	mA
			5, 6	+125°C, -55°C	8	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-15	mA
			5, 6	+125°C, -55°C	-	-8	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	6.8	mA
			2, 3	+125°C, -55°C	-	8	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	6.8	mA
			2, 3	+125°C, -55°C	-	8	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V, V+ = +20V, V- = -15V V+ = +10V, V- = -15V	1	+25°C	100	-	dB
			2, 3	+125°C, -55°C	94	-	dB
	-PSRR	ΔV_{SUP} = 10V, V+ = +15V, V- = -20V V+ = +15V, V- = -10V	1	+25°C	100	-	dB
			2, 3	+125°C, -55°C	94	-	dB

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	+25°C	0.75	-	V/µs
	-SR	V_{OUT} = +3V to -3V	7	+25°C	0.75	-	V/µs
Rise and Fall Time	t_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	400	ns
	t_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	400	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	2	µV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	20	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{NP-P}	0.1Hz to 10Hz	1	+25°C	-	0.25	μV_{P-P}
Input Noise Voltage Density	E_N	R_S = 20Ω, f_O = 1kHz	1	+25°C	-	10	nV/√Hz
Input Noise Current Density	I_N	R_S = 2MΩ, f_O = 1kHz	1	+25°C	-	2	pA/√Hz

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Gain Bandwidth Product	GBWP	V_O = 200mV, $f_O \geq$ 100kHz	1	+25°C	3	-	MHz
Unity Bandwidth Product	UBWP	V_O = 200mV	1	+25°C	3	-	MHz
Slew Rate	+SR	V_{OUT} = -3V to +3V	1	+25°C to +125°C	0.75	-	V/µs
	-SR	V_{OUT} = +3V to -3V	1	-55°C	0.6	-	V/µs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	12	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Rise and Fall Time	t_R	V_{OUT} = 0V to +200mV	1, 4	-55°C to +125°C	-	400	ns
	t_F	V_{OUT} = 0V to -200mV	1, 4	-55°C to +125°C	-	400	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	-55°C to +125°C	-	40	%
	-OS	V_{OUT} = 0V to -200mV	1	-55°C to +125°C	-	40	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	86	Ω
Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	240	mW
Channel Separation (AC)	CS (AC)	V_{IN} = 1V_{P-P}, f_O = 100Hz	1	+25°C	120	-	dB
		V_{IN} = 1V_{P-P}, f_O = 10kHz	1	+25°C	120	-	dB
Channel Separation (DC)	CS (DC)	V_O = ±10V (20V_{P-P}), $\Delta V_{IO} \leq$ 20µV	1	+25°C	120	-	dB

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πV_{PEAK}).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.).
4. Measured between 10% and 90% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
91 x 114 x 19 mils ± 1 mils
2300 x 2900 x 483µm ± 25.4µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si3N4) over Silox (SIO2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
$2.5 \times 10^5 A/cm^2$
This device meets Glassivation Integrity Test Requirement
per MIL-STD-883 Method 2021 and MIL-I-38535 Paragraph 30.5.5.4.

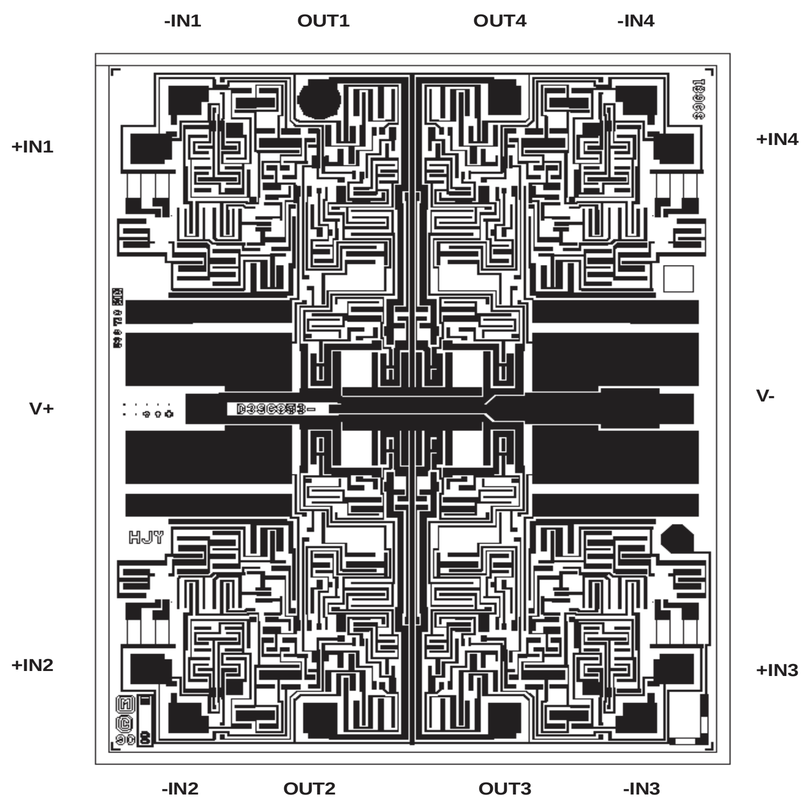
SUBSTRATE POTENTIAL (Powered Up):
Unbiased

TRANSISTOR COUNT: 160

PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5134/883



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