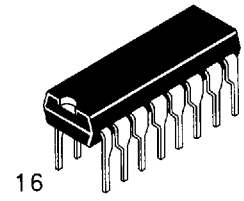
Available Q3, 1995

Hex D Flip-Flop with Master Reset

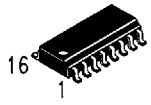
DV74AC174
DV74ACT174

This device is a high speed hex D flip-flop. It is primarily used as a 6-bit edge triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH transition. The device has a Master Reset to simultaneously clear all flip-flops.

- **Advanced very high speed CMOS**
- **Outputs source/sink 24 mA**
- **Transmission line driving 50 ohms**
- **ACT has TTL compatible inputs**
- **Operation from 2 to 6 volts guaranteed**
- **DC & AC Parameters guaranteed over –40 to +85°C**

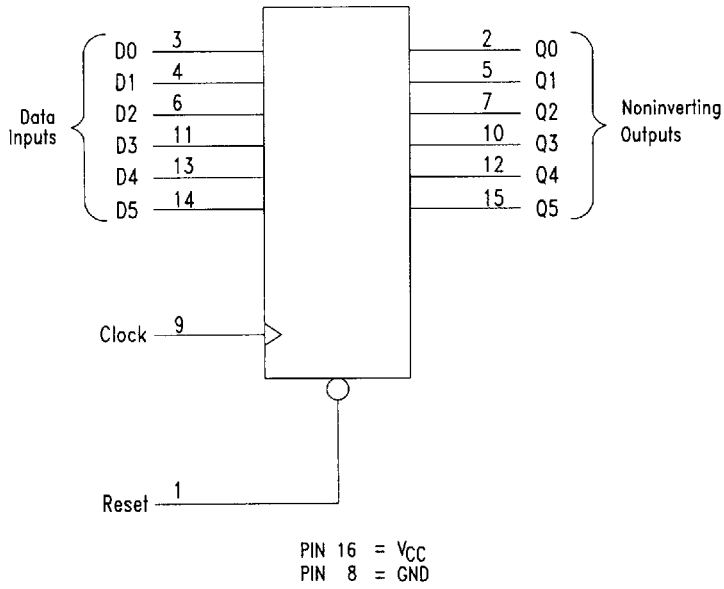


N Suffix
Plastic DIP
AVG-003 Case



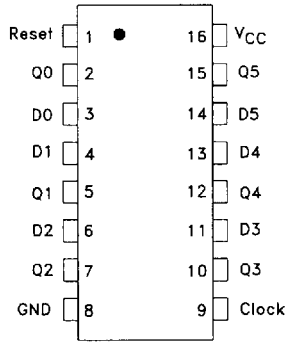
D Suffix
Plastic SOP
AVG-004 Case

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



TRUTH TABLE

Inputs			Output
Reset	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

H=HIGH Voltage Level
L=LOW Voltage Level
X=Either Low or High Logic Level
↑=LOW to HIGH transition of Clock

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	AC174, ACT174	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{STG}	Storage Temperature	– 65 to +150	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage, (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) **'AC** Devices except Schmitt Inputs	V_{CC} @ 3.0 V			150	ns/V
		V_{CC} @ 4.5 V			40	ns/V
		V_{CC} @ 5.5 V			25	ns/V
t_r, t_f	Input Rise and Fall Time (Note 2) **'ACT** Devices except Schmitt Inputs	V_{CC} @ 4.5 V			10	ns/V
		V_{CC} @ 5.5 V			8.0	ns/V
T_A	Operating Ambient Temperature Range		–40		85	°C
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0 V		85		pF
C_{IN}	Input Capacitance V_{CC} = 5.0 V	V_{CC} = 5.0 V		4.5		pF

1. V_{IN} from 30% to 70% V_{CC}
2. V_{IN} from 0.8 to 2.0 V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Vcc (V)	74AC			Unit
				T_A = +25°C		T_A = –40 to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = –50 µA	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V
		V_{IN} = V_{IL} or V_{IH} –12mA I_{OH} –24mA –24 mA	3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V
V_{OL}	MaximumLow Level Output Voltage	I_{OUT} = 50 µA	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IL} or V_{IH} 12mA I_{OH} 24mA 24 mA	3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	VI=V_{CC}, GND	5.5		±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		8.0	80	µA

AC CHARACTERISTICS

Symbol	Parameter (C_L = 50 pF)	Vcc ±10% (V)	AC174					Unit
			T_A = +25°C			T_A = – 40°C to +85°C		
			Min	Typ	Max	Min	Max	
fmax	Maximum Clock Frequency	3.3 5.0	90 100	100 125		70 100		MHz
t_{PLH}	Propagation Delay Clock to Q_n	3.3 5.0	2.0 1.5	9.0 6.0	11.5 8.5	1.5 1.0	12.5 9.5	ns
t_{PHL}		3.3 5.0	2.0 1.5	8.5 6.0	11 8.0	1.5 1.0	12.5 9.0	
t_{PLH}	Propagation Delay Master Reset to Qn	3.3 5.0	2.5 1.5	9.0 7.0	11.5 9.0	2.0 1.5	12.5 10.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter (C_L = 50 pF)	Vcc ±10% (V)	AC174		Unit
			T_A = +25°C	T_A = – 40°C to +85°C	
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW, Dn to Clock	3.3 5.0	6.5 5.0	7.0 5.5	ns
t_h	Hold Time, HIGH or LOW, Dn to Clock	3.3 5.0	3.0 3.0	3.0 3.0	ns
t_w	Master Reset Pulse Width, LOW	3.3 5.0	5.5 5.0	7.0 5.0	ns
t_w	Clock Pulse Width	3.3 5.0	5.5 5.0	7.0 5.0	ns
t_{rec}	Recovery Time, Master Reset to Clock	3.3 5.0	2.5 2.0	2.5 2.0	ns

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DC ELECTRICAL CHARACTERISTICS

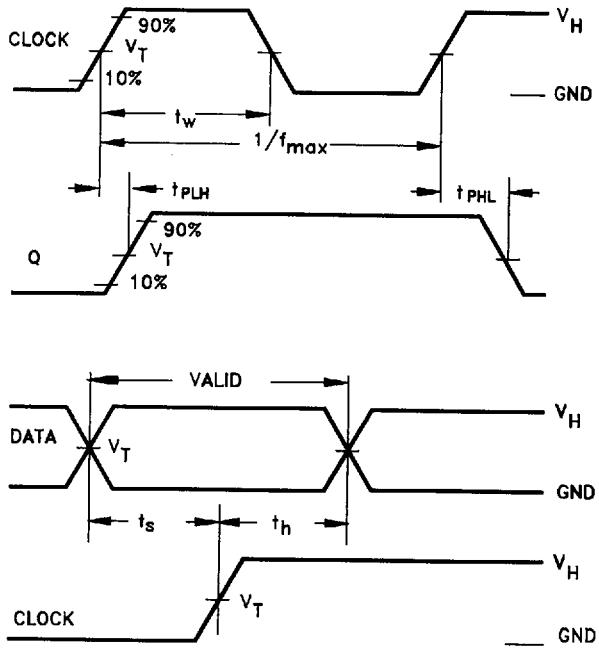
Symbol	Parameter	Conditions	Vcc (V)	ACT174			Unit
				TA = +25°C		TA = –40 to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = –50 µA	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V
		V_{IN} = V_{IL} or V_{IH} I_{OH} –24mA –24 mA	4.5 5.5		3.86 4.86	3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	I_{OUT}= 50 µA	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V
		V_{IN} = V_{IL} or V_{IH} I_{OL} 24mA 24 mA	4.5 5.5		0.36 0.36	0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	V_I=V_{CC}, GND	5.5		±0.1	±1.0	µA
ΔI_{CCT}	Additional Max I_{CC}/Input	V_I=V_{CC} – 2.1 V	5.5	0.6		1.5	mA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		8.0	80	µA

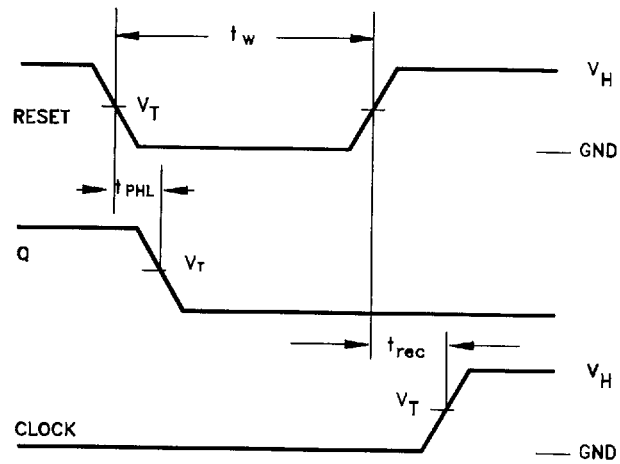
AC CHARACTERISTICS

Symbol	Parameter (C_L = 50 pF)	Vcc ±10% (V)	ACT174				Unit
			T_A = +25°C		T_A = −40°C to +85°C		
			Min	Max	Min	Max	
fmax	Maximum Clock Frequency	5.0	165		140		MHz
t_{PLH}	Propagation Delay, Clock to Q_n	5.0	1.5	10.5	1.5	11.5	ns
t_{PHL}	Propagation Delay, Clock to Q_n	5.0	1.5	10.5	1.5	11.5	ns
t_{PHL}	Propagation Delay, Master Reset to Q_n	5.0	1.5	9.5	1.5	11..0	ns

Symbol	Parameter (C_L = 50 pF)	Vcc ±10% (V)	ACT174		Unit
			T_A = +25°C	T_A = −40°C to +85°C	
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW, Dn to Clock	5.0	1.5	1.5	ns
t_h	Hold Time, HIGH or LOW, Dn to Clock	5.0	2.0	2.0	ns
t_w	Master Reset Pulse Width, LOW	5.0	3.0	3.5	ns
t_w	Clock Pulse Width	5.0	3.0	3.5	ns
t_{rec}	Recovery Time, Master Reset to Clock	5.0	0.5	0.5	ns

SWITCHING WAVEFORMS





Input and output threshold voltage:
V_T = 50% Vcc for AC; 1.5V for ACT
V_H = Vcc for AC, 3V for ACT

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