Programmable Low Power Gyroscope

Preliminary Technical Data

ADIS16250

FEATURES

Yaw rate gyro with digital range scaling
±80°/sec, ±160°/sec, and ±320°/sec settings
14-bit digital gyroscope sensor outputs
12-bit digital temperature sensor output
Calibrated sensitivity and bias
In-system, auto-zero for bias drift calibration
Digitally controlled sample rate
Digitally controlled frequency response
Dual alarm settings with rate/threshold limits
On-board integration for short-term angle estimates
Digitally activated self-test
Digitally activated low power mode
Interrupt-driven wake-up
SPI®-compatible serial interface
Auxiliary 12-bit ADC input and 12-bit DAC output
Auxiliary digital input/output
Single-supply operation: 4.75 V to 5.25 V
2000 *g* powered shock survivability

APPLICATIONS

Instrumentation control
Platform control and stabilization
Motion control and analysis
Avionics instrumentation
Navigation
Image stabilization
Robotics

FUNCTIONAL BLOCK DIAGRAM

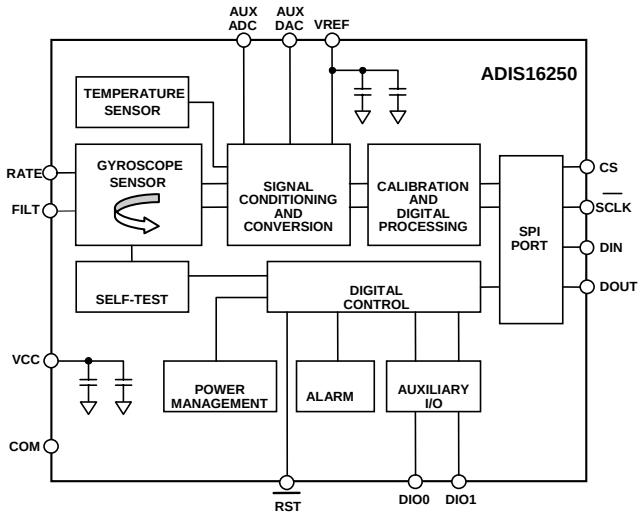

Figure 1.

GENERAL DESCRIPTION

The ADIS16250 is a complete, angular rate measurement system available in a single compact package enabled by Analog Devices' *i*Sensor™ integration. By enhancing Analog Devices' *i*MEMS® sensor technology with an embedded signal processing solution, the ADIS16250 provides factory calibrated and tunable digital sensor data in a convenient format that can be accessed using a simple SPI serial interface. The SPI interface provides access to measurements for the gyroscope, temperature, power supply, and one auxiliary analog input. Easy access to calibrated digital sensor data provides developers with a system-ready device, reducing development time, cost, and program risk.

The device range can be digitally selected from three different settings: ±80°/sec, ±160°/sec, and ±320°/sec. Unique characteristics of the end system are accommodated easily through several built-in features, including an auto-zero recalibration via a single register command, as well as configurable sample rate and frequency response.

Additional features can be used to further reduce system complexity, including a configurable alarm function, an auxiliary 12-bit ADC, an auxiliary 12-bit DAC, a configurable digital I/O port, and a digital self-test function.

System power dissipation can be optimized via the ADIS16250 power management features, including an interrupt-driven wake-up.

The ADIS16250 is available in an 11 mm x 11 mm x 5.5 mm laminate-based land grid array (LGA) package with a temperature range of –40°C to +85°C.

Rev. PrB

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SPECIFICATIONS

T_A = −40°C to +85°C, V_{CC} = 5.0 V, angular rate = 0°/sec, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SENSITIVITY	Clockwise rotation is positive output				
Dynamic Range[1]	Full-scale range	±320			°/sec
Initial[2]	At 25°C, dynamic range = ±320°/sec		13.65		LSB/°/sec
	At 25°C, dynamic range = ±160°/sec		27.3		LSB/°/sec
	At 25°C, dynamic range = ±80°/sec		54.6		LSB/°/sec
Temperature Drift	V_{CC} = 4.75 V to 5.25 V		TBD		ppm/°/sec
Nonlinearity	Best fit straight line		±0.1		% of FS
NULL					
Initial Null			1.0		°/sec
Temperature Drift	V_{CC} = 4.75 V to 5.25 V		TBD		ppm/°C
Turn-On Time	Power on to ±2°/sec of final, no averaging, minimum sample period		150		ms
Linear Acceleration Effect	Any axis		TBD		°/sec/*g*
Voltage Sensitivity	V_{CC} = 4.75 V to 5.25 V, max averaging		TBD		°/sec/V
NOISE PERFORMANCE					
Output Noise	At 25°C, ±320°/sec dynamic range, no filtering		0.5		°/sec rms
	At 25°C, ±160°/sec dynamic range, 4-tap filter		0.3		°/sec rms
	At 25°C, ±80°/sec dynamic range, 16-tap filter		0.15		°/sec rms
Rate Noise Density	At 25°C, f = 25 Hz, no average		0.05		°/sec/√Hz rms
FREQUENCY RESPONSE					
3 dB Bandwidth (User Selectable)	0 nF as comp cap (see Setting Bandwidth)		50		Hz
Sensor Resonant Frequency			14		kHz
SELF-TEST STATE					
Change for Positive Stimulus	Relative to nominal output	+32	+53	+80	°/sec
Change for Negative Stimulus	Relative to nominal output	−32	−53	−80	°/sec
TEMPERATURE SENSOR					
Output at 25°C			0		LSB
Scale Factor			+6.88		LSB/°C
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		2.5	V
Input Capacitance	During acquisition		20		pF
ON-CHIP VOLTAGE REFERENCE			2.5		V
Accuracy	At 25°C	−10		+10	mV
Reference Temperature Coefficient			±40		ppm/°K
Output Impedance			70		Ω
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		4		LSB
Differential Nonlinearity			1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range			0 to 2.5		V

Parameter	Conditions	Min	Typ	Max	Unit
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
	For –CS signal when used to wake up from SLEEP mode			0.55	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V		–40	–60	µA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SLEEP TIMER					
Timeout Period[3]		0.5		128	Sec
FLASH MEMORY					
Endurance[4]		20,000			Cycles
Data Retention[5]	T_J = 55°C	20			Years
CONVERSION RATE					
Minimum Conversion Time			3.906		ms
Maximum Conversion Time			7.75		Sec
Maximum Throughput Rate			250		SPS
Minimum Throughput Rate			0.129		SPS
POWER SUPPLY					
Operating Voltage Range V_{CC}		4.75	5.0	5.25	V
Power Supply Current	Normal mode at 25°C		15	19	mA
	Fast mode at 25°C		41	48	mA
	Sleep mode at 25°C		500	750	µA

[1] Dynamic range is only limited by performance criteria; sensor structure is capable of measuring ±600°/sec with degraded performance.
[2] Dynamic range setting can be established by accessing the SENS/AVG register.
[3] Guaranteed by design.
[4] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at –40°C, +25°C, +85°C, and +125°C.
[5] Retention lifetime equivalent at junction temperature (T_J) 55°C as per JEDEC Standard 22 Method A117. Retention lifetime decreases with junction temperature.

TIMING SPECIFICATIONS

T_A = −40°C to +85°C, V_{CC} = 5.0 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Fast Mode[2]	0.01		2.5	MHz
	Normal Mode[2]	0.01		1.0	MHz
$t_{DATARATE}$	Chip Select Period, Fast Mode	40			µs
$t_{DATARATE}$	Chip Select Period, Normal Mode	100			µs
t_{CS}	Chip Select to Clock Edge	48.8			ns
t_{DAV}	Data Output Valid after SCLK Edge			100	ns
t_{DSU}	Data Input Setup Time Before SCLK Rising Edge	24.4			ns
t_{DHD}	Data Input Hold Time After SCLK Rising Edge	48.8			ns
t_{DF}	Data Output Fall Time		5	12.5	ns min
t_{DR}	Data Output Rise Time		5	12.5	ns min
t_{SFS}	$\overline{CS}$ High after SCLK Edge	5			ns typ

[1] Guaranteed by design, typical specifications are not tested or guaranteed.
[2] Based upon sample rate selection.

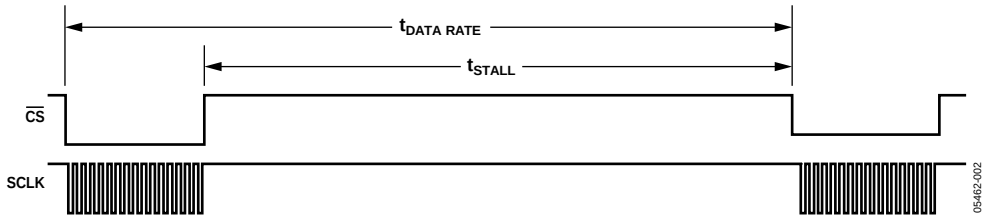

Figure 2. SPI Chip Select Timing

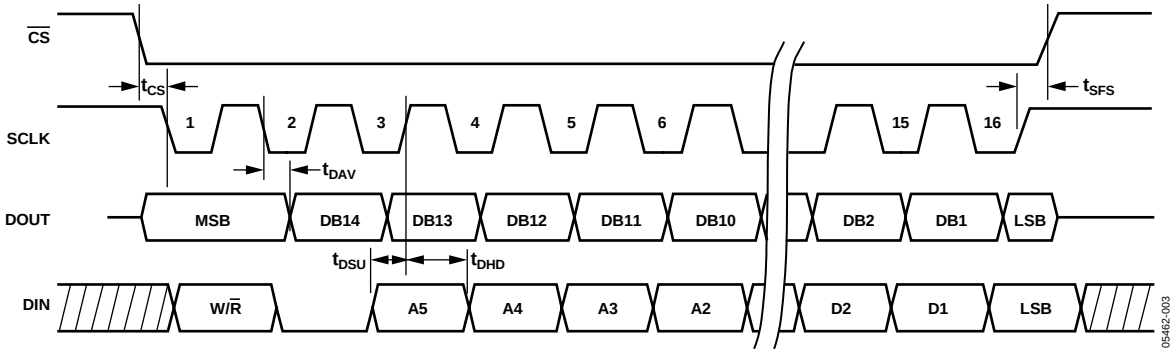

Figure 3. SPI Timing
(Utilizing SPI Settings Typically Identified as Phase = 1, Polarity = 1)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
V_{CC} to COM	−0.3 V to +6.0 V
Digital Input/Output Voltage to COM	−0.3 V to +5.5 V
Analog Inputs to COM	−0.3 V to 3.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

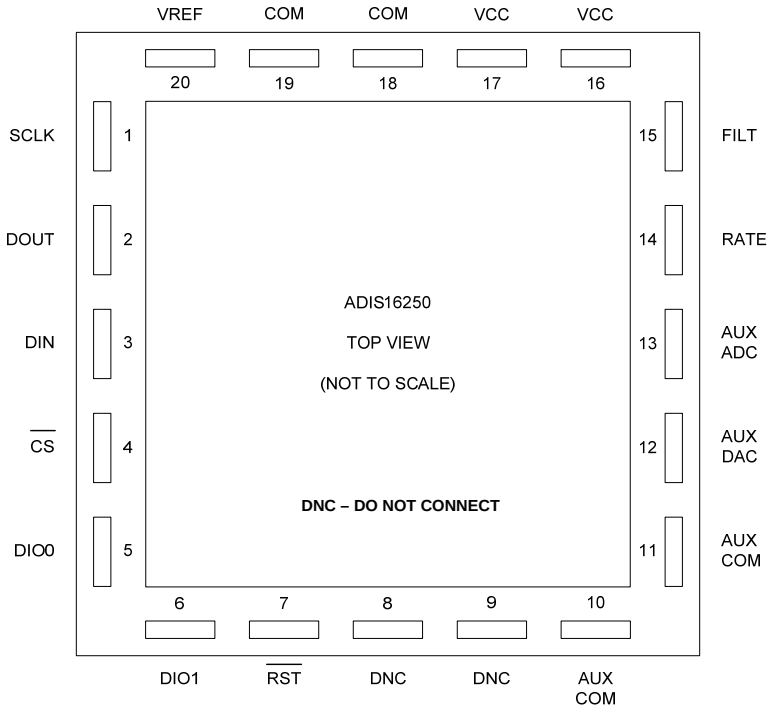

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SCLK	I	Serial Clock. SCLK provides the serial clock for accessing data from the part and writing serial data to the control registers.
2	DOUT	O	Data Out. The data on this pin represents data being read from the control registers and is clocked out on the falling edge of the SCLK.
3	DIN	I	Data In. Data written to the control registers is provided on this input and is clocked in on the rising edge of the SCLK.
4	$\overline{CS}$	I	Chip Select, Active Low. This input frames the serial data transfer.
5, 6	DIO0, DIO1	I/O	Multifunction Digital Input/Output pin.
7	$\overline{RST}$	I	Reset, Active Low. This resets the sensor signal conditioning circuit and initiates a start-up sequence.
8, 9	DNC	–	Do Not Connect.
10, 11	AUX COM	I	Auxiliary Grounds. Connect to GND for proper operation.
12	AUX DAC	O	Auxiliary DAC Analog Voltage Output.
13	AUX ADC	I	Auxiliary ADC Analog Input Voltage.
14	RATE	O	Analog Rate Signal Output.
15	FILT	I	Analog Amplifier Summing Junction.
16,17	V_{CC}	S	+5.0 V Power Supply.
18,19	COM	S	Common. Reference point for all circuitry in the ADIS16250.
20	VREF	O	Precision Reference Output.

[1] S = Supply; O = Output; I = Input.

THEORY OF OPERATION

OVERVIEW

The core angular rate sensor integrated inside the ADIS16250 is based on Analog Devices' iMEMS technology. This sensor operates on the principle of a resonator gyro. Two polysilicon sensing structures each contain a dither frame, which is electrostatically driven to resonance. This produces the necessary velocity element to produce a Coriolis force during angular rate. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers that are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output.

The base sensor's output is sampled using an ADC and then the digital data is fed into a proprietary digital calibration circuit. This circuit contains calibration coefficients from the factory calibration, along with user-defined calibrations that can be used to calibrate system-level errors.

The calibrated gyro data is made available through output data registers along with temperature, power supply, auxiliary ADC, and relative angle output calculations.

BASIC OPERATION

The ADIS16250 is a calibrated, digital angular rate sensor that also provides power supply measurements, temperature measurements, auxiliary ADC data, and integrated angular rate data. It also offers a number of useful programmable features that allow users to optimize its operation in their systems. The basic operation of the ADIS16250 is facilitated by reading and writing to a set of registers that have been dedicated to the required I/O functions. These registers are accessed by using the 4-wire, serial peripheral interface (SPI) port. Each one has its own unique address and bit assignments that have been optimized for each function. The output data registers are summarized in Table 6. The control registers are summarized in Table 9.

Using the ADIS16250 in the most basic, simple configuration requires only the power supply connections (+5 V/COM) and the SPI port's four wires. A common approach for accessing the ADIS16250 through the SPI port is with a digital processing solution, such as the Black*fin*® family of DSP/MCUs. For example, the BF533 has seven different SPI ports that can each be used to access multiple SPI-driven devices.

REGISTER DETAILS

The registers in the ADIS16250 are 16 bits in length. Each of them has been assigned an address for their upper byte and lower byte. Each control register's bit map uses the numerical assignments that are displayed in Table 5.

Table 5. Basic Register Bit Map

MSB							LSB
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0

The upper byte consists of Bit 8 to Bit 15, and the lower byte consists of Bit 0 to Bit 7. The following sections provide descriptions of each register including purpose, scaling information, bit maps, addresses, and default values.

Table 6. Data Output Register Information

Name	Function	Address	Resolution (Bits)	Data Format	Scale Factor (per LSB)
SUPPLY_OUT	Power Supply Data	0×03, 0×02	12	Binary	1.22 mV
GYRO_OUT	Gyroscope Data	0×05, 0×04	14	Twos Complement	0.07326°/sec[1]
AUX_ADC	Auxiliary Analog Input Data	0×0B, 0×0A	12	Binary	0.61 mV
TEMP_OUT	Sensor Temperature Data	0×0D, 0×0C	12	Binary	−0.47°C
ANGL_OUT	Angle Output	0×0F, 0×0E	14	Binary	0.03663°

[1] Assumes that the scaling is set to 320°/sec.

SPI Operation

The ADIS16250 SPI port provides full duplex data transfer, which maximizes the efficiency of each data transfer. By using a single SCLK edge to accomplish both data input reads (DIN) and data output transfers (DOUT), ADIS16250 data transfers require less of the serial buses' time. Each data transfer is 16 SCLK cycles in length. Read cycles require two data transfer cycles while write cycles only require one.

The 4-wire SPI port lines are assigned as follows: the chip select line (~CS), the data clock (SCLK), data input (DIN), and data output (DOUT).

Reading Registers

Reading the contents of any accessible register in the ADIS16250 requires two data transfer cycles: one for transferring the register's address and one for reading the two bytes from the register. Figure 5 displays the sequence of a read cycle on the ADIS16250 SPI port and Table 8 contains the bit definitions for DIN and DOUT. The DIN sequence starts with two zeros, followed by the registers address, A5 to A0. For example, the GYRO_OUT register address is 0x04, which results in an A5 to A0 bit sequence of 000100. The last 8 bits in the DIN sequence, B7 to B0, are ignored by the ADIS16250 during read cycles. During the next data transfer cycle, the 16-bit contents of the register are read out on the DOUT pin, starting with two status bits, new data (ND) and error/alarm (EA). Then, the data associated with the GYRO_OUT register are transferred out, starting with the MSB.

The ND bit provides the ability to check if a conversion cycle has been complete. If the ND bits condition is a Logic 1, the contents of the register have been written since the last read cycle. Otherwise, the contents of the register have previously been read. If the condition of the EA bit is a Logic 1, an error or alarm condition occurs, announcing the need to read the STATUS register.

The angular rate data and angle out data registers are 14 bits in length. The angular rate data is formatted as a two's complement number and the angle output is formatted as binary data. The rest of the data output registers are 12 bits in length, leaving D12 and D13 as "don't care" bits. The output format for each of these registers, along with their addresses, can be found in Table 6. Each output data register has two different addresses. The first address is for the upper byte, which contains the most significant bits (D8 to D13), ND, and EA data. The second address is for the lower byte, which contains the eight least significant bits (D0 to D7). Reading either of these addresses results in all 16 bits being clocked out on the DOUT line as defined in Figure 5 during the next SPI cycle.

Writing to Registers

Write cycles require one 16-SLCK data transfer cycle. Once the ~CS line is taken low, the information on DIN is clocked in using the next 16 SLCK cycles. The first bit in the DIN sequence is a 1, which identifies the write designation. The second bit is a 0, which is followed by 6 bits that identify the address of the register being written to. The last 8 bits contain the contents that are to be written to the register. Because all of the registers are 2 bytes in length, a complete register update takes two 16-SCLK cycles.

Table 7. Output Coding Example, GYRO_OUT[1, 2]

Rate of Rotation					
±320°/sec range	**±160°/sec range**	**±80°/sec range**	**Binary Output**	**HEX Output**	**Decimal**
+600°/sec	+300°/sec	+150°/sec	01 1111 1111 1111	0x1FFF	8191
+320°/sec	+160°/sec	+80°/sec	01 0001 0001 0001	0x1110	4368
+80°/sec	+40°/sec	+20°/sec	00 0100 0100 0100	0x0444	1092
+40°/sec	+20°/sec	+10°/sec	00 0010 0010 0010	0x0222	546
+0.07326°/sec	+0.03663°/sec	+0.018315°/sec	00 0000 0000 0001	0x0001	1
0°/sec	0°/sec	0°/sec	00 0000 0000 0000	0x0000	0
−0.07326°/sec	−0.03663°/sec	−0.018315°/sec	11 1111 1111 1111	0x3FFF	−1
−40°/sec	−20°/sec	−10°/sec	11 1101 1101 1110	0x3DDE	−546
−80°/sec	−40°/sec	−20°/sec	11 1011 1011 1100	0x3BBC	−1092
−320°/sec	−160°/sec	−80°/sec	10 1110 1111 0000	0x2EF0	−4368
+600°/sec	−300°/sec	−150°/sec	10 0000 0000 0000	0x2000	−8192

[1] Two MSBs have been masked off and are not considered in the coding.
[2] Nominal sensitivity and zero offset null performance are assumed.

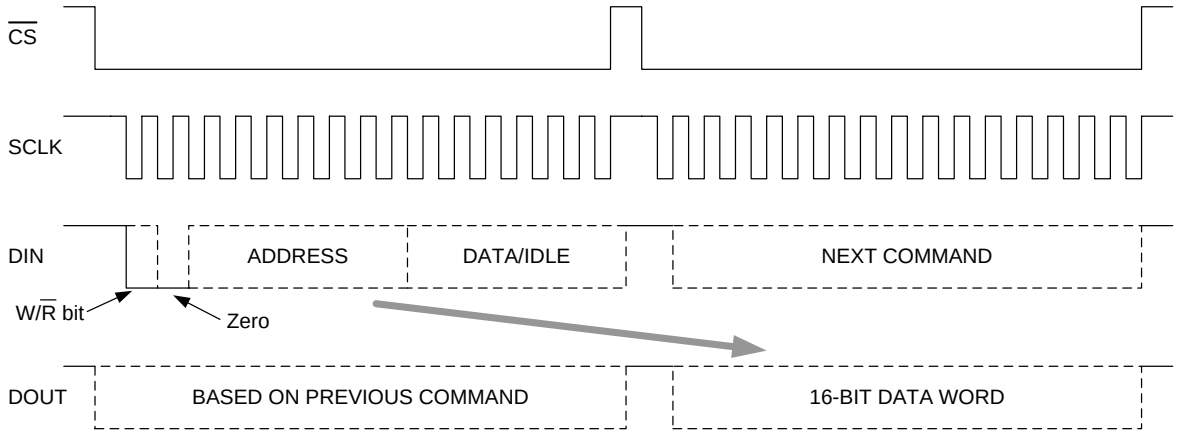

Figure 5. Register Read/Write Command Sequence

Table 8. Register Read/Write Command Bit Map

DIN	W/R	0	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
DOUT	**ND**	**EA**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	Upper Byte								Lower Byte							

CALIBRATION

The ADIS16250 angular rate output is calibrated at the factory, providing a high degree of accuracy and simpler system implementation. In addition, for system or field updates, the device has two control registers associated with calibrating the angular rate output data (see the Calibration Register Definitions section). Each of these registers has read/write capability and is 16 bits (2 bytes) in length. The calibration factors are 12 bits in length. The GYRO_OFF register uses the twos complement format allowing for both positive and negative offsets. The GYRO_SCALE register uses a straight binary format.

The data within these two calibration registers is utilized in offsetting and scaling of the output data registers according to the following relationship:

$$Output = A \times (x + C)$$

where:
x represents the raw data prior to calibration.
C is the offset.
A is the scalar.
Output represents the output data register where the resultant data is stored.

Simple access to these registers enables field calibration to correct for in-system error sources. In particular, the GYRO_OFF register allows the user to reset to 0°/sec reference point for the device. The GYRO_SCALE register allows for adjusting the sensitivity of the sensor measurements.

A global command is implemented within the ADIS16250 to simplify the loading of the GYRO_OFF register. Once the device is no longer rotating, establishing a zero-reference rotation, a null command can be sent to the ADIS16250 via the command control register, which zeros the GYRO_OUT and ANGL_OUT registers. Consequently, on the next reading of the five output data registers, the angular rate output should be set to zero. (neglecting noise and repeatability limitations).

It is suggested that when the null command is implemented, the AVG_CNT control register be adjusted to optimize the filtering and reduce the effects of noise in determining the values to be loaded into the offset control registers. Optionally, the user can manually load each of the two calibration registers via the SPI in order to calibrate the end system. This is applicable when the user plans to adjust the scale factor, thus requiring an external stimulus to excite the ADIS16250.

RANGE SELECTION

The AD16250 offers three different measurement ranges: ±320°/sec, ±160°/sec, and ±80°/sec. The maximum sample rate for each of these settings is 256, 64, and 16 samples per second respectively.

RELATIVE ANGLE ESTIMATE

The ANGL_OUT register offers the integration of the GYRO_OUT data. This number is reset when the NULL command is used, after a RESET command is used, and during power-up. This function can be used to estimate change in angle over a period. Users are cautioned to fully understand their stability requirements and the time period over which they can use this estimate relative angle position.

CONTROL REGISTER OPERATION

OVERVIEW

The Theory of Operation section describes the most basic operation of the ADIS16250. For added system flexibility and programmability, the following sections describe additional controls for the ADIS16250 sensor, as provided by the use of 21 digital control registers accessible via the SPI interface. A high level listing of these registers is given within Table 9. This table also refers to the appropriate tables regarding each register's definition. The following sections expand upon the functionality of each of these control registers, providing for the full clarification of each of the control registers behavior. Available control modes for the device include selectable sample rates for reading the five output vectors, selectable data averaging at the output registers, alarm settings, control of the on-board 12-bit auxiliary DAC, handling of the two general purpose I/O lines, facilitating of the sleep mode, enabling the self-test mode, and other miscellaneous control functions.

The conversion process is repeated continually, providing for the continuous update of the five output registers. New data ready bit (ND) flag bits common to all five output registers allow the completion of the conversion process to be tracked via the SPI. As an alternative, the digital I/O lines can be configured through software control to create a data ready hardware function that can signal the completion of the conversion process.

Two independent alarms provide the ability to monitor any one of the five output registers. They can be configured to report an alarm condition on either fixed thresholds or rates of change. The alarm conditions are monitored through the SPI. In addition, the user can configure the digital I/O lines through software control to create an alarm function that allows for monitoring of the alarm conditions through hardware.

The five output signals noted above are calibrated independently at the factory, delivering a high degree of accuracy. In addition, the user has access to independent offset and scale factors for the gyroscope output vector. This allows independent scaling and level adjustment control of gyroscope register prior to the value being read via the SPI. In turn, field level calibrations can be implemented within the sensor itself using these offset and scale variables. System level commands provided within the sensor include automatic zeroing of the gyroscope output and the angle output using a single null command via the SPI. In addition, the original factory calibration settings can be recovered at any point using a simple factory reset command.

ACCESS

The control registers within the ADIS16250 are based upon a 16-bit/2-byte format, and are accessed via the SPI. The SPI operates in full duplex mode with the data clocked out of the DOUT pin at the same time data is clocked in through the DIN pin. All commands written to the ASIS16250 are categorized as write commands or read commands. All write commands are self-contained and take place within a single cycle. Each read command requires two cycles to complete; the first cycle is for transmitting the register address and the second cycle is for reading the data. During the second cycle, when the data out line is active, the data in line is used to receive the next sequential command; this allows for overlapping the commands. For more information on basic SPI port operation, see the SPI Operation section.

The read and write commands are identified through the most significant bit (MSB), B15, of the received data. Write a 1 to B15 to indicate a write command. Write a 0 to B15 to indicate a read command. Bit B13 through Bit B8 contain the address of the control register that is being accessed. The remaining 8 bits of the write command contain the data that is being written into the part, whereas the remaining 8 bits of the read command contain "don't care" levels. Given that the data within the write command is 8 bits in length, the 8-bit data format is the default byte size. A write command operates on a single chip select cycle as shown in Figure 5. The read command operates on a 2-chip select cycle basis as seen in Figure 5. All 64 bytes of register space is accessed using the 6-bit address. Data written into the device is performed on a byte-wise basis with the address of each byte being explicitly called out in the write command. Conversely, data being read from the device consists of two, back-to-back, 8-bit variables being sent out with the first byte out corresponding to the upper address (odd number address) and the second byte relating to the next lower address space (even number address). For example, a data read of address 0x03 results in the data from address 0x03 being fed out followed by data from address 0x02. Likewise, a data read of address 0x02 results in the same data stream being output from the device

The ADIS16250 is a flash-based device with nonvolatile functional registers implemented as flash registers. Take into account the endurance limitation of 20,000 writes when considering the system-level integration of these devices. The nonvolatile column in Table 9 indicates which registers are recovered upon power-up. The user must instigate a manual flash update command via the command register to store the nonvolatile data registers once they are configured properly. When performing a manual flash update command, the user needs to assure that the power supply remains within limits for a minimum of 50 μs after the write is initiated. This assures a successful write of the nonvolatile data.

Table 9. Control Register Mapping

Register Name	Type	Address	Bytes	Function	Reference Table
SUPPLY_OUT	R	0x02	2	Power Supply Output Data.	Table 10, Table 11
GYRO_OUT	R	0x04	2	X-Axis Gyroscope Output Data.	Table 12, Table 13
		0x06 to 0x09	4	Reserved.	
AUX_ADC	R	0x0A	2	Auxiliary ADC Data.	Table 14,Table 15
TEMP_OUT	R	0x0C	2	Temperature Output Data.	Table 16, Table 17
ANGL_OUT	R/W	0x0E	2	X-Axis Angular Output Data.	Table 18, Table 19
		0x10	4	Reserved.	
GYRO_OFF	R/W	0x14	2	Gyroscope Offset Factor.	Table 20, Table 21
GYRO_SCALE	R/W	0x16	2	Gyroscope Scale Factor	Table 22, Table 23
		0x18 to to 0x1F	8	Reserved.	
ALM_MAG1	R/W	0x20	2	Alarm 1 Amplitude Threshold.	Table 24, Table 25
ALM_MAG2	R/W	0x22	2	Alarm 2 Amplitude Threshold.	Table 28, Table 29
ALM_SMPL1	R/W	0x24	2	Alarm 1 Sample Period.	Table 26, Table 27
ALM_SMPL2	R/W	0x26	2	Alarm 2 Sample Period.	Table 30, Table 31
ALM_CTRL	R/W	0x28	2	Alarm Source Control Register.	Table 32, Table 33
		0x2A to 0x2F	6	Reserved.	
AUX_DAC	R/W	0x30	2	Auxiliary DAC Data.	Table 48, Table 49
GPIO_CTRL	R/W	0x32	2	Auxiliary Digital I/O Control Register.	Table 46, Table 47
MSC_CTRL	R/W	0x34	2	Miscellaneous Control Register.	Table 44, Table 45
SMPL_PRD	R/W	0x36	2	ADC Sample Period Control.	Table 34, Table 35
SENS/AVG	R/W	0x38	2	Defines both sensitivity setting and the number of taps selected for the digital filter.	Table 36, Table 37
PWR_MDE	R/W	0x3A	2	Counter used to determine length of power-down mode.	
STATUS	R	0x3C	2	System Status Register.	Table 40, Table 41
COMMAND	W	0x3E	2	System Command Register.	Table 42, Table 43

ALARMS

The ADIS16250 contains two independent alarm functions that are referred to as Alarm 1 and Alarm 2. The Alarm 1 function is managed by the ALM_MAG1 and ALM_SMPL1 control registers. The Alarm 2 function is managed by the ALM_MAG2 and ALM_SMPL2 control registers. Both the Alarm 1 and Alarm 2 functions share the ALM_CTRL register. For simplicity, the following text references the Alarm 1 functionality only.

The 16-bit ALM_CTRL register serves three distinct roles in controlling the Alarm 1 function. First, it is used to enable the overall Alarm 1 function and select the output data variable that is to be monitored for the alarm condition. Second, it is used to select whether the Alarm 1 function is based upon a predefined threshold (THR) level or a predefined rate-of-change (ROC) slope. Third, the ALM_CTRL register can be used in setting up one of the two general-purpose input/output lines (GPIOs) to serve as a hardware output that indicates when an alarm condition has occurred. Enabling the I/O alarm function, setting its polarity, and controlling its operation are accomplished using this register.

Note that when enabled, the hardware output indicator serves both the Alarm 1 and Alarm 2 functions and cannot be used to differentiate between one alarm condition and the other. It is simply used to indicate that an alarm is active and that the user should poll the device via the SPI to determine the source of the alarm condition (see Table 40).

Because the ALM_CTRL, MSC_CTRL, and GPIO_CTRL control registers can influence the same GPIO pins, a priority level has been established to avoid conflicting assignments of the two GPIO pins. This priority level is defined as MSC_CTRL, which, in turn, has precedence over ALM_CTRL, which has precedence over GPIO_CTRL.

The ALM_MAG1 control register used in controlling the Alarm 1 function has two roles. The first role is to store the value with which the output data variable is compared to discern if an alarm condition exists or not. The second role is to identify whether the alarm should be active for excursions above or below the alarm limit. The comparison value contained within the ALM_MAG1 control register is located within the lower 14 bits.

The format utilized for this 14-bit value should match that of the output data register that is being monitored for the alarm condition. For instance, if the GYRO_OUT output data register is being monitored by Alarm 1, then the 14-bit value within the ALM_MAG1 control register takes on a twos complement format with each LSB equating to nominal 0.07326°/sec

(assumes unity scale and zero offset factors). The ALM_MAG value can be compared against the filtered or unfiltered data of the parameter being monitored.

Use caution when monitoring the temperature output register for the alarm conditions. Here, the negative temperature scale factor results in the greater than and less than selections requiring reverse logic.

When the THR function is enabled, the output data variable is compared against the ALM_MAG1 level. When the ROC function is enabled, the comparison of the output data variable is against the ALM_MAG1 level averaged over the number of samples, as identified in the ALM_SMPL1 control register. This acts to create a comparison of (Δ units/Δ time) or the derivative of the output data variable against a predefined slope.

The versatility built into the alarm function is intended to allow the user to adapt to a number of different applications. For example, in the case of monitoring a twos complement variable, Bit 15 within the ALM_MAG1 control register can allow for the detection of negative excursions below a fixed level. In addition, the Alarm 1 and Alarm 2 functions can be set to monitor the same variable that allows the user to discern if an output variable remains within a predefined window.

Other options include the rate-of-change function that can be used in monitoring angular acceleration levels that would warrant special attention. With the addition of the alarm hardware functionality, the ADIS16250 can be left to run independently of the main processor and interrupt the system only when an alarm condition occurs. Conversely, the alarm condition can be monitored through the routine polling of any one of the five data output registers.

The alarm hardware output indicator is not latched but tracks the actual alarm conditions in real time.

GENERAL PURPOSE I/O CONTROL

As previously noted, the ADIS16201 provides two general-purpose, bidirectional I/O pins (GPIOs) that are available to the user for control of auxiliary circuits within the target application. All I/O pins are 5 V tolerant, meaning that the GPIOs support an input voltage of 5 V. All GPIO pins have an internal pull-up resistor of approximately 100 kΩ, and their drive capability is 1.6 mA. The direction, as well as the logic level, can be controlled for these GPIO pins through the GPIO_CTRL control register, as defined in Table 47.

These same GPIO pins are also controllable through the ALM_CTRL and MSC_CTRL control registers. The priority for these three control registers in controlling the two GPIO pins is MSC_CTRL has precedence over ALM_CTRL, which, in turn, has precedence over GPIO_CTRL.

MISCELLANEOUS CONTROL REGISTER

The MSC_CTRL control register within the ADIS16250 provides control of two miscellaneous functions: the data-ready hardware I/O function and the self-test function. The bits to control these two functions are shown in Table 27.

The operation of the data-ready hardware I/O function is very similar to the alarm hardware I/O function (controlled through the ALM_CTRL control register). In this case, the MSC_CNTRL register can be used in setting up one of the two GPIO pins to serve as the hardware output pin that indicates when the sampling, conversion, and processing of the five data output variables has been completed. This register provides the ability to enable the data-ready hardware function and establish its polarity.

The data-ready hardware I/O pin is reset automatically to an inactive state part way through the next conversion cycle, resulting in a pulse train with a duty cycle varying from ~15% to 35%, depending upon the sample period setting. Upon completion of the next sample/conversion/processing cycle, the data ready hardware I/O line is reasserted.

The MSC_CTRL, ALM_CTRL, and GPIO_CTRL control registers can influence the same GPIO pins. A priority level has been established to avoid conflicting assignments of the two GPIO pins. This priority level is defined as MSC_CTRL and has precedence over ALM_CTRL, which has precedence over GPIO_CTRL.

SAMPLE PERIOD CONTROL

The five output data variables within the ADIS16250 are sampled and updated at a rate based upon the SMPL_PRD control register.

Note that the sample period given is defined as the cumulative time required to sample, process, and update all seven data output variables. The five data output variables are sampled as a group and in unison with one another. Whatever update rate is selected for one signal, all five output data variables are updated at the same rate whether they are monitored via the SPI or not.

For a sample period setting of less than 15.62 ms (SMPL_RATE ≤ 0x07), the overall power dissipation in the part rises by approximately 300%. The default setting for the SMPL_RATE register is 0x01 at initial power-up, thus allowing for the maximum SPI clock rate of 2.5 MHz.

SENSITIVITY/FILTERING CONTROL

The ADIS16250 offers three distinct sensitivity settings that result in the following measurement ranges: ±320°/sec, ±160°/sec, and ±80°/sec. It also has the ability to perform basic filtering on the five output data variables. Both of these functions are controlled and setup through the SENS/AVG control register. The filtering performed is that of a low-pass,

Bartlet-Window filter. The number of filter taps is determined through the SENS/AVG control register. The filtering applied through the SENS/AVG control register is applied to all five data output variables concurrently and, thus, one output variable cannot be filtered differently from another.

POWER-DOWN CONTROL

The ADIS16250 has the ability to power down for user-defined amounts of time, using the SLP_CNT control register.

STATUS FEEDBACK

The status control register within the ADIS16250 is utilized in determining the present state of the device. The ability to monitor the device becomes necessary when and if the ADIS16250 has registered an alarm or error condition as indicated by the "alarm enable" within the five output data registers. The 16-bit status register is broken into two bytes. The three lower bits of the lower data byte are used to indicate which error condition exists. The next two bits of the lower byte monitor the status of the maximum angular rate and the internal diagnostics. The two lower bits of the upper data byte are utilized in indicating which alarm condition exists.

COMMAND CONTROL

The COMMAND control register is utilized in sending global commands to the ADIS16250 device. There are five separate commands that act as global commands in the controlling of the ADIS16250 operation. Any one of the four commands can be implemented by writing 1 to its corresponding bit location. The command control register has write-only capability and is volatile. Table 43 describes each of these global commands.

PERIPHERALS

AUXILIARY ADC FUNCTION

The auxiliary ADC function integrates a standard 12-bit ADC into the ADIS16250 to digitize other system-level analog signals. The output of the ADC can be monitored through the AUX_ADC control register, as defined in Table 6. The ADC consists of a 12-bit successive approximation converter. The output data is presented in straight binary format with the full-scale range extending from 0 V to VREF. A high precision, low drift, factory calibrated 2.5 V reference is also provided.

Figure 6 shows the equivalent circuit of the analog input structure of the ADC. The input capacitor, C1, is typically 4 pF and can be attributed to parasitic package capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This would cause these diodes to become forward-biased and start conducting. They can handle 10 mA without causing irreversible damage to the part. The resistor is a lumped component that represents the on resistance of the switches. The value of this resistance is typically 100 Ω. Capacitor C2 represents the ADC sampling capacitor and is typically 16 pF.

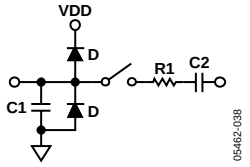

Figure 6. Equivalent Analog Input Circuit
Conversion Phase: Switch Open
Track Phase: Switch Closed

For AC applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins.

In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated.

AUXILIARY DAC FUNCTION

The auxiliary DAC function integrates a standard 12-bit DAC into the ADIS16201. The DAC output is buffered and fed off-chip to allow for the control of miscellaneous system-level functions. Data is downloaded through the writing of two adjacent data bytes, as defined in its register definition. To prevent the DAC from transitioning through inadvertent states during data downloads, a single command is used to simultaneously latch both data bytes into the DAC after they have been written into the AUX_DAC control register. This command is implemented by writing 1 to Bit 2 of the command control register, which, once received, results in the DAC output transitioning to the desired state.

The DAC output provides an output range of 0 V to 2.5 V. The DAC output buffer features a true rail-to-rail output stage. This means that, unloaded, the output is capable of reaching within 5 mV of ground. Moreover, the DAC's linearity performance (when driving a 5 kΩ resistive load to ground) is good through the full transfer function, except for Code 0 to Code 100. Linearity degradation near ground is caused by saturation of the output amplifier. As the output is forced to sink more current, the nonlinear region at the bottom of the transfer function becomes larger. Larger current demands can significantly limit output voltage swing.

REGISTER DETAILS

DATA OUTPUT REGISTER DEFINITIONS

Table 10. SUPPLY_OUT Register Definition

Address	Scale[1]	Default	Format	Access
0x03, 0x02	1.8315 mV	N/A	Binary	R

[1] Scale is the weight of each LSB.

The SUPPLY_OUT register contains the sampled power supply measurements. A measurement of 0 V is equal to 0 LSBs.

Table 11. SUPPLY_OUT Bit Designations

Bit	Description
15	New Data Flag. Set when register data is updated.
14	Error/Alarm. Set when error or alarm is activated.
13,12	Not Used.
11:0	Data Bits.

Table 12. GYRO_OUT Register Definition

Address	Scale[1]	Default	Format	Access
0x05, 0x04	0.07326°/sec	N/A	Twos complement	R

[1] Scale is the weight of each LSB. This scale assumed ±320°/sec sensitivity setting.

With the range set to 320°/sec, an angular rotation of ±320°/sec translates into ±8736 LSB. A 0°/sec rotational rate ideally translates to a value of 0x0000. Additional range settings of 160°/sec and 80°/sec are selectable with corresponding resolutions of 0.03663°/sec/LSB (27.3 LSB/°/sec) and 0.018315°/sec/LSB (54.6 LSB/°/sec) respectively. Theoretical full-scale range for the ±320°/sec, ±160°/sec, and ±80°/sec settings are ±600°/sec, ±300°/sec, and ±150°/sec respectively.

Table 13. GYRO_OUT Bit Designations

Bit	Description
15	New Data Flag. Set when register data is updated.
14	Error/Alarm. Set when error or alarm is activated.
13:0	Data Bits.

Table 14. AUX_ADC Register Definition

Address	Scale[1]	Default	Format	Access
0x0B, 0x0A	0.6105 mV	N/A	Binary	R

[1] Scale is the weight of each LSB.

The AUX_ADC register contains the digitized auxiliary ADC's output data. An input voltage of 0 V ideally translates into 0 LSBs.

Table 15. AUX_ADC Bit Designations

Bit	Description
15	New Data Flag. Set when register data is updated.
14	Error/Alarm. Set when error or alarm is activated.
13,12	Not Used.
11:0	Data Bits.

Table 16. TEMP_OUT Register Definition

Address	Scale[1]	Default	Format	Access
0x0D, 0x0C	0.1453°C	N/A	Twos complement	R

[1] Scale is the weight of each LSB.

The TEMP_OUT register contains the digitized temperature data. A temperature of 25°C ideally translates to 0x0000.

Table 17. TEMP_OUT Bit Designations

Bit	Description
15	New Data Flag. Set when register data is updated.
14	Error/Alarm. Set when error or alarm is activated.
13,12	Not Used.
11:0	Data Bits.

Table 18. ANGL_OUT Register Definition

Address	Scale[1]	Default	Format	Access
0x0F, 0x0E	0.03663°	0x0000	Binary	R

[1] Scale is the weight of each LSB.

The ANGL_OUT provides integrated angular rate data, which represents relative angle. An output of 0x0000 translates to an angle of 0°. Value can be reset to zero via the null command located within the COMMAND register. Register can also be overwritten with an arbitrary value between 0 and 359.963 with any subsequent integration of rotational data occurring relative to this value.

Table 19. ANGL_OUT Bit Designations

Bit	Description
15	New Data Flag. Set when register data is updated.
14	Error/Alarm. Set when error or alarm is activated.
13:0	Data Bits.

CALIBRATION REGISTER DEFINITIONS

Table 20. GYRO_OFF Register Definition

Address	Scale[1]	Default	Format	Access
0x11, 0x10	0.018315°/sec	0x0000	Twos complement	R/W

[1] Scale is the weight of each LSB.

The GYRO_OFF register is the user-controlled register for calibrating system-level angular rate offset errors. It represents the offset variable in the calibration equation (see the Calibration section). The maximum calibration range is ±37.5°/sec, or +2047/−2048 codes, assuming nominal sensor sensitivity. The contents of this register are nonvolatile and are set to zero upon initial power-up.

Table 21. GYRO_OFF Bit Designations

Bit	Description
15:12	Not Used.
11:0	Data Bits.

Table 22. GYRO_SCALE Register Definition

Address	Scale[1]	Default	Format	Access
0x13, 0x12	0.0488%	0x0800	Binary	R/W

[1] Scale is the weight of each LSB.

The GYRO_SCALE register is the user-controlled register for calibrating system-level acceleration sensitivity errors. It represents the A variable in the calibration equation. This register offers a sensitivity calibration range of 0 to 1.9995, with unity gain being equal to 2048 LSBs. The contents of this register are nonvolatile.

Table 23. GYRO_SCALE Bit Designations

Bit	Description
15:12	Not Used.
11:0	Data Bits.

ALARM REGISTER DEFINITIONS

Table 24. ALM_MAG1 Register Definition

Address	Default[1]	Format	Access
0x21, 0x20	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The ALM_MAG1 register contains the threshold level for Alarm 1. The contents of this register are nonvolatile.

Table 25. ALM_MAG1 Bit Designations

Bit	Description
15	Greater than active alarm bit. 1: Alarm is active for an output greater than Alarm Magnitude 1 Register setting. 0: Alarm is active for an output less than Alarm Magnitude 1 Register setting.
14	Not Used.
13:0	Data Bits. This number can be either twos complement or straight binary. The format is set by the value being monitored by this function.

Table 26. ALM_SMPL1 Register Definition

Address	Default[1]	Format	Access
0x25, 0x24	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The ALM_SMPL1 register contains the sample period information for Alarm 1, when it is set for rate-of-change alarm monitoring. The rate-of-change alarm function averages the change in the output variable over the specified number of samples and compares this change directly to the values specified in the ALM_MAG1 register. The contents of this register are nonvolatile.

Table 27. ALM_SMPL1 Bit Designations

Bit	Description
15:8	Not Used.
7:0	Data Bits.

Table 28. ALM_MAG2 Register Definition

Address	Default[1]	Format	Access
0x23, 0x22	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The ALM_MAG2 register contains the threshold level for Alarm 2. The contents of this register are nonvolatile.

Table 29. ALM_MAG2 Bit Designations

Bit	Description
15	Greater than active alarm bit. 1: Alarm is active for an output greater than Alarm Magnitude 2 Register setting. 0: Alarm is active for an output less than Alarm Magnitude 2 Register setting.
14	Not Used.
13:0	Data Bits. This number can be either twos complement or straight binary. The format is set by the value being monitored by this function.

Table 30. ALM_SMPL2 Register Definition

Address	Default[1]	Format	Access
0x27, 0x26	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The ALM_SMPL2 register contains the sample period information for Alarm 2, when it is set for rate-of-change alarm monitoring. The rate-of-change alarm function averages the change in the output variable over the specified number of samples and compares this change directly to the values specified in the ALM_MAG1 register. The contents of this register are nonvolatile.

Table 31. ALM_SMPL2 Bit Designations

Bit	Description
15:8	Not Used.
7:0	Data Bits.

Table 32. ALM_CTRL Register Definition

Address	Default[1]	Format	Access
0x29, 0x28	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The ALM_CTRL register contains the alarm control variables.

Table 33. ALM_CTRL Bit Designations

Bit	Value	Description
15		Rate of Change (ROC) Enable for Alarm 2.
		1: ROC is active.
		0: ROC is inactive.
14:12		Alarm 2 Source Selection.
	000	Alarm Disable.
	001	Alarm Source: Power Supply Output.
	010	Alarm 2 Source: Gyroscope Output.
	011	Alarm 2 Source: Inactive.
	100	Alarm 2 Source: Inactive.
	101	Alarm 2 Source: Auxiliary ADC Output.
	110	Alarm 2 Source: Temperature Sensor Output.
	111	Alarm 2 Source: Inactive.
11		Rate of Change (ROC) Enable for Alarm 1.
		1: ROC is active.
		0: ROC is inactive.
10:8		Alarm 1 Source Selection.
	000	Alarm Disable.
	001	Alarm Source: Power Supply Output.
	010	Alarm 1 Source: Gyroscope Output.
	011	Alarm 1 Source: Inactive.
	100	Alarm 1 Source: Inactive.
	101	Alarm 1 Source: Auxiliary ADC Output.
	110	Alarm 1 Source: Temperature Sensor Output.
	111	Alarm 1 Source: Inactive.
7:5		Not Used.
4		Data Source Select. This bit determines whether the Alarm thresholds are compared with pre-filtered data or post-filtered data.
		1: Filtered data is used for alarm comparisons.
		0: Pre-filtered data is used for the alarm comparisons
3		Not Used.
2		Alarm Output Enable.
		1: Alarm output enabled.
		0: Alarm output disabled.
1		Alarm Output Polarity.
		1: Active high.
		0: Active low.
0		Alarm Output Line Select.
		1: DIO1.
		0: DIO0.

PROGRAMABLE FEATURE REGISTER DEFINITIONS

Table 34. SMPL_PRD Register Definition

Address	Default[1]	Format	Access
0x37, 0x36	0x0001	N/A	R/W

[1] Default is valid only until the first register write cycle.

The data within this register is nonvolatile, allowing for data recovery upon reset. The initial value is set to 0x01 upon initial power-up, allowing for a sample rate of 256 samples per second.

Table 35. SMPL_PRD Bit Descriptions

Bit	Description
15:8	Not Used.
7:0	ADC Sample Period Count, ADC Sample Time Control Register. The 16 bit register is set to 0x01 upon initial power-up allowing for a combined sample rate of 256 samples per second (combined sample rate being the rate at which all four outputs are sampled and updated). The MSB, SR7, allows for selection of the combined base acquisition time of 1.953 ms with SR7 set to 0 ms or 60.54 ms when SR7 is set to 1. The lower seven bits, SR6 to SR0, represent a binary count, which when added to one and then multiplied by the combined base acquisition time, results in an overall acquisition time. Note that the minimal allowable setting for the bits SR6 to SR0 is 0x01. The overall acquisition time can be varied from 3.906 ms to 250 ms in 1.953 ms increments for SR7 = 0 and from 121 ms to 7.75 sec in 60.54 ms increments for SR7 = 1. This equates to the sample rate varying from 256 SPS to 4.0 SPS for SR7 = 0 and from 8.26 SPS to 0.129 SPS for SR1 = 1. Last written value is nonvolatile allowing for data recovery upon reset. Read/Write capability.

Table 36. SENS/AVG Register Definition

Address	Default[1]	Format	Access
0x39, 0x38	0x0402	Binary	R/W

[1] Default is valid only until the first register write cycle.

The SENS/AVG controls two different features: sensitivity and averaging. The sensitivity directly impacts the measurement range of the sensor and the averaging setting establishes the number of taps in the filtering network.

Table 37. SENS/AVG Bit Description

Bit	Value	Description
15:11		Not used
10:8		Sensitivity Selection Bits. Default setting: 320°/sec. Suggest writing these three bits in a separate write command, before setting the average count using bits 3:0.
	100	320°/sec
	010	160°/sec; automatically limits AC2 to AC0 to 0x02 minimum.
	001	80°/sec; automatically limits AC2 to AC0 to 0x04 minimum.
7:4		Not Used.
3:0		The average count register represents the number of taps utilized within the digital filter. The 3-bit binary value identifies the number of taps as defined by 2N where N is represented by the binary data AC2 to AC0 and is limited to a value ranging from 0 to 7. The number of taps can thus be varied from 1 to 128 by powers of two. The register is set to 2 upon initial power-up resulting in an effective filter with a −3dB point of approximately 40 Hz (SMPL_PRD set to 256 SPS). The value within the average count register is applied concurrently to the primary output registers: gyroscope, power supply, sensor temperature, auxiliary ADC, and angle output. Minimum value written to these bits is superseded by the S2 to S0 bit setting. Last written value is nonvolatile allowing for data recovery upon reset. Read/Write capability.

Table 38. SLP_CNT Register Definition

Address	Default[1]	Format	Access
0x3B, 0x3A	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The sleep count register is used in determining the duration of the sleep time within the sleep mode. The 8-bit register defines the sleep period by multiplying the binary value represented by SC7 to SC0 by the constant 0.5 sec. This results in a power-down period varying from 0.5 sec to 127.5 sec in 0.5 sec increments. If the register reads 0, the sleep mode is disabled. The sleep count register is volatile and is set to all 0's upon initial power-up. At anytime during a SLEEP interval, the value 0x00 may be written to the SLP_CNT register in order to wake up the part. In addition, resetting the part prematurely wakes up the part from its sleep times.

Table 39. SLP_CNT Bit Designations

Bit	Description
15:8	Not Used.
7:0	Data Bits.

Table 40. STATUS Register Definition

Address	Default[1]	Format	Access
0x3D, 0x3C	0x0000	N/A	Read only

[1] Default is valid only until the first register write cycle.

The STATUS control register contains the alarm/error flags that indicate abnormal operating conditions. See Table 41 for each status bit definition. Error flags are set as various error or alarm conditions occur, with the setting of multiple flags simultaneously being a possibility. Bits ST0, ST1, and ST4 are automatically cleared upon removal of the error condition thus making them "non-sticky." All flags are cleared upon the reading of the STATUS register. Potential exists for the flags to be set repeatedly if error conditions persist. All 0's upon reset. Read mode only.

Table 41. STATUS Bit Descriptions

Bit	Description
15:10	Not Used.
9	Alarm 2 Status. 1: Active. 0: Normal mode.
8	Alarm 1 Status. 1: Active. 0: Normal Mode.
7:6	Not Used.
5	Self-Test Diagnostic Error Flag. 1: Error Condition. 0: Normal Mode.
4	Angular Rate Overrange. 1: Error Condition. 0: Normal Mode.
3	SPI Communications Failure. 1: Error Condition. 0: Normal Mode.
2	Control Register Update Failed. 1: Error Condition. 0: Normal Mode.
1	Power Supply above 5.25 V. 1: Error Condition. 0: Normal Mode.
0	Power Supply below 4.75 V. 1: Error Condition. 0: Normal Mode.

Table 42. COMMAND Register Definition

Address	Default[1]	Format	Access
0x3F, 0x3E	0x0000	N/A	Write only

[1] Default is valid only until the first register write cycle.

The COMMAND control register is utilized in sending global commands to the ADIS16250 device.

Table 43. COMMAND Bit Descriptions

Bit	Description
15:8	Not used.
7	Software Reset Command. Allows for resetting of the device via the SPI.
6:4	Not used.
3	Manual FLASH Update Command. Setting this bit high results in the nonvolatile registers being written to FLASH memory. The update process takes approximately 50 ms with the user being asked to refrain from using the SPI for 50 ms once the bit is set. Power should remain valid during this time. Also note that the NULL and FACTORY reset command bits also initiate the FLASH update process and require the same stipulations as does the manual FLASH update command bit.
2	Auxiliary DAC Data Latch. This command latches any previous data sent to the auxiliary DAC registers into the DAC latches upon receipt of the command. This allows for sequential loading of the upper and lower DAC data bytes into the device via the serial interface without having the DAC go into unwanted states based upon the individual DAC bytes. Once the two bytes have been loaded, the DAC DATA latch command can be initiated to update the DAC.
1	Factory Reset Command. Allows user to reset the system level GYRO_OFF and GYRO_SCL registers to the initial factory settings upon receipt of command. Data within the digital filters are reset as well. Also see CMD3 command.
0	CMD0: Null Command. Sets the GYRO_OFF register upon receipt of command in order to zero out the Gyroscopic output. Also see CMD3 command.

Table 44. MSC_CTRL Register Definition

Address	Default[1]	Format	Access
0x35, 0x34	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The 16 bit miscellaneous control register is used in the controlling of the self-test and data-ready hardware functions. This includes turning on and off the diagnostics feature and self-test functions, as well as enabling and configuring the data-ready function. For the data-ready function, the written values are nonvolatile allowing for data recovery upon reset. The self-test data is volatile and is set to 0's upon reset.

Table 45. MSC_CTRL Bit Descriptions

Bit	Description
15:11	Not Used.
10	Internal Self-Test Enable. 1: Internal Self-Test Initiated. 0: Internal Self-Test Disabled. This bit initiates an internal diagnostics check of the sensor using simulated ± rotation rates relative to any steady state rotation. Once completed, the IST bit is cleared. Any errors are recorded in the STATUS register if detected.
9	External Negative Self-Test Enable. 1: ENST Enabled. 0: ENST Disabled. Simulates negative angular rotation of ~ −50°/sec relative to any steady state rotation.
8	External Positive Self-Test Enable. 1: EPST Enabled. 0: EPST Disabled. Simulates positive angular rotation of ~50°/sec relative to any steady state rotation.
7:3	Not Used.
2	Data-Ready Enable. 1: DR Enabled. 0: DR Disabled.
1	Data-Ready Polarity. 1: Active High. 0: Active Low.
0	Data-Ready Line Select. 1: DIO1. 0: DIO0.

Table 46. GPIO_CTRL Register Definition

Address	Default[1]	Format	Access
0x33, 0x32	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The data within auxiliary digital I/O control register is volatile and is set to 0s upon reset.

Table 47. GPIO_CTRL Bit Descriptions

Bit	Description
15:10	Not Used.
9	General-Purpose I/O Line 0, Data Direction Control. 0: Input. 1: Output.
8	General-Purpose I/O Line 1, Data Direction Control. 0: Input. 1: Output.
7:2	Not used.
1	General-Purpose I/O Line 0 Polarity. 0: Low. 1: High.
0	General-Purpose I/O Line 1 Polarity. 0: Low. 1: High.

Table 48. AUX_DAC Register Definition

Address	Default[1]	Format	Access
0x31, 0x30	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The AUX_DAC register controls the ADIS16201 DAC function. The data bits provide a 12-bit binary format number with 0 representing 0 V and 0x0FFFh representing 2.5 V. The data within this register is volatile and is set to 0s upon reset. This register has read/write capability.

Table 49. AUX_DAC Bit Descriptions

Bit	Description
15:12	Not Used.
11:0	Data Bits.

APPLICATIONS

HARDWARE CONSIDERATIONS

The ADIS16250 can be operated from a single 5.0 V (4.75 V to 5.25 V) power supply. The ADIS16250 integrates two decoupling capacitors, 1 µF and 0.1 µF in value. For the local operation of the ADIS16250, no additional power supply decoupling capacitance is required.

However, if the system power supply presents a substantial amount of noise, additional filtering can be required. If additional capacitors are required, connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, it should be noted that all analog and digital grounds be referenced to the same system ground reference point.

GROUNDING AND BOARD LAYOUT RECOMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of ADIS16250 designs in order to achieve optimum performance from the ADC and DAC.

Understanding that the ADIS16250 typically connects to both analog and digital circuits, the user must tie the separate ground planes together very close to the ADIS16250. In systems where analog and digital ground planes are connected together somewhere else (at the system power supply for example), they cannot be tied together at the ADIS16250 since a ground loop would result. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board such that digital return currents do not flow near analog circuitry and vice versa. The ADIS16250 can then be placed between the digital and analog sections.

In all of these scenarios, and in more complicated real-life situations, keep in mind that the current flows from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations.

Whenever possible, avoid large discontinuities in the ground plane as they force return signals to travel a longer path. Make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect any high speed logic signals (rise/fall times <5 ns) to either of the ADIS16250 digital I/O pins, add a series resistor to each line to keep the rise and fall times longer than 5 ns at the ADIS16250 digital I/O pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling (via parasitic capacitive paths) into the ADIS16250 and affecting the accuracy of the ADC conversions.

BANDGAP REFERENCE

The ADIS16250 provides an on-chip band gap reference of 2.5 V, which is utilized by the on-board ADC and DAC. This internal reference also appears on the VREF pin. This reference can be connected to external circuits in the system. An external buffer would be required because of the low drive capability of the VREF output.

SECOND-LEVEL ASSEMBLY

The recommended pad geometries for the ADIS16250 are displayed in Figure 7. The ADIS16250 can be attached to printed circuit boards using SN63 (or equivalent) or lead-free solder. Figure 8 and Table 50 provide recommended solder reflow profiles for each solder type. Note: These profiles may not be the optimum profile for the user's application. In no case, should the temperature exceed 260°C. It is recommended that the user develop a reflow profile based upon the specific application. In general, keep in mind that the lowest peak temperature and shortest dwell time above the melt temperature of the solder results in less shock and stress to the product. In addition, evaluating the cooling rate and peak temperature can result in a more reliable assembly.

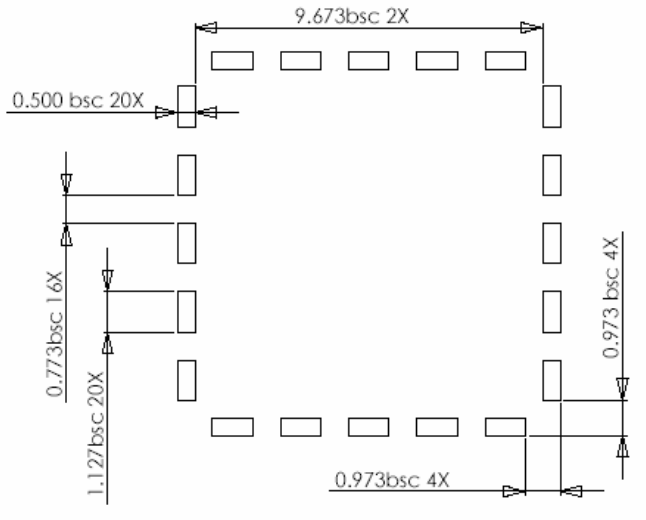

Figure 7. Recommended Pad Layout

Table 50.

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 120 sec	60 sec to 150 sec
T_{SMAX} to T_L		
Ramp-Up Rate	3°C/sec	3°C/sec
Time Maintained Above Liquidous (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240°C + 0°C/–5°C	260°C + 0°C/–5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max	8 min max

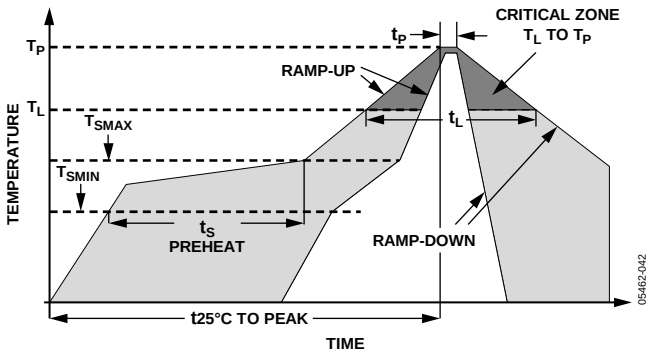

Figure 8. Acceptable Solder Reflow Profiles

OUTLINE DIMENSIONS

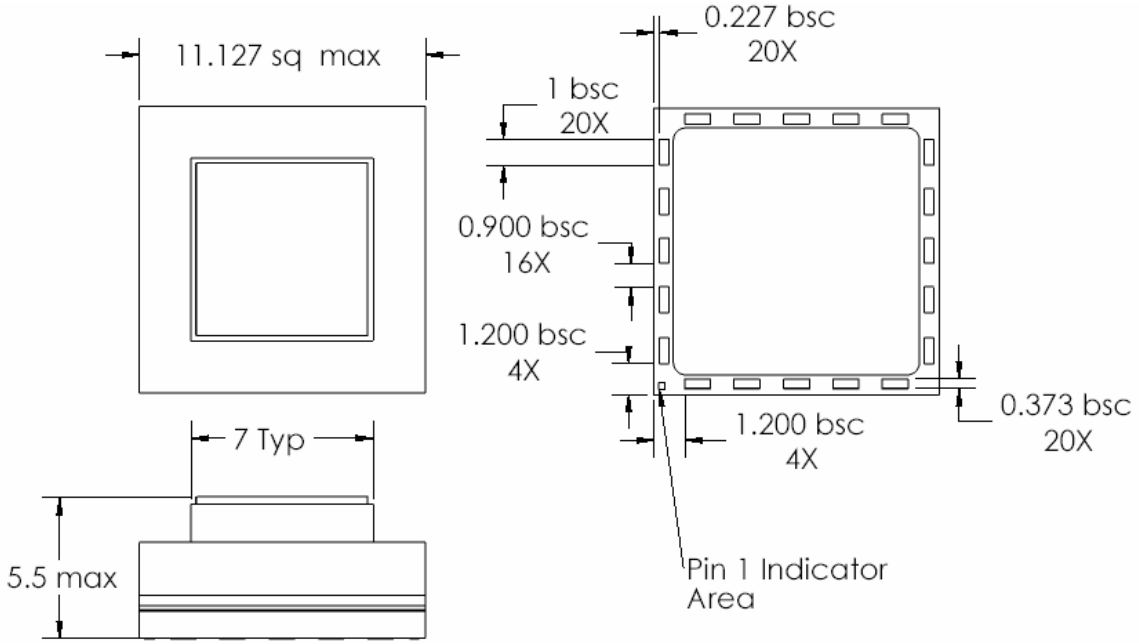

Figure 9. 20-Terminal Land Grid Array [LGA]
(CC-20-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16250ACCZ	−40°C to +85°C	20-Terminal Land Grid Array [LGA]	CC-20-5
ADIS16250/PCBZ		Evaluation Board	

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PR06070-0-6/06(PrB)