XRD4460/XRD44L60

CCD Image Digitizers with
CDS, PGA, and 10-bit A/D

FEATURES

- 10-Bit Resolution ADC
- 16MHz Sampling Rate
- Correlated Double Sampling (CDS)
- Programmable Gain from 6dB to 38dB (PGA)
- Digital Black Level Auto-Calibration
- CDS Clocks Can Sample Rising Edge or Falling Edge
- Single 5V or 3.0V Power Supply
- Low Power for Battery Applications:
  XRD4460: 250mW @ V_{DD} = 5.0V
  XRD44L60: 120mW @ V_{DD} = 3.0V
- 50μA - Typ Current in Stand By Mode
- 3–State Digital Outputs
- ESD Protection to Over 4000V

APPLICATIONS

- Digital Video Camcorders
- Digital Still Cameras
- PC Video Teleconferencing
- Digital Copiers
- Infrared Image Digitizers
- CCD/CIS Imager Interface

ALSO SEE

- XRD4461/XRD4462: Reduced Cost 32 Pin TQFP
- XRD4460EVAL: Evaluation System User Manual

GENERAL DESCRIPTION

The XRD4460/XRD44L60 are complete CCD Image Digitizers for digital cameras. The products include a high bandwidth differential Correlated Double Sampler (CDS), 8-bit digitally Programmable Gain Amplifier (PGA), 10-bit Analog-to-Digital Converter (ADC) and digital black level auto-calibration circuitry.

The Correlated Double Sampler (CDS) subtracts the CCD output signal black level from the video level. Common mode signal noise and power supply noise are rejected by the differential CDS input stage. CDS inputs are designed to be used either differential or single-ended.

The PGA is digitally controlled with 8-bit resolution on a linear dB scale, resulting in a gain range of 6dB to 38dB with 0.125dB per LSB of the gain code.

The PGA and black level auto-calibration are controlled through a simple 3-wire serial interface. The timing circuitry is designed to enable users to select a wide variety of available CCD image sensors for their applications.

The XRD4460/XRD44L60 has direct access to the PGA output and ADC input through the pin TESTVIN.

The XRD4460/XRD44L60 are packaged in 48-lead surface mount TQFP to reduce space and weight, and suitable for hand-held and portable applications.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range	Power Supply
XRD4460CIV	48 Lead TQFP (7 x 7 x 1.0 mm)	-40°C to 85°C	5.0V
XRD44L60CIV	48 Lead TQFP (7 x 7 x 1.0 mm)	-40°C to 85°C	3.0V

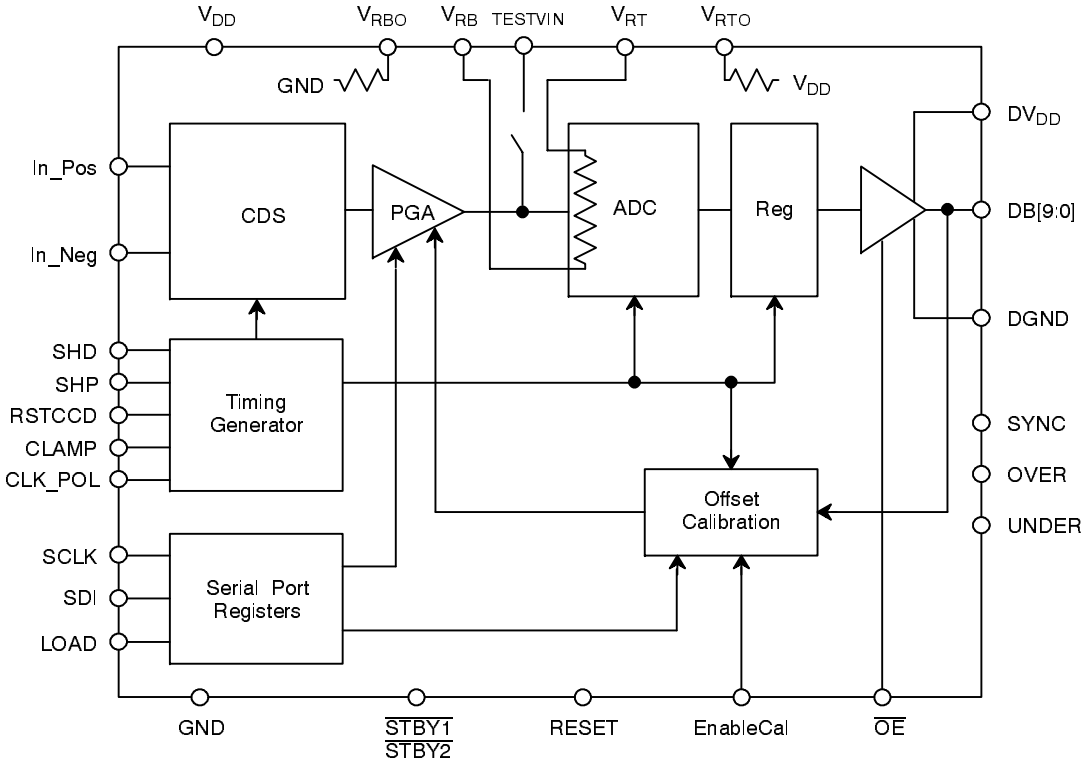
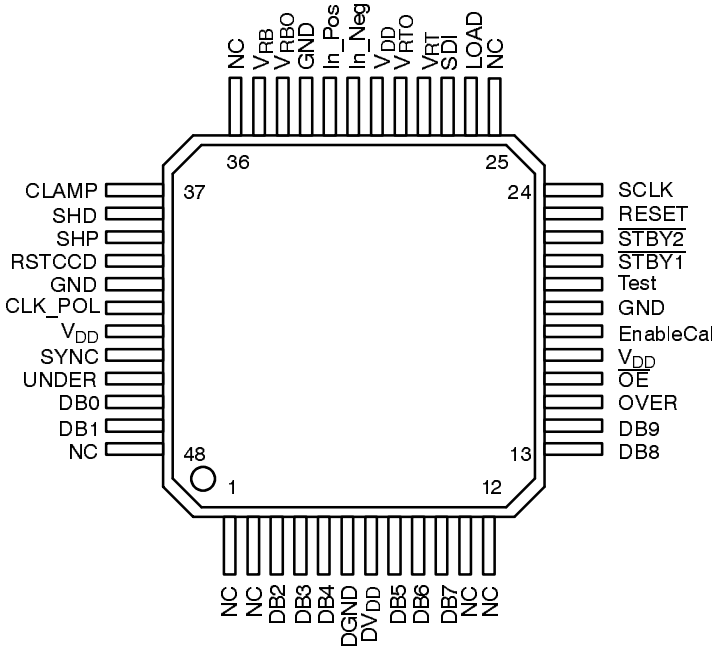


Figure 1. XRD4460/XRD44L60 Simplified Block Diagram

PIN CONFIGURATION



48 Lead TQFP (7 x 7 x 1.0 mm)

PIN DESCRIPTION - 48 pin TQFP

Pin #	Symbol	Description
1	NC	**No Connect.**
2	NC	**No Connect.**
3	DB2	**ADC Output.** DB0 is the LSB, DB9 is the MSB. The data changes on the rising edge of the RSTCCD clock. If $\overline{OE}$ is high or $\overline{STBY1}$ is low, the data bus goes into the high impedance state.
4	DB3	**ADC Output.**
5	DB4	**ADC Output.**
6	DGND	**Digital Output Ground.**
7	DV_{DD}	**Digital Output Power Supply.** Can be lower than V_{DD} supply voltage. Cannot be higher than V_{DD}.
8	DB5	**ADC Output.**
9	DB6	**ADC Output.**
10	DB7	**ADC Output.**
11	NC	**No Connect.**
12	NC	**No Connect.**
13	DB8	**ADC Output.**
14	DB9	**ADC Output.**
15	OVER	**Over Range Output Bit.** OVER goes high to indicate the ADC input voltage is greater than V_{RT}. When OVER goes high, DB[9:0] will output the full-scale code.
16	$\overline{OE}$	**Digital Output Enable (Three-State Control).** Controls the ADC output bus (DB[9:0], OVER and UNDER). Pull $\overline{OE}$ low to enable output drivers. Pull $\overline{OE}$ high to put output drivers in high impedance state.

PIN DESCRIPTION - 48 pin TQFP (CONT'D)

Pin #	Symbol	Description
17	V_{DD}	**Analog Power Supply.**
18	EnableCal	**Calibration Enable.** Pull high to enable the offset calibration circuit. Pull low to diable offset calibration.
19	GND	**Analog Ground.**
20	TESTVIN	**ADC Test Input & PGA Test Output.**
21	$\overline{STBY1}$	**Standby Control 1.** Pull low to put chip in power down mode.
22	$\overline{STYB2}$	**Standby Control 2.** Short to $\overline{STBY1}$ pin if not using TESTVIN pin.
23	RESET	**Chip Reset.** When reset goes high all internal control registers are set to power up default values. Gain register is set to code 00h (minimum gain). Offset code is set to 08h. Calibration circuit is cleared to uncalibrated state.
24	SCLK	**Shift Clock for Serial Register.** Serial register latches SDI data on the rising edges of SCLK. When LOAD is high SCLK is internally disabled.
25	NC	**No Connect.**
26	LOAD	**Data Load.** Rising edge loads data from serial input register to gain or offset register. Load must be low to enable shift register to read data from SDI.
27	SDI	**Data Input for Serial Register.**
28	V_{RT}	**Top ADC Reference.** Voltage at V_{RT} sets the full-scale of the ADC digitizing range.
29	V_{RTO}	**Internal Bias for V_{RT}.** Short V_{RT} to V_{RTO} to use internal reference voltage.
30	V_{DD}	**Analog Power Supply.**
31	In_Neg	**CDS Inverting Input.** Connect with DC blocking capacitor to CCD video output.
32	In_Pos	**CDS Non-inverting Input.** Connect with DC blocking capacitor to CCD ground or black reference.
33	GND	**Analog Ground.**
34	V_{RBO}	**Internal Bias for V_{RB}.** Short V_{RB} to V_{RB0} to use internal reference voltage.
35	V_{RB}	**Bottom ADC Reference.** The voltage at V_{RB} sets the zero scale of the ADC digitizing range.
36	NC	**No Connect.**
37	CLAMP	**CDS Clamp Control.** Clamps the CCD input pins (In_Pos & In_Neg) to internal black level bias, and enables the offset calibration.
38	SHD	**CDS Clock.** Controls sampling of the pixel video level.
39	SHP	**CDS Clock.** Controls sampling of the pixel black level.
40	RSTCCD	**CCD Reset Pulse Disconnect.** Used to decouple CDS during the reset pulse for noise reduction.
41	GND	**Analog Ground.**
42	CLK_POL	**Clock Polarity.** Controls the polarity of the CDS clock signals SHP, SHD & CLAMP.
43	V_{DD}	**Analog Power Supply.**
44	SYNC	**Digital output for Exar test purposes only.** No connect.
45	UNDER	**Under Range Output Bit.** UNDER goes high to indicate the ADC input voltage is less than V_{RB}. When UNDER goes high, DB[9:0] will output the zero-scale code.
46	DBO	**ADC Output.**
47	DB1	**ADC Output**.
48	NC	**No Connect.**

DC ELECTRICAL CHARACTERISTICS - XRD4460

Test Conditions: Unless otherwise specified: DV_{DD} = V_{DD} = 5.0V, Pixel Rate = 16MSPS, V_{RT} = 3.8V, V_{RB} = 0.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		200	800	mV_{PP}	Pixel (Black Level - Video Level)
BW	Small Signal Bandwidth (-3dB)		60		MHz	
SR	Slew Rate		40		V/µs	400mV Step Input.
FT	Feed-through (Hold Mode)		-60		dB	
PGA Parameters						
AV_{MIN}	Minimum Gain		6		dB	
AV_{MAX}	Maximum Gain		38		dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB).
GE	Gain Error		5		% FS	At maximum or minimum gain setting.
ADC Parameters (Measured Through TESTVIN)						
ADC n	Resolution	10			bits	
f_s	Max Sample Rate	18			MSPS	
DNL	Differential Non-Linearity	-1.0	±0.75	1.0	LSB	
EZS	Zero Scale Error	-5		5	mV	Measured relative to a zero input to the CDS. Zero scale code is set through the serial port.
EFS	Full Scale Error			4	% FS	
V_{IN}	DC Input Range	GND		V_{DD}	V	V_{IN} of the ADC can swing from GND to V_{DD}, actual digitized range is set by V_{RT} & V_{RB}. Input range is limited by the output swing of the PGA.
V_{RT}	Top Reference Voltage	1.5	3.8	V_{DD}	V	V_{RT}>V_{RB}
V_{RB}	Bottom Reference Voltage	GND	0.5	V_{DD}-1	V	V_{RT}>V_{RB}
ΔV_{REF}	Differential Reference Voltage	1.0	3.3	V_{DD}	V	
R_L	Ladder Resistance		500		Ω	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{V_{DD}}{10}\right)$		0.5		V	V_{RB} connected to V_{RBO}.
V_{RT}	Self Bias V_{RT} $\left(V_{RT} = \frac{V_{DD}}{1.30}\right)$		3.8		V	V_{RT} connected to V_{RTO}.
System Specifications						
DNL_{SMIN}	DNL @ Minimum Gain		0.75		LSB	
DNL_{SMAX}	DNL @ Maximum Gain		0.75		LSB	

DC ELECTRICAL CHARACTERISTICS - XRD4460 (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications (Cont'd)						
INL_{SMIN}	INL @ Minimum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
INL_{SMAX}	INL @ Maximum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
$V_{OS\ MINAV}$	Offset (Input Referred) @ Minimum Gain		5		mV	Offset is defined as the input pixel value-0.5 LSB required to cause the ADC output to switch from "Zero scale" to "Zero scale + 1LSB". Offset is measured after calibration.
$V_{OS\ MAXAV}$	Offset (Input Referred) @ Maximum Gain		1		mV	Zero scale is the code in the offset register. Offset depends on PGA gain code.
$en_{\ MAXAV}$	Input Referred Noise @ Maximum Gain		0.2		mV_{rms}	Noise depends upon gain setting of the PGA.
$en_{\ MINAV}$	Input Referred Noise @ Minimum Gain		3.5		mV_{rms}	Noise depends upon gain setting of the PGA.
Digital Inputs						
V_{IH}	Digital Input High Voltage	3.5			V	
V_{IL}	Digital Input Low Voltage			1.5	V	
I_L	DC Leakage Current		5		µA	Input Between GND and V_{DD}.
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	V_{DD}-0.5			V	While sourcing 2mA.
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA.
I_{OZ}	High-Z Leakage	-10		10	µA	$\overline{OE}$=1 or $\overline{STBY1}$= $\overline{STBY2}$ = 0. Output between GND & DV_{DD}.
Digital I/O Timing						
T_{DL}	Data Valid Delay		20	25	ns	
T_{PW1}	Pulse Width of SHD	15			ns	
T_{PW2}	Pulse Width of SHD	15			ns	
T_{PIX}	Pixel Period	62			ns	
T_{BK}	Sample Black Aperture Delay		4	6	ns	Over -40°C to 85°C range
T_{VD}	Sample Video Aperture Delay		3	5	ns	Over -40°C to 85°C range
T_{RST}	RSTCCD Switch Delay	0		4	ns	Over -40°C to 85°C range
T_{SC}	Shift Clock Period	40	70		ns	
T_{SET}	Shift Register Setup Time	10			ns	

DC ELECTRICAL CHARACTERISTICS - XRD4460 (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Power Supplies						
V_{DD}	Analog Supply Voltage	4.5	5.0	5.5	V	
DV_{DD}	Digital Output Supply Voltage	2.7	5.0	5.5	V	$DV_{DD} \leq V_{DD}$ Always
I_{DD}	Supply Current		50	70	mA	$DV_{DD} = V_{DD} = 5.0V$
I_{DDPD}	Power Down Supply Current		50	100	µA	$\overline{STBY1}$ = 0 and $\overline{STBY2}$ = 0

DC ELECTRICAL CHARACTERISTICS - XRD44L60

Test Conditions: Unless otherwise specified: $DV_{DD} = V_{DD} = 2.7V$, Pixel Rate = 16MSPS, $V_{RT} = 2.0V$, $V_{RB} = 0.3V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		200	800	mV_{PP}	Pixel (Black Level - Video Level)
BW	Small Signal Bandwidth (-3dB)		60		MHz	
SR	Slew Rate		40		V/µs	400mV Step Input.
FT	Feed-through (Hold Mode)		-60		dB	
PGA Parameters						
AV_{MIN}	Minimum Gain		6		dB	
AV_{MAX}	Maximum Gain		38		dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB).
GE	Gain Error		5		% FS	At maximum or minimum gain setting.
ADC Parameters (Measured Through TESTVIN)						
ADC n	Resolution	10			bits	
f_S	Max Sample Rate	18			MSPS	
DNL	Differential Non-Linearity	-1.0	±0.75	1.0	LSB	
EZS	Zero Scale Error	-5		5	mV	Measured relative to a zero input to the CDS. Zero scale code is set through the serial port.
EFS	Full Scale Error			4	% FS	
V_{IN}	DC Input Range	GND		V_{DD}	V	V_{IN} of the ADC can swing from GND to V_{DD}, actual digitized range is set by V_{RT} & V_{RB}. Input range is limited by the output swing of the PGA.
V_{RT}	Top Reference Voltage	1.5	2.07	V_{DD}	V	$V_{RT} > V_{RB}$

DC ELECTRICAL CHARACTERISTICS - XRD44L60 (CON'T)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
ADC Parameters (Con't)						
V_{RB}	Bottom Reference Voltage	GND	0.27	V_{DD}-1	V	$V_{RT} > V_{RB}$
ΔV_{REF}	Differential Reference Voltage	1.0	1.8	V_{DD}	V	
R_L	Ladder Resistance		500		Ω	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{V_{DD}}{10}\right)$		0.27		V	V_{RB} connected to V_{RBO}.
V_{RT}	Self Bias V_{RT} $\left(V_{RT} = \frac{V_{DD}}{1.30}\right)$		2.07		V	V_{RT} connected to V_{RTO}.
System Specifications						
DNL_{SMIN}	DNL @ Minimum Gain		0.75		LSB	
DNL_{SMAX}	DNL @ Maximum Gain		0.75		LSB	
INL_{SMIN}	INL @ Minimum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
INL_{SMAX}	INL @ Maximum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
$V_{OS\ MINAV}$	Offset (Input Referred) @ Minimum Gain		5		mV	Offset is defined as the input pixel value-0.5 LSB required to cause the ADC output to switch from "Zero scale" to "Zero scale + 1LSB". Offset is measured after calibration.
$V_{OS\ MAXAV}$	Offset (Input Referred) @ Maximum Gain		1		mV	Zero scale is the code in the offset register. Offset depends on PGA gain code.
$en_{\ MAXAV}$	Input Referred Noise @ Maximum Gain		0.2		mV_{rms}	Noise depends upon gain setting of the PGA.
$en_{\ MINAV}$	Input Referred Noise @ Minimum Gain		3.5		mV_{rms}	Noise depends upon gain setting of the PGA.
Digital Inputs						
V_{IH}	Digital Input High Voltage	2.0			V	
V_{IL}	Digital Input Low Voltage			0.8	V	
I_L	DC Leakage Current		5		µA	Input Between GND and V_{DD}.
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	V_{DD}-0.5			V	While sourcing 2mA.
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA.
I_{OZ}	High-Z Leakage	-10		10	µA	$\overline{OE}$=1 or $\overline{STBY1}$= $\overline{STBY2}$ = 0. Output between GND & DV_{DD}.

DC ELECTRICAL CHARACTERISTICS - XRD44L60 (CON'T)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital I/O Timing						
T_{DL}	Data Valid Delay		28	35	ns	
T_{PW1}	Pulse Width of SHD	15			ns	
T_{PW2}	Pulse Width of SHD	15			ns	
T_{PIX}	Pixel Period	62			ns	
T_{BK}	Sample Black Aperture Delay		5	7	ns	Over -40°C to 85°C range
T_{VD}	Sample Video Aperture Delay		4	6	ns	Over -40°C to 85°C range
T_{RST}	RSTCCD Switch Delay	0		5	ns	Over -40°C to 85°C range
T_{SC}	Shift Clock Period	40	70		ns	
T_{SET}	Shift Register Setup Time	10			ns	
Power Supplies						
V_{DD}	Analog Supply Voltage	2.7	3.0	3.6	V	
DV_{DD}	Digital Output Supply Voltage	2.7	3.0	3.6	V	$DV_{DD} \leq V_{DD}$ Always
I_{DD}	Supply Current		40	50	mA	$DV_{DD} = V_{DD} = 3.0$ V
I_{DDPD}	Power Down Supply Current		50	100	µA	$\overline{STBY1} = 0$ and $\overline{STBY2} = 0$

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7.0V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND -0.5V
V_{IN} ..... V_{DD} +0.5 to GND -0.5V
All Inputs ..... V_{DD} +0.5 to GND -0.5V
All Outputs ..... V_{DD} +0.5 to GND -0.5V
Storage Temperature ..... -65°C to 150°C
Lead Temperature (Soldering 10 seconds) ... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Ratings (T_A= +70°C)
TQFP ..... θ_{JA} = 54°C/W
ESD 4000V

Notes

1 Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

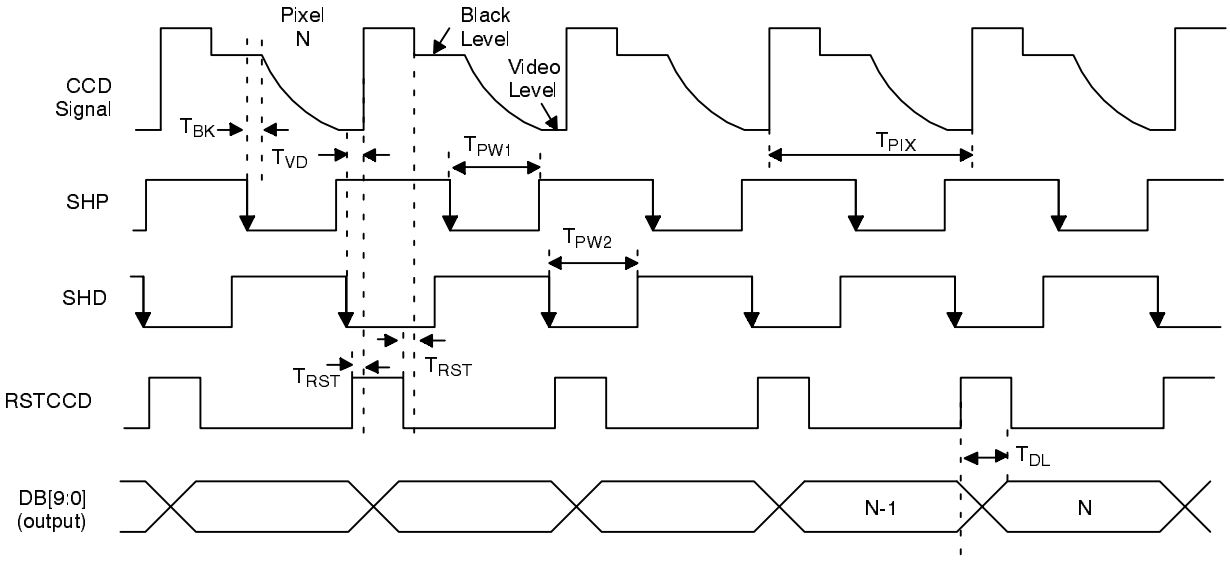


Figure 2. Conversion Timing Diagram (CLK_POL = High)

Event	Action
↑RSTCCD	Disconnect CDS Inputs from Reset Noise
↓RSTCCD	Connect CDS Inputs and Track Black Level
↓SHP	Hold Black Level and Track Video Level
↓SHD	Hold Video Level
↑SHP/SHD	No Action

Table 2. Timing Event Description
Table Valid for CLK_POL=High

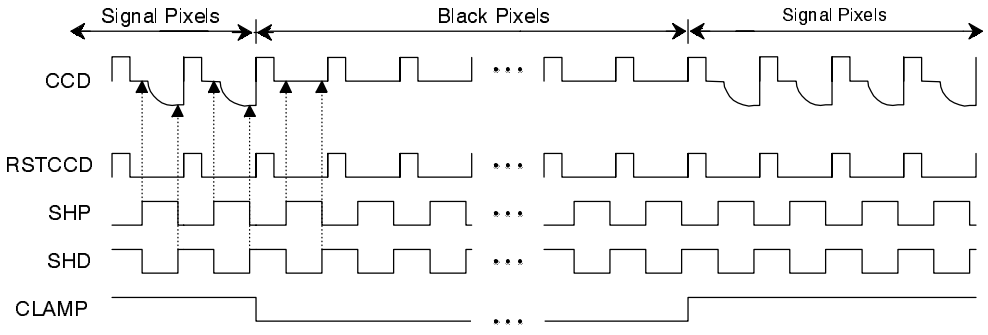


Figure 3. CDS Timing (with CLK_POL=Low)

Event	Action
↑RSTCCD	Disconnect CDS Inputs from Reset Noise
↓RSTCCD	Connect CDS Inputs and Track Black Level
↑SHP	Hold Black Level and Track Video Level
↑SHD	Hold Video Level
↓SHP/SHD	No Action
CLAMP Low	Force ADC Output Code to Equal Offset Code

Table 3. Timing Event Description for CLK_POL =0

SYSTEM DESCRIPTION

Correlated Double Sample/Hold (CDS) & Programmable Gain Amplifier (PGA)

The function of the CDS block, shown in *Figure 4*, is to sense the voltage difference between the black level and the video level of each pixel. CCD2 (IN_POS) would typically be considered the "common" voltage of the CCD which may be ground or the CCD black reference. CCD1 (IN_NEG) would be the actual CCD video output signal. The internal bias voltage, V_{BIAS}, sets the DC voltage of the input pins In_Pos & In_Neg. The DC voltage is updated every line using the CLAMP control input. The falling edges of SHP and SHD (with CLK_POL = High) are used to generate the internal signals SDRK and SPIX. SDRK samples the pixel black level by clamping the PGA inputs to V_{DD} when the CCD outputs the pixel black level. When SDRK goes low, the pixel value is transmitted through the internal capacitors and converted into a fully differential signal ***va*** by differential amplifier PGA1 which also provides programmable gains of 2.5, 1, and 0.4. The gain is controlled by the two most significant bits of the 8-bit gain control code. SPIX is used to sample/hold the pixel value ***va*** so that the required bandwidth of the following circuit is reduced. In each coarse gain segment set by PGA1, the second programmable amplifier PGA2 provides fine gain control (each LSB adds 0.125dB). The combined gain of the two PGA blocks is controlled by the digital code in the gain register. The gain register is programmed through the serial port.

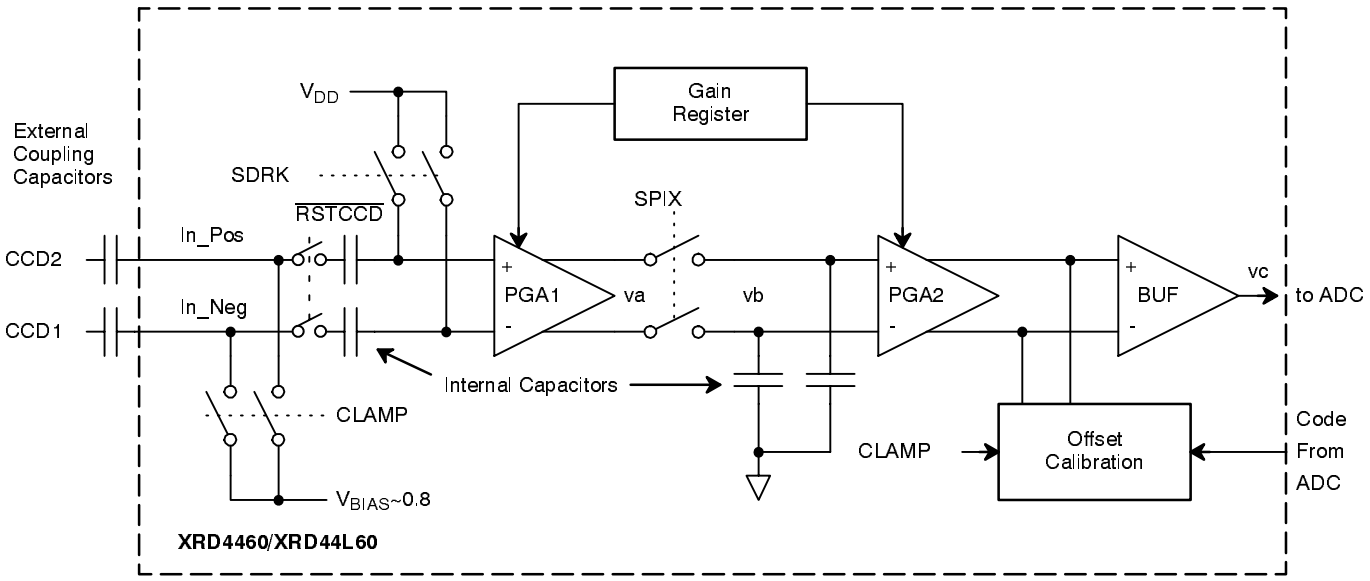


Figure 4. Block Diagram of the CDS

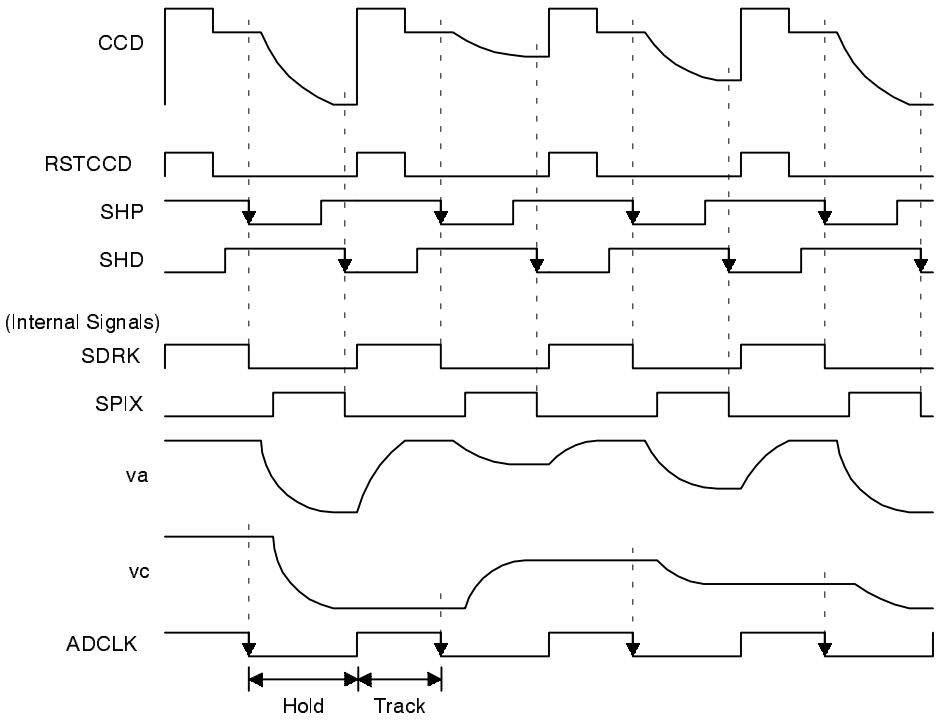


Figure 5. Timing Diagram of the CDS Clocks and Internal Signals (With CLK_POL = High)

Figure 5 shows the wave forms of the control clocks and the output voltages at various nodes in the block diagram. The falling edge of SHP samples the black level while the falling edge of SHD samples the pixel value. The ADC samples the output ***vc*** before the rising edge of SPIX. Note that ***vb*** and ***vc*** will have the same waveform shape, but ***vc*** will be delayed relative to ***vb***, and will have a different amplitude depending upon the gain setting.

Figure 6 shows PGA gain vs. gain register code. The PGA provides a programmable gain range of 32 dB. The minimum gain (code 00h) is 6dB ± 1dB. The maximum gain (code FFh) is 38dB ±1dB. Ideally, the gain can be expressed by the following equation.

$$\text{Gain[dB]} = 6 + \left(32 \cdot \frac{\text{code}}{256}\right)$$

where code is between 0 *and* 255.

The gain is realized by two stages. The gain transfer function is split into three main segments. The first stage, PGA1, is controlled by two MSBs of the 8-bit gain code and selects one of the three gain segments. The second stage, PGA2, provides fine gain adjustment within each gain segment. One LSB of the gain code represents a 0.125dB gain step. The gain control may not be monotonic between the codes 63-64, and 127-128 because of device mismatch; the maximum error is within 0.25dB.

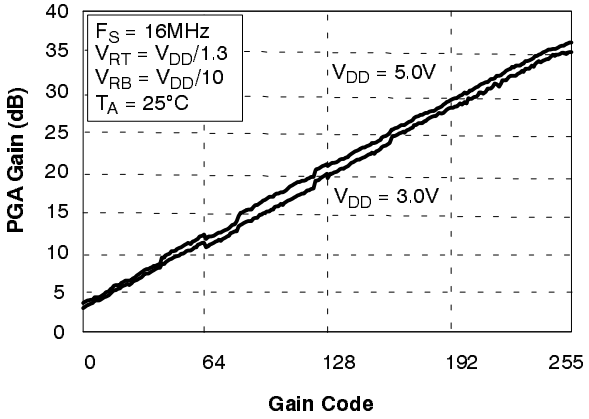


Figure 6. PGA Gain vs. Gain Code

Offset Calibration

To get maximum resolution in dark areas of an image the black level offset of the PGA must be equal to the bottom reference voltage of the ADC. When the EnableCal pin is high, the offset calibration logic operates during the interline black level clamping (CLAMP=active). The logic compares the ADC output code to the value stored in the offset register, and then increments or decrements the offset adjust DAC to make the ADC output equal to the code in the offset register. Each adjustment requires 6 cycles of the SHP/SHD clocks: 1 cycle for CDS, 3 cycles for A/D conversion, 1 cycle for logic, and 1 cycle for DAC update. Once the CLAMP signal is deactivated, the calibration process stops, and the black level calibration state is held. When the EnableCal pin is low, the offset calibration logic is disabled, and the current state of the offset DAC will be held constant. The offset register is 8 bits wide and is programmed through the serial port. The default value of this register at power up is 08h. Typical values for this register are between 02h and 20h. When the part is first powered up, the calibration may take several hundred clock cycles to converge to the proper offset. However, it requires only a few clock cycles subsequently to maintain the offset value (see *Figure 7*).

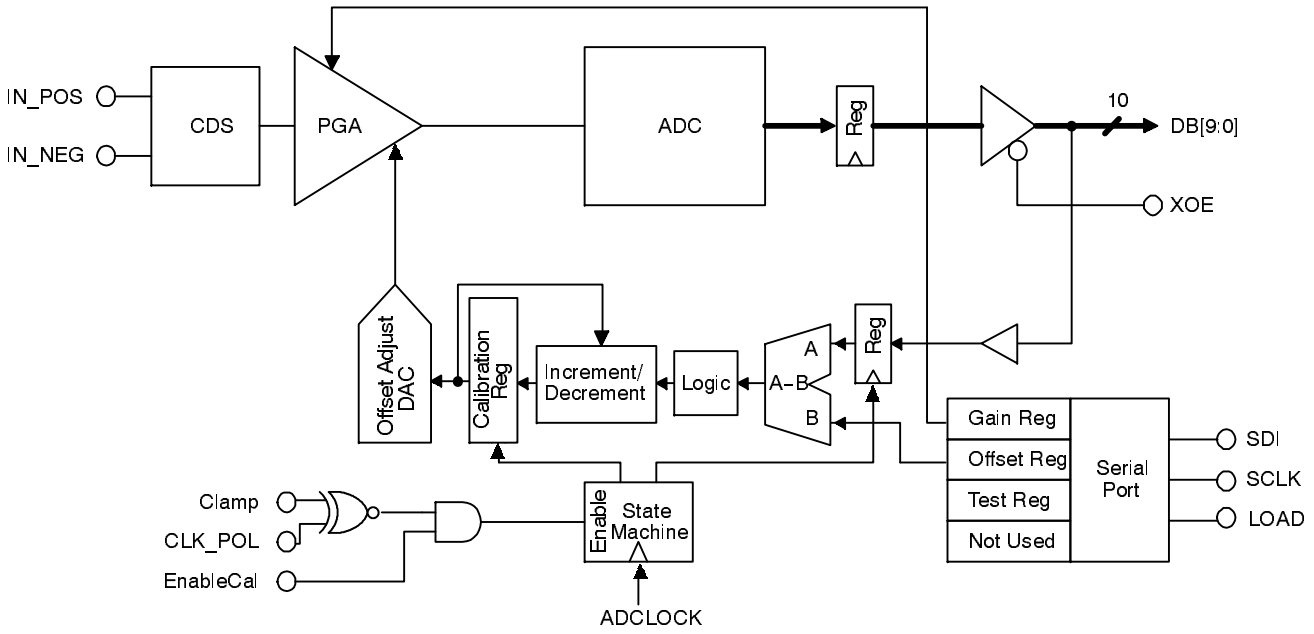


Figure 7. Offset Calibration Loop

Analog To Digital Converter

The analog-to-digital converter is based upon a two-step sub-ranging flash converter architecture with a built in track and hold input stage. The ADC conversion is controlled by an internally generated signal, ADCLK (see *Figure 5).* The ADC tracks the output of the CDS/PGA while ADCLK is high and holds when ADCLK is low. This allows maximum time for the CDS/PGA output to settle to its final value before being sampled. The conversion is then performed and the parallel output is updated, after a 2.5 cycle pipeline delay, on the rising edge of RSTCCD. The pipeline delay of the entire XRD4460/XRD44L60 is 4 clock cycles. The references of the ADC can be generated internally or external voltages can be applied. The internal reference values are set by a resistor divider between V_{DD} and GND. To enable the internal reference, connect V_{RTO} to V_{RT} and connect V_{RBO} to V_{RB}. To maximize the performance of the XRD4460/XRD44L60, the internal references should be used and decoupled to GND. Although the internal references have been set to maximize the performance of the CDS/PGA channel, some applications may require other reference values. To use external references, drive the V_{RT} and V_{RB} pins directly with the desired voltages, and leave V_{RBO} and V_{RTO} open (NC). The ADC parallel output bus is equipped with a high impedance capability, controlled by $\overline{OE}$. The outputs are enabled when $\overline{OE}$ is low.

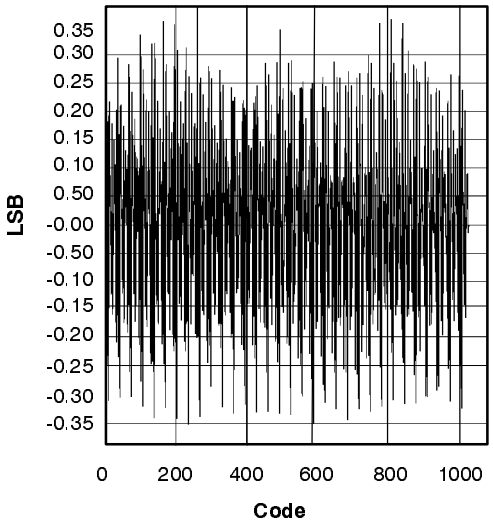


Figure 8. ADC Core Differential Non-Linearity (DNL)

Input Serial Port

A three wire serial interface is used to control the PGA code register and the offset register (there are also two test registers which should not be modified). The shift register is 10 bits long. The first two bits loaded in the shift register are the address bits for which internal register is to get updated, the following eight bits are the data (MSB first, LSB last). The port is controlled by the SCLK, LOAD and SDI pins. To enable the shift register the LOAD pin must be held low. When load is high, SCLK is internally disabled. Since SCLK is gated by LOAD, SCLK can be a continuously running clock signal, but this will increase system noise. The data at SDI is strobed into the shift register on the rising edges of SCLK. The addressed internal register is updated when the LOAD signal goes high (see *Figure 9*).

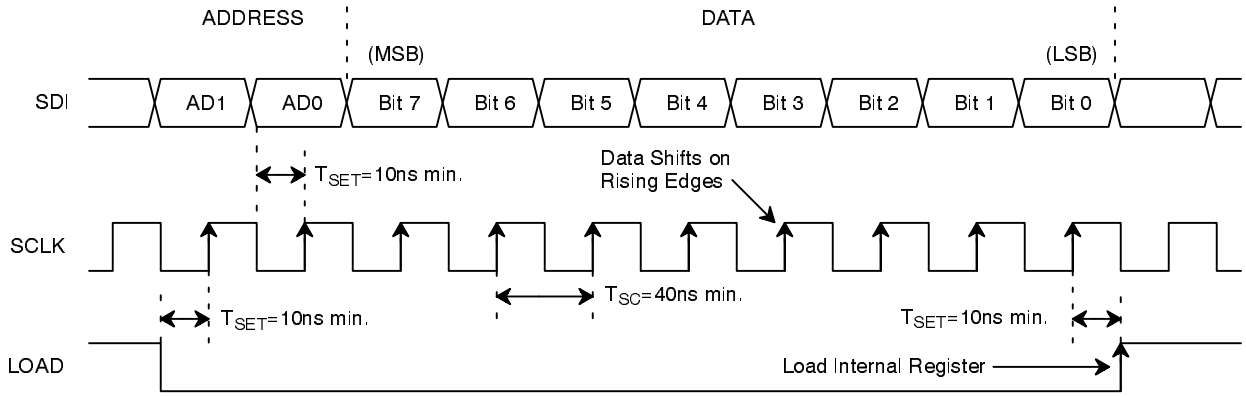


Figure 9. Serial Port Timing

The following truth table gives the address for the serial port registers.

AD1	AD0	Register
0	0	PGA Code
0	1	Offset Code
1	0	Test (see using Test Vin)
1	1	Unused

Table 3. Serial Port Truth Table

Stand By Mode (Power Down)

The $\overline{\text{STBY1}}$ and $\overline{\text{STBY2}}$ pins should connected together and treated as a single control pin (they are separated for Exar factory test purposes). Pulling these pins low puts the chip in the low power, stand-by mode. In this mode all sampling and conversions stop, the digital outputs go into the high impedance state and the power supply current drops to under 50μA.

Chip Reset

When the reset pin is forced high all the internal control registers are set to reset values. The chip also has an internal power-on-reset function to ensure reset conditions are established when the chip is first powered up. The reset values are:

Gain register set to minimum gain (code 00000000).

Offset register set to 08h (code 00001000).

Offset calibration register set to uncalibrated state.

ADC output register set to 000h (code 0000000000).

CDS Clock Polarity

The CLK_POL pin is used to determine the polarity of the CDS clocks (SHD, SHP, CLAMP) (see *Figure 10* and *Figure 11).*

When CLK_POL is high:

CLAMP is active high.

Falling edge of SHP samples pixel black level.

Falling edge of SHD samples pixel data.

RSTCCD high disconnects input.

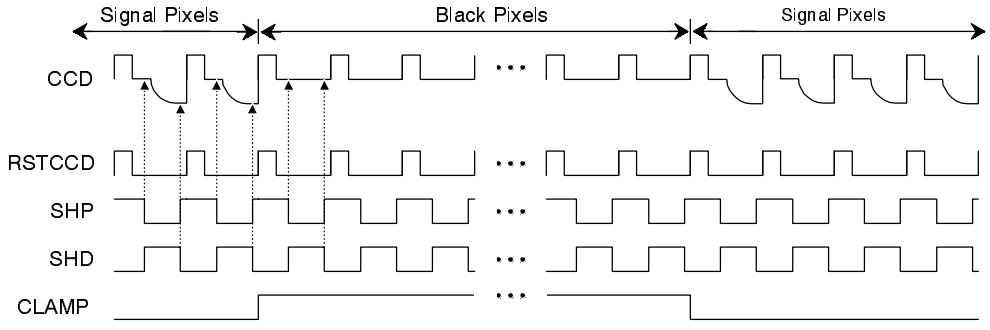


Figure 10. CDS Timing (With CLK_POL=High)

When CLK_POL is low:

CLAMP is active low.

Rising edge of SHP samples pixel black level.

Rising edge of SHD samples pixel data.

RSTCCD high disconnects input.

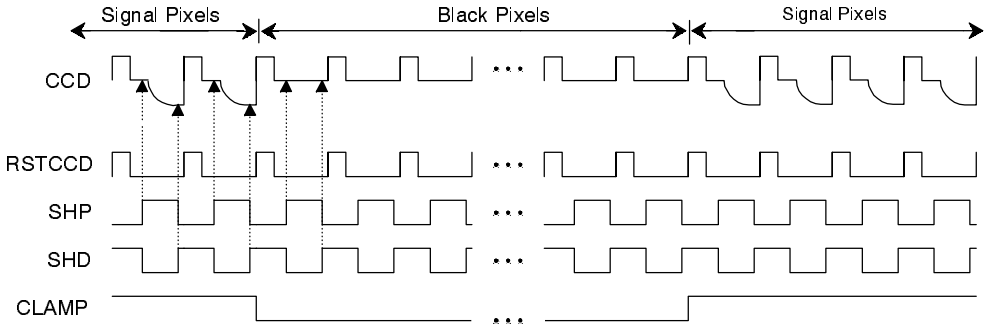


Figure 11. CDS Timing (with CLK_POL=Low)

Using TestVin (pin 20)

The TestVin pin allows access to the input of the ADC, or it can be used to monitor the CDS/PGA output. The TestVin pin accesses the ADC input node through switch S1 (see Figure 12). This switch is controlled by Bit3 of the serial port Test register. When Bit3 of the test register is high, switch S1 is “ON” and the TestVin pin can be used to access the ADC input/PGA output. When Bit3 of the test register is low, switch S1 is “OFF” and the TestVin pin is disconnected from the ADC input/PGA output.

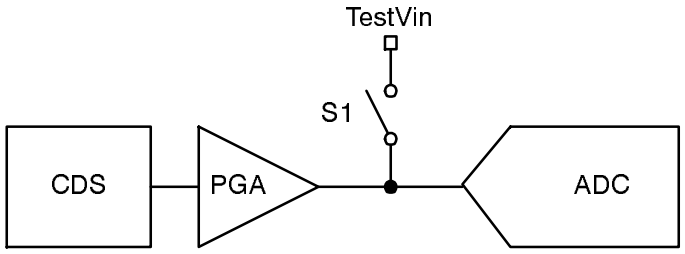


Figure 12. Using TestVin to access PGA output & ADC input.

Mode	AD1	AD0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TestVin	1	0	0	0	0	1	1	0	0	0
Normal	1	0	0	0	0	1	0	0	0	0

Table 4. Serial port data to use TestVin.

To use TestVin as an auxiliary ADC input force $\overline{STBY2}$=low and $\overline{STBY1}$=high. This will disable the CDS/PGA and leave the ADC operating. The ADC clock is generated from the RSTCCD and SHP clocks. The CLK_POL pin controls the clock polarity as shown in Figure 13 & Figure 14.

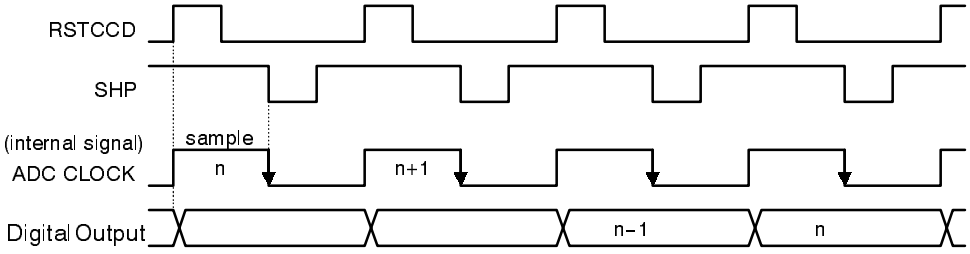


Figure 13. ADC timing with CLK_POL=high

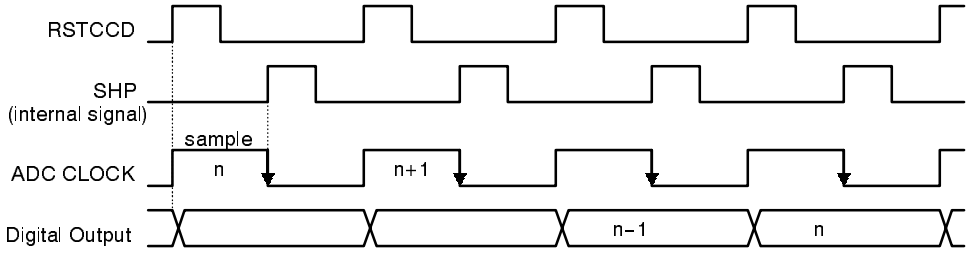


Figure 14. ADC timing with CLK_POL=low

When using $TEST_{VIN}$ as the A/D input, the offset calibration should be disabled. This is accomplished by either not activating the CLAMP control pin or by pulling the EnableCal pin low. Either of these methods will protect the data in the internal calibration register.

To use TestVin to monitor the PGA output both $\overline{STBY1}$ $\overline{STBY2}$ must be high. Please note that PG performance will degrade when PGA output is probed or used as an output. The PGA output signal is discontinuous between pixels, i.e. the waveform is switched in and out.

Digital Output Power Supplies

The DV_{DD} and DGND pins supply power to the digital output drivers for pins DB[9:0], UNDER, and OVER. DV_{DD} is isolated from V_{DD} so it can be at a voltage level less than or equal to V_{DD}. This allows the digital outputs to interface with advanced digital ASICs requiring reduced supply voltages. For example V_{DD} can be 5.0 or 3.3V, while DV_{DD} is 2.5V.

Systems which use the same voltage level for both analog and digital power supplies can take advantage of the isolated DV_{DD} & DGND pins to reduce system noise. The output drivers create large supply transients as they switch. Therefore DV_{DD} and DGND should be routed separately from the analog V_{DD} & GND to avoid injecting this noise into the analog power network (see *Figure 15.*)

Power Supply Sequencing

There are no power supply sequencing issues if DV_{DD} and V_{DD} of the XRD4460/44L60 are driven from the same supply. When DV_{DD} and V_{DD} are driven separately, V_{DD} must come up at the same time or before DV_{DD}, and go down at the same time or after DV_{DD}. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DV_{DD} and V_{DD}. An external diode (5082-2235) layed out close to the converter from DV_{DD} to V_{DD} prevents damage from occurring when power is cycled incorrectly.

Note: *V_{DD} must be greater than or equal to DV_{DD} or the source-body diodes will be forward based.*

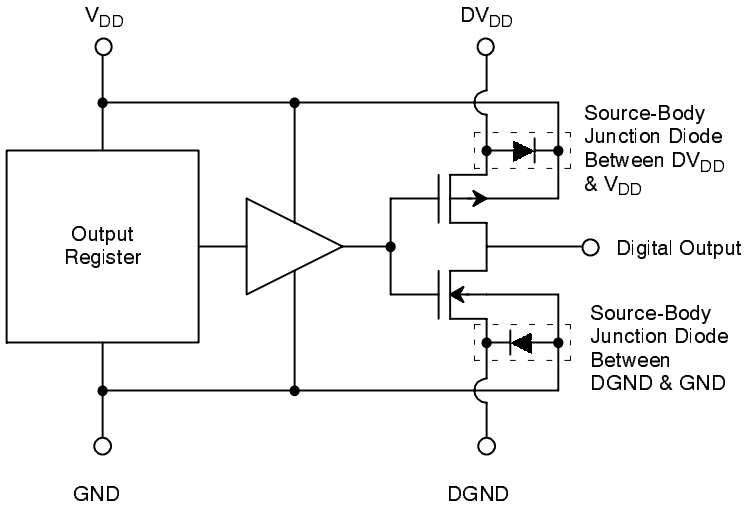


Figure 15. DV_{DD} & DGND Digital Output Power Supplies

General Power Supply and Board Design Issues

All of the GND pins, other than DGND, are tied to the substrate and should be connected directly to the analog ground plane under the XRD4460/XRD44L60. The V_{DD}'s should be supplied from a low noise, well filtered regulator which derives the power supply voltage from the CCD power supply. All of the V_{DD} pins are analog power supplies and should be locally decoupled to the nearest GND pin with a 0.01µF, high frequency capacitor. DV_{DD} and DGND are the power supplies for the digital outputs and should be locally decoupled. DV_{DD} and DGND should be connected to the same power supply network as the digital ASIC which receives the XRD4460/XRD44L60 data.

In general, all traces leading to the XRD4460/XRD44L60 should be as short as possible to minimize signal crosstalk and high frequency digital signals from feeding into sensitive analog inputs. The two CCD inputs, In_Pos and In_Neg, should be routed as fully differential signals and should be shielded and matched. Efforts should be made to minimize the board leakage currents on In_Pos and In_Neg since these nodes are AC coupled from the CCD to the XRD4460/XRD44L60. The digital output traces should be as short as possible to minimize the capacitive loading on the output drivers (see *Figure 16.*)

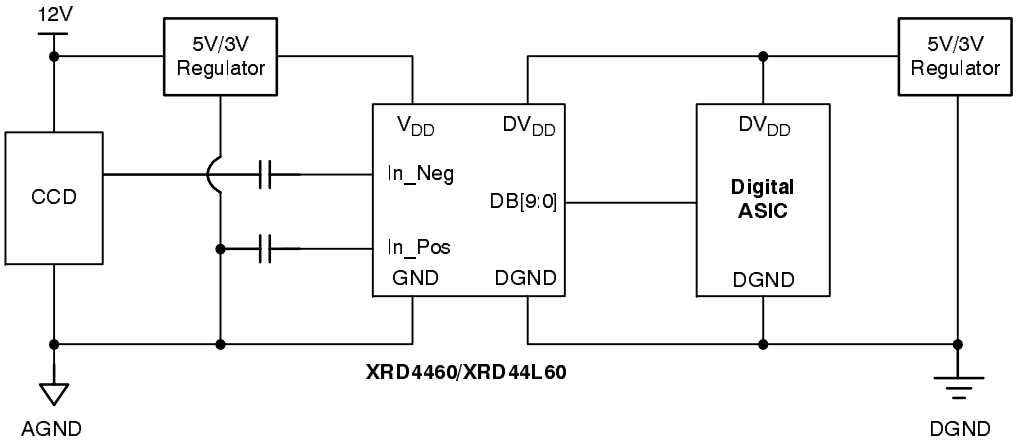


Figure 16. XRD4460/XRD44L60 Power Supply Connections

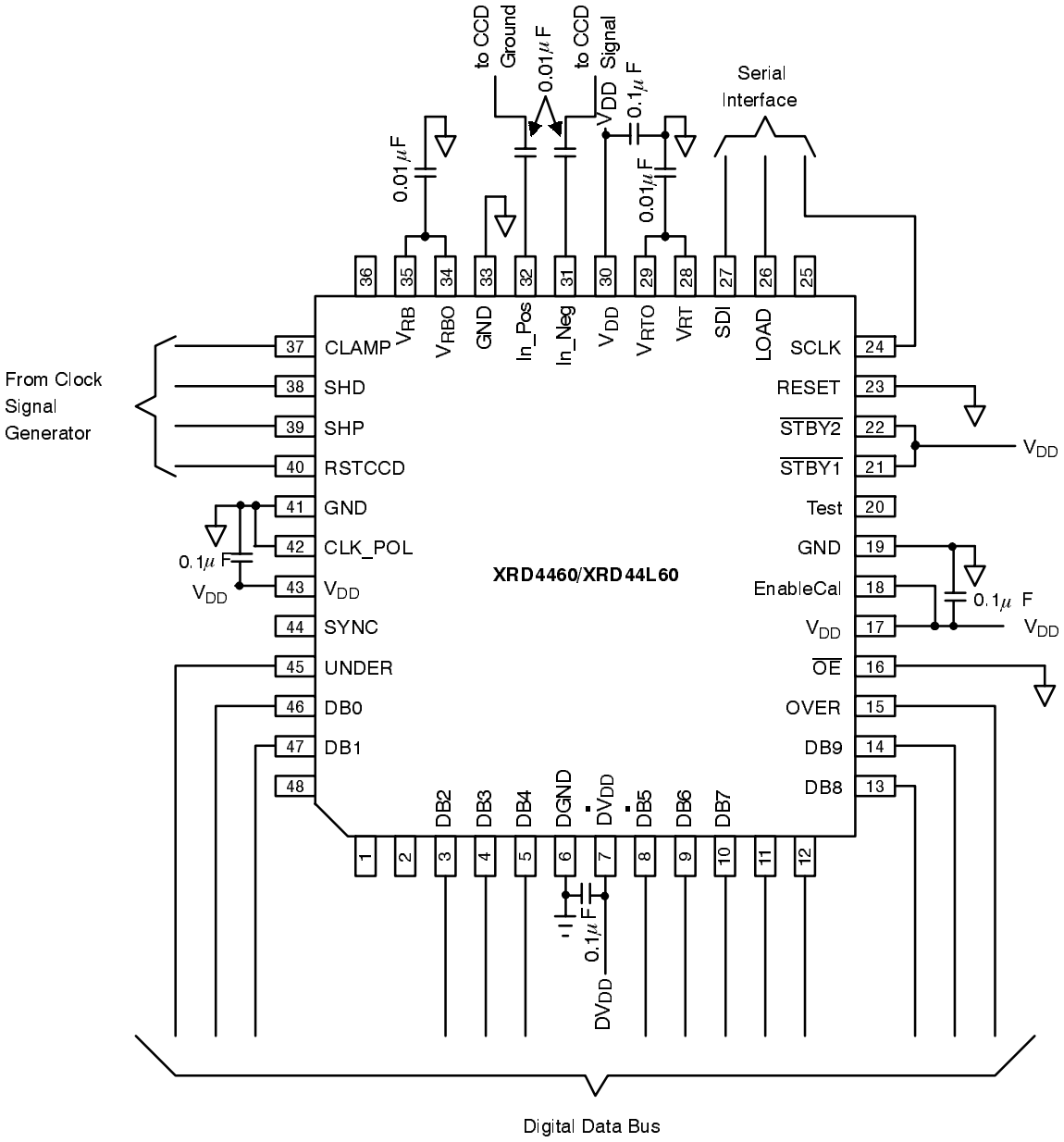


Figure 17. XRD4460/XRD44L60 Application Schematic

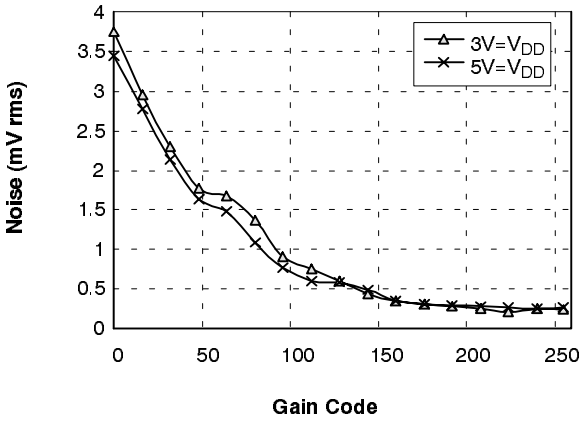


Figure 18. Input Referred Noise vs Gain Code, F_S=16MSPS

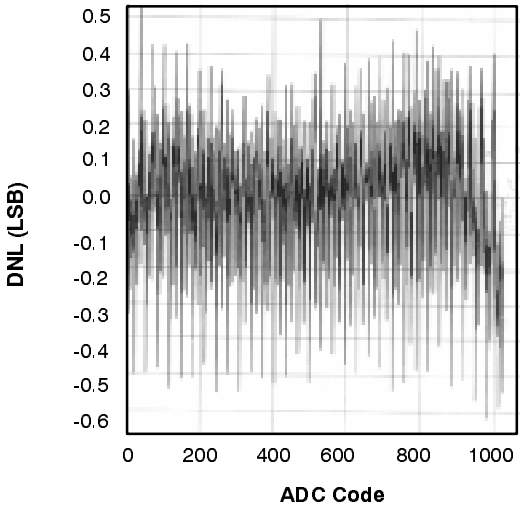


Figure 19. DNL_S for the entire XRD4460

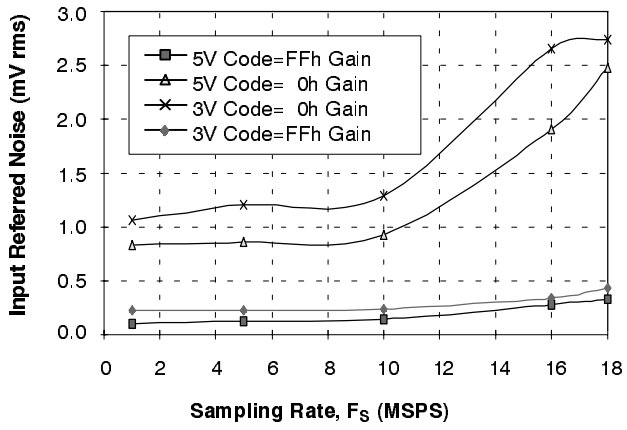


Figure 20. Input Referred Noise at Gain Code FFh and 0 vs Sampling Rate

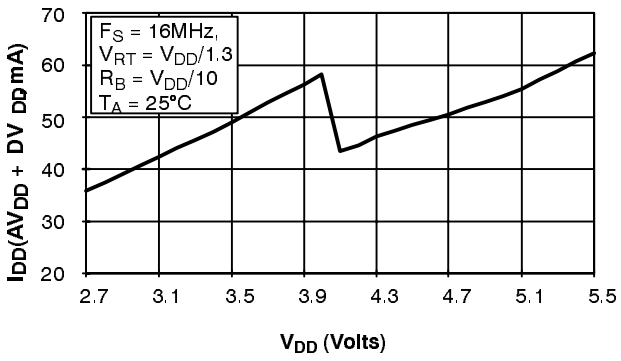


Figure 21. I_{DD} vs V_{DD} Shows the Internal Regulation of V_{DD}

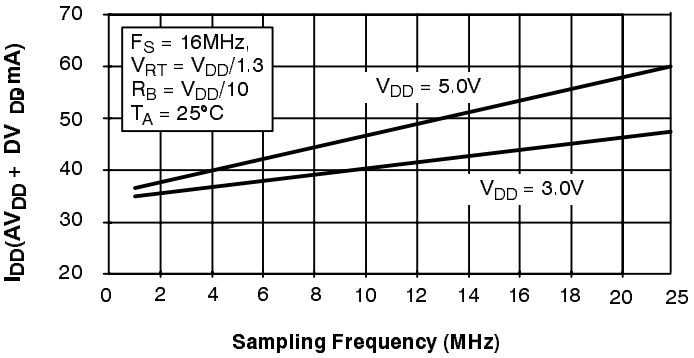


Figure 22. I_{DD} vs Sample Rate

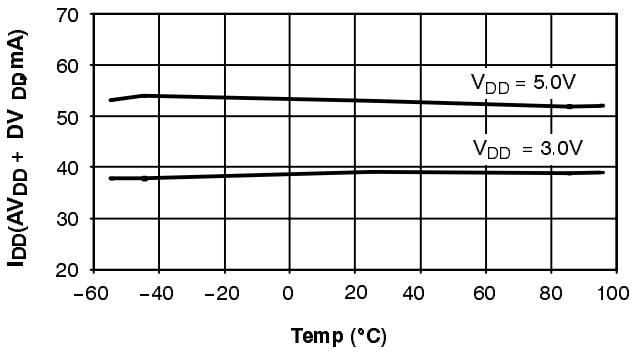


Figure 23. I_{DD} vs Temperature, F_S=16MSPS, V_{RT}=V_{DD}/1.3, V_{RB}=V_{DD}/10

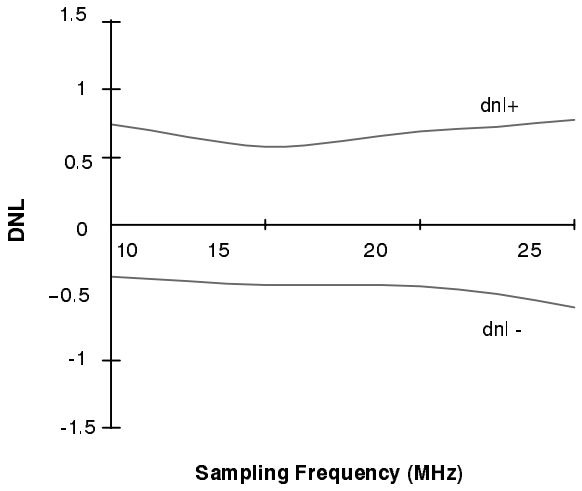
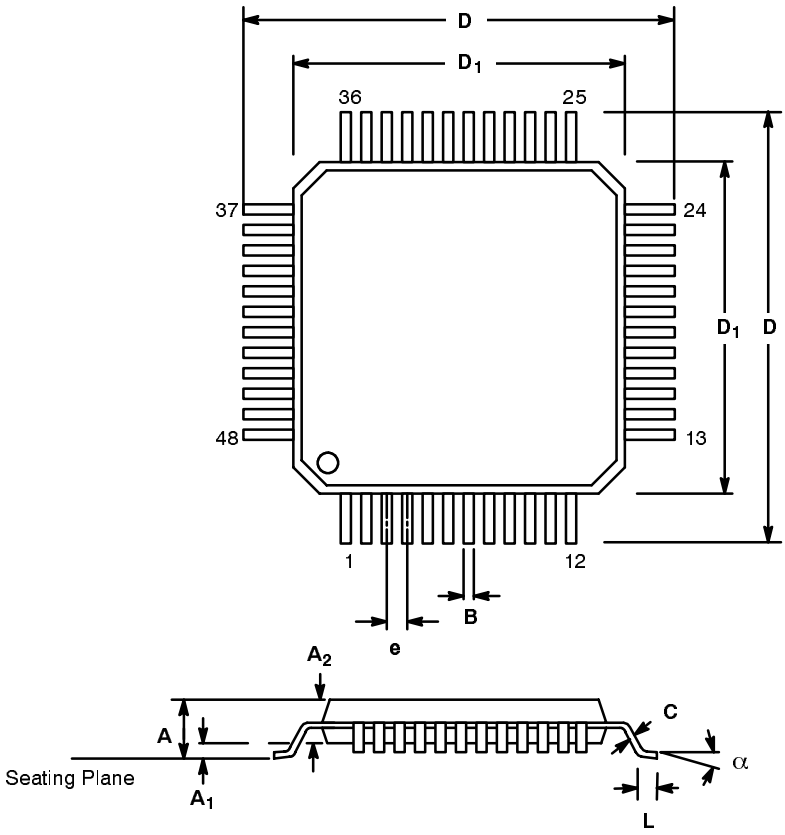


Figure 24. XRD44L60 DNL vs Sampling Frequecy, V_{DD} = 3V

48 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.0 mm, TQFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column