DATA SHEET

TEA6886HL
Up-level Car radio Analog Signal Processor (CASP)

Product specification
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Philips Semiconductors

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CONTENTS

1 FEATURES

1.1 General

- I^2C-bus compatible
- Digital alignment/adjustment via I^2C-bus:
  - FM noise blanker sensitivity
  - FM stereo noise canceller
  - FM High Cut Control (HCC)
  - FM stereo separation.
- FM audio processing hold for RDS updating; holds the detectors for the FM weak signal processing in their present state
- FM bandwidth limiting; limits the bandwidth of the FM audio signal with external capacitors
- AM stereo input; AM stereo audio can be fed in at the pins for the de-emphasis capacitors; this will provide 8 dB of gain to the AM audio.

1.2 Stereo decoder and noise blanking

- FM stereo decoder
- Accepts FM multiplex signals and AM audio at input
- Pilot detector and pilot canceller
- De-emphasis selectable between 75 and 50 μs
- AM noise blanker: impulse noise detector and an audio hold.

1.3 Weak signal processing

- FM weak signal processing: six signal condition detectors, soft mute, stereo noise canceller (blend), and high cut control (roll-off).

1.4 Audio pre-amplifier

- Source selector for 6 sources: 2 stereo inputs external (channels A and B), 1 symmetrical stereo input (channel C), 1 symmetrical mono input (D), 1 internal stereo input (AM or FM), and 1 chime/diagnostic mono input
- Volume 1 control from +20 to –56 dB in 1 dB steps; programmable 20 dB loudness control included
- Volume 2 control from 0 to –56 dB in 1 dB steps, –56, –58.5, –62, –68 dB and mute
- Programmable loudness control with bass boost as well as bass and treble boost
- Treble control from –14 to +14 dB in 2 dB steps
- Bass control from –18 to +18 dB in 2 dB steps with selectable characteristic
- Analog Step Interpolation (ASI) minimizes pops by smoothing out the transitions in the audio signal when a switch is made
- Audio Blend Control (ABC) minimizes pops by automatically incrementing the volume and loudness controls through each step between their present settings and the new settings
- Rear Seat Audio (RSA) can select different sources for the front and rear speakers
- Chime input: can be sent to any audio output, at any volume level
- Chime adder circuit: chime input can also be summed with left front and/or right front audio, or be turned off.

2 GENERAL DESCRIPTION

The TEA6886HL is a monolithic bipolar integrated circuit providing the stereo decoder function and ignition noise blanking facility combined with source selector and tone/volume control for AM/FM car radio applications. The device operates with a power supply voltage range from 7.8 to 9.2 V and a typical current consumption of 40 mA.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6886HL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.8	8.5	9.2	V
I_{CC}	supply current		32	40	48	mA
Stereo decoder path						
S/N	signal-to-noise ratio		–	78	–	dB
THD	total harmonic distortion		–	0.1	–	%
α_{cs}	channel separation		40	–	–	dB
$V_{o(rms)}$	output voltage level at ROPO and LOPO (RMS value)	FM: 91% modulation; AM: 100% modulation; f_{mod} = 400 Hz	840	950	1060	mV
Tone volume control						
$V_{o(max)(rms)}$	maximum output voltage level at LF, LR, RF and RR (RMS value)	V_{CC} = 8.5 V; THD ≤ 0.1%	2000	–	–	mV
G_v	voltage gain	1 dB steps	–112	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–18	–	+18	dB
G_{treble}	treble control		–14	–	+14	dB
$G_{step(treble, bass)}$	step resolution (bass and treble)		–	2	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	107	–	dB
THD	total harmonic distortion	$V_{o(rms)}$ = 1.0 V; G_v = 0 dB	–	0.01	–	%
RR_{100}	ripple rejection	V_{ripple} < 200 mV (RMS); f = 100 Hz; G_v = 0 dB	–	70	–	dB
CMRR	common mode rejection ratio differential stereo input		48	53	–	dB

5 BLOCK DIAGRAM

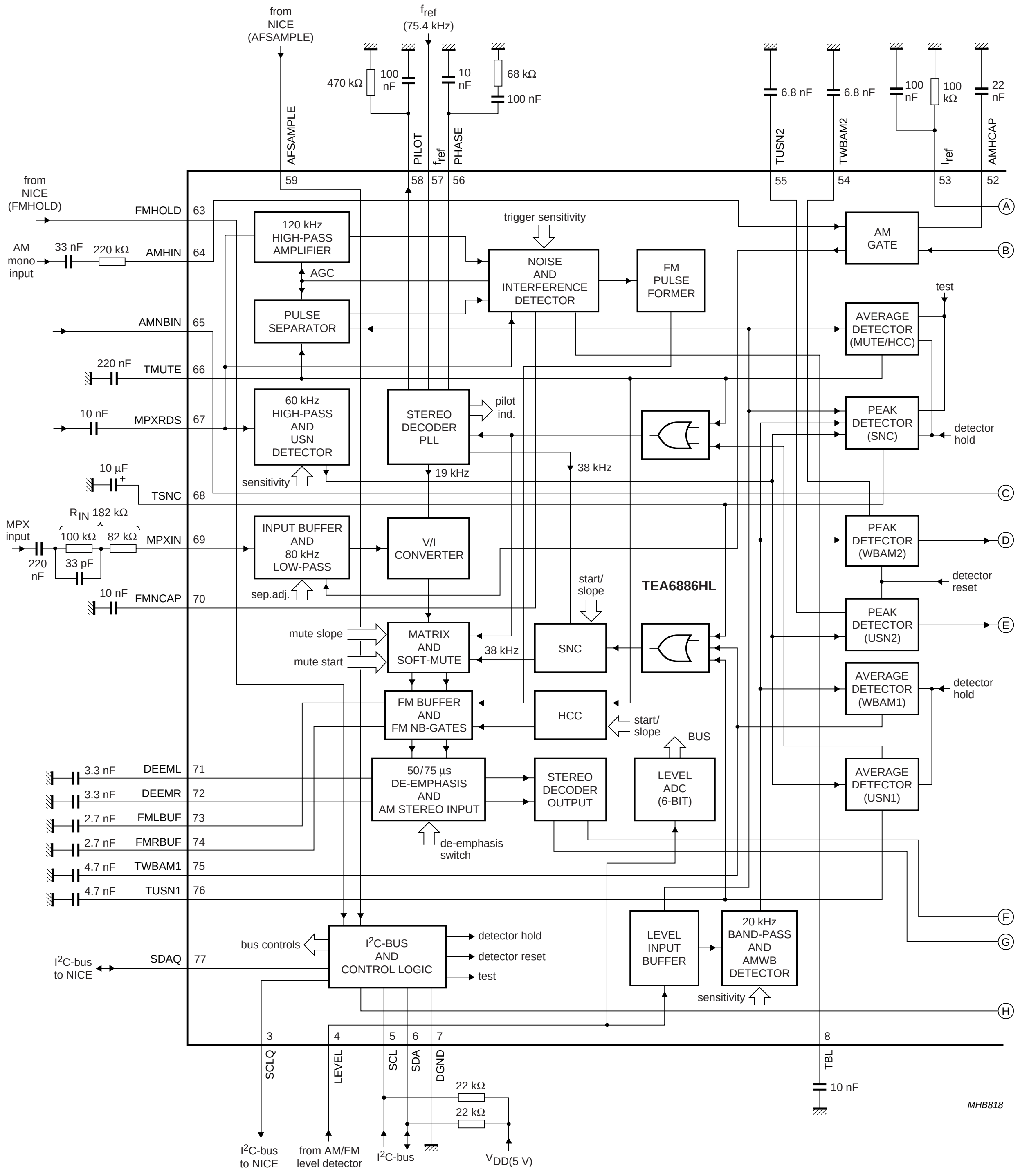


Fig.1 Block diagram (continued in Fig.2).

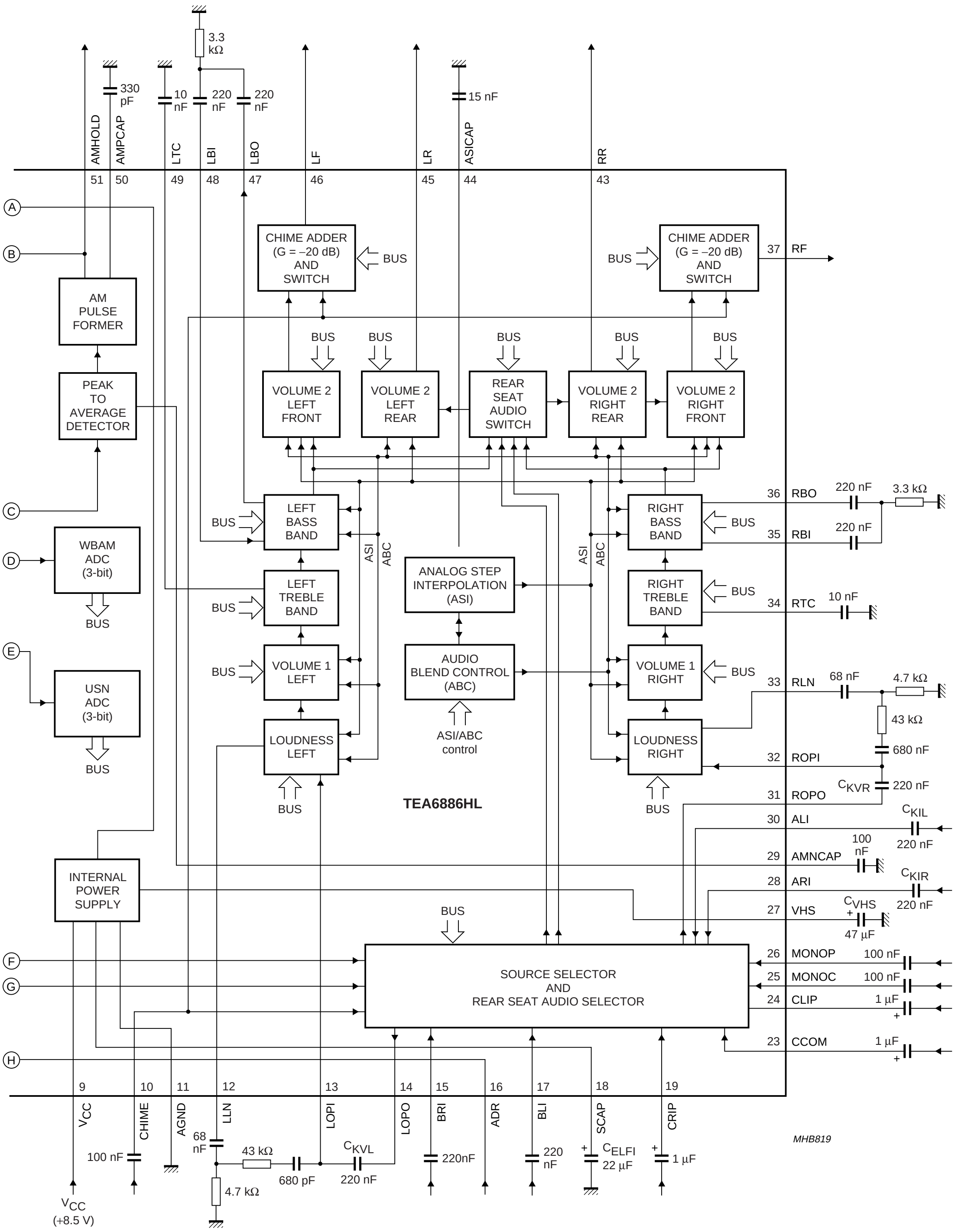


Fig.2 Block diagram (continued from Fig.1).

6 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
SCLQ	3	clock output (to TEA6840H)
LEVEL	4	FM and AM level input (from TEA6840H)
SCL	5	I^2C-bus clock input
SDA	6	I^2C-bus data input/output
DGND	7	digital ground
TBL	8	time constant for FM modulation detector
V_{CC}	9	supply voltage
CHIME	10	chime tone input
AGND	11	analog ground
LLN	12	loudness left network
LOPI	13	left option port input (terminal impedance typical 100 kΩ)
LOPO	14	left option port output
BRI	15	channel B right stereo input (terminal impedance typical 100 kΩ)
ADR	16	address select input
BLI	17	channel B left stereo input (terminal impedance typical 100 kΩ)
SCAP	18	supply filter capacitor
CRIP	19	channel C right symmetrical input (terminal impedance typical 30 kΩ)
n.c.	20	not connected
n.c.	21	not connected
n.c.	22	not connected
CCOM	23	channel C common input (terminal impedance typical 30 kΩ)
CLIP	24	channel C left symmetrical input (terminal impedance typical 30 kΩ)
MONOC	25	mono common input (terminal impedance typical 30 kΩ)
MONOP	26	mono symmetrical input (terminal impedance typical 30 kΩ)
VHS	27	half supply filter capacitor
ARI	28	channel A right stereo input (terminal impedance typical 100 kΩ)
AMNCAP	29	peak-to-average detector capacitor for AM noise blanker
ALI	30	channel A left stereo input (terminal impedance typical 100 kΩ)
ROPO	31	right option port output
ROPI	32	right option port input (terminal impedance typical 100 kΩ)
RLN	33	loudness right network
RTC	34	right treble capacitor
RBI	35	right bass network input
RBO	36	right bass network output
RF	37	right front output
n.c.	38	not connected
n.c.	39	not connected
n.c.	40	not connected

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
n.c.	42	not connected
RR	43	right rear output
ASICAP	44	analog step interpolate capacitor
LR	45	left rear output
LF	46	left front output
LBO	47	left bass network output
LBI	48	left bass network input
LTC	49	left treble capacitor
AMPCAP	50	AM blanking time capacitor
AMHOLD	51	AM noise blanker flag
AMHCAP	52	AM noise blanker hold capacitor
I_{ref}	53	temperature independent reference current
TWBAM2	54	time constant for AM wideband peak detector
TUSN2	55	time constant for ultrasonic noise peak detector
PHASE	56	phase detector
f_{ref}	57	frequency reference input (75.4 kHz from TEA6840H)
PILOT	58	pilot on/off output
AFSAMPLE	59	reset for multipath detector (from TEA6840H for RDS update)
n.c.	60	not connected
n.c.	61	not connected
n.c.	62	not connected
FMHOLD	63	FM audio processing hold input (from TEA6840H for RDS update)
AMHIN	64	AM signal input (from TEA6840H)
AMNBIN	65	AM noise blanker input (from TEA6840H)
TMUTE	66	time constant for soft mute
MPXRDS	67	unmuted MPX input (from TEA6840H for RDS update)
TSNC	68	time constant for stereo noise canceller
MPXIN	69	MPX input (from TEA6840H)
FMNCAP	70	FM noise detector capacitor
DEEML	71	left de-emphasis capacitor
DEEMR	72	right de-emphasis capacitor
FMLBUF	73	left AM/FM audio buffer capacitor
FMRBUF	74	right AM/FM audio buffer capacitor
TWBAM1	75	time constant for AM wideband average detector
TUSN1	76	time constant for ultrasonic noise average detector
SDAQ	77	data input/output (to TEA6840H)
n.c.	78	not connected
n.c.	79	not connected
n.c.	80	not connected

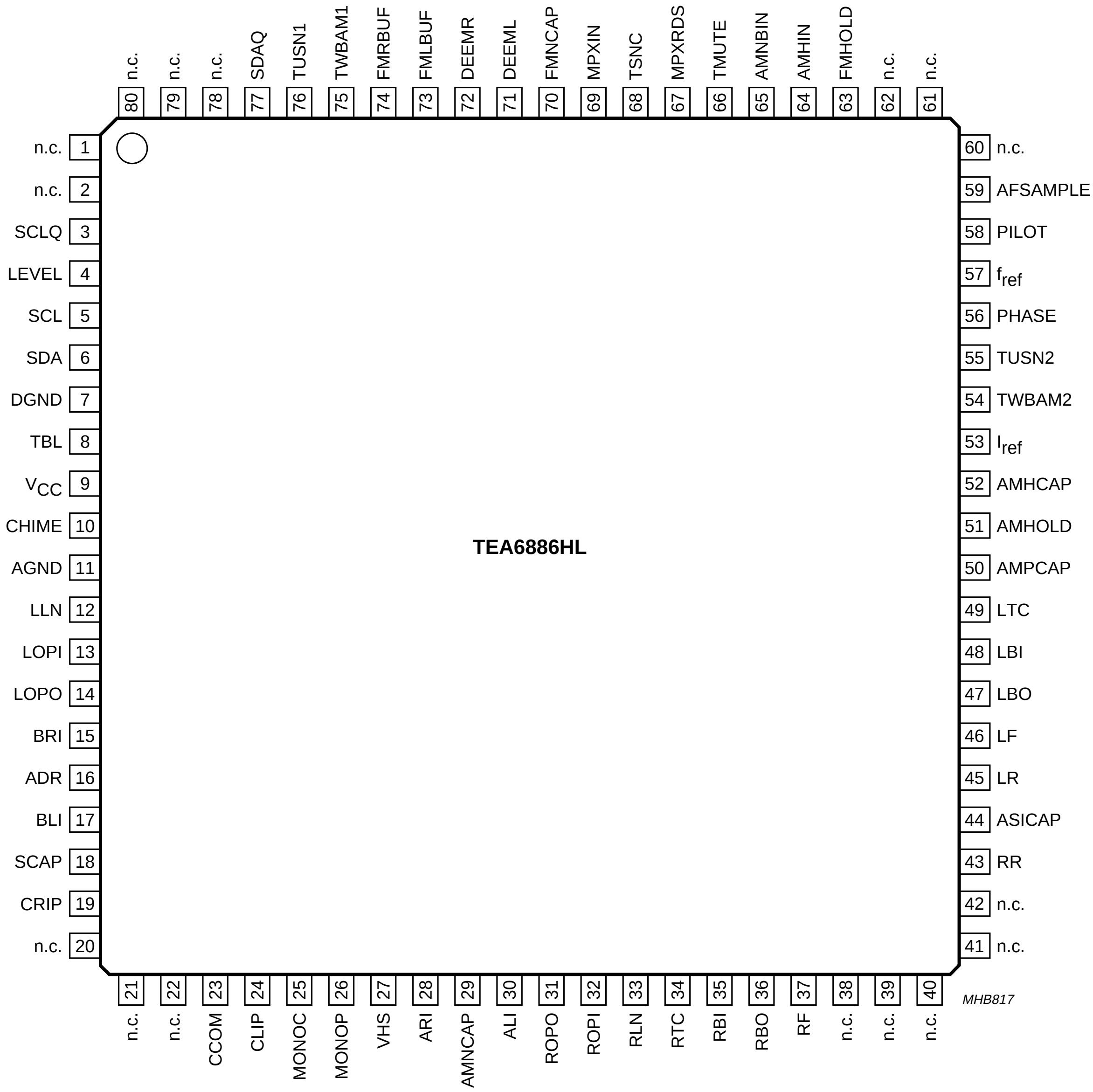


Fig.3 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Stereo decoder

The MPX input is the null-node of an operational amplifier with internal feedback resistor. Adapting the stereo decoder input to the level of the MPX signal, coming from the FM demodulator output, is realized by the value of the input series resistor R_{IN}. To this input a second source (AM detector output) can be fed by current addition.

The input amplifier is followed by an integrated 4th-order Bessel low-pass filter with a cut-off frequency of 80 kHz. It provides the necessary signal delay for FM noise blanking and damping of high frequency interference at the stereo decoder input.

The output signal of this filter is fed to the soft mute control circuitry, the output is voltage-to-current converted and then fed to the phase detector, pilot detector and pilot canceller circuits, contained in the stereo decoder PLL block. A PLL is used for regeneration of the 38 kHz subcarrier. The fully integrated oscillator is adjusted by means of a digital auxiliary PLL into the capture range of the main PLL. The auxiliary PLL needs an external reference frequency (75.4 kHz) which is provided by the TEA6840H. The required 19 and 38 kHz signals are generated by division of the oscillator output signal in a logic circuit. The 19 kHz quadrature phase signal is fed to the 19 kHz phase detector, where it is compared with the incoming pilot tone. The DC output signal of the phase detector controls the oscillator (PLL).

The pilot present detector is driven by an internally generated in-phase 19 kHz signal. Its pilot dependent DC output voltage is fed to a threshold switch, which activates the pilot indicator bit and switches the stereo decoder to stereo operation. The same DC voltage is used to control the amplitude of an anti-phase internally generated 19 kHz signal. The pilot tone is compensated by this anti-phase 19 kHz signal in the pilot canceller.

The pilot cancelled signal is fed to the matrix. There, the side signal is demodulated and combined with the main signal to the left and right audio channels. Compensation for roll-off in the incoming MPX signal caused by the IF filters and the FM demodulator is typically realized by an external compensation network at pin MPXIN, individual alignment is achieved by I^2C-bus controlled amplification of the side signal (DAA). A smooth mono-to-stereo takeover is achieved by controlling the efficiency of the matrix with the help of the SNC peak detector.

The matrix is followed by the FM noise suppression gates, which are combined with FM single poles and High Cut Control (HCC).

The single pole is defined by internal resistors and external capacitors. Audio is fed from the gate circuits to the switchable de-emphasis, where the demodulated AM stereo signal can be fed in. After de-emphasis the signal passes to the output buffers and is fed to the radio input of the source selector. For HCC, the time constant of the single pole contained in the output buffer can be changed to higher values. This function is controlled by an average detector contained in the multipath and fading detector.

7.2 FM noise blanker

The input of the ignition noise blanker is coupled to the MPXRDS input signal and to the LEVEL input. Both signals are fed via separate 120 kHz filters and rectifiers to an adder circuit. The output signal of the adder circuit is fed in parallel to the noise detector and the interference detector. The noise detector is a negative peak detector. Its output controls the trigger sensitivity (prevention of false triggering at noisy input signals) and the gain of the MPX high-pass filter. The output of the interference detector, when receiving a steep pulse, fires a single-shot trigger circuit, contained in the pulse former circuitry. The time constant of the single-shot trigger circuit is defined by an internal capacitor, and its output activates the blanking gates in the audio.

7.3 AM noise blanker

The AM noise blanking pulse is derived from the AM audio signal which is fed into pin AMNBIN with the help of a peak-to-average comparator. The blanking time is set by a pulse former with external capacitor. The blanking pulse is fed to the gate in the AM audio path and out at pin AMHOLD to operate the gate built into the external AM stereo processor.

7.4 Multipath/fading detection and weak signal control

For FM signal quality dependent controls there is a built-in combination of six detectors. These detectors are driven by the level information direct, by the AC components on the level via a 20 kHz band-pass filter (AM wideband) or by the high notes present at the FM demodulator output via a 60 kHz high-pass filter (ultrasonic noise). The relationship between the DC level and the AC components is programmable by the I^2C-bus (2 bits each). The output of the level buffer, AM wideband detector and ultrasonic noise detector are analog-to-digital converted and readable by the I^2C-bus.

For the period of fast RDS updating soft mute, SNC and HCC can be put on hold. The AM wideband peak detector and the ultrasonic noise peak detector are reset by a switch signal delivered from the TEA6840H via pin FMHOLD.

The six separate detecting circuits are as follows:

1. The AM wideband noise peak detector is driven from a 20 kHz band-pass filter connected to the level buffer output. The time constant is defined by an external capacitor connected to pin TWBAM2. The output voltage of the detector is analog-to-digital converted by a 3-bit ADC.
2. The AM wideband noise average detector is driven from a 20 kHz band-pass filter connected to the level buffer output. The time constant is defined by an external capacitor connected to pin TWBAM1. The output of the detector is connected to the Stereo Noise Control (SNC) circuit.
3. The ultrasonic noise peak detector is driven from a 60 kHz high-pass filter connected to the MPX signal from pin MPXRDS. The time constant is defined by an external capacitor connected to pin TUSN2. The output voltage of the detector is analog-to-digital converted by a 3-bit ADC.
4. The ultrasonic noise average detector is driven from a 60 kHz high-pass filter connected to the MPX signal from pin MPXRDS. The time constant is defined by an external capacitor connected to pin TUSN1. The output of the detector is connected to soft mute control and stereo noise control circuits.
5. For soft mute and high cut control purposes an average detector with an externally defined time constant (TMUTE) is provided. The detector is driven by level output only. Soft mute and high cut control can be switched off via the I^2C-bus.
6. The stereo noise control peak detector with an externally defined time constant (TSNC) is driven by DC level output, AM wideband and ultrasonic noise outputs. It provides the stereo blend facility (SNC). The starting point and slope of the stereo blend can be chosen via the I^2C-bus controlled reference voltage.

7.5 Tone/volume control

The tone/volume control part consists of the following functions:

- Source selector
- Loudness
- Volume 1
- Treble
- Bass
- Volume 2
- Rear Seat Audio (RSA) selector
- Chime adder
- Analog step interpolation
- Audio blend control.

The stages loudness, volume 1, bass and volume 2 include the Analog Step Interpolation (ASI) function. This minimizes pops by smoothing out the transitions in the audio signal during switching. The transition time is I^2C-bus programmable in a range of 1 : 24 in four steps.

The stages loudness, volume 1 and volume 2 also have the Audio Blend Control (ABC) function. This minimizes pops by automatically incrementing the volume and loudness controls through each step between their present settings and the new settings. The speed of the ABC function is correlated with the transition time of the ASI function.

All stages are controlled via the I^2C-bus.

7.5.1 SOURCE SELECTOR

The source selector allows the selection between 6 sources:

- 2 external stereo inputs (ALI, ARI, BLI and BRI)
- 1 external symmetrical stereo input (CLIP, CRIP and CCOM)
- 1 external symmetrical mono input (MONOP and MONON)
- 1 internal stereo input (AM/FM)
- 1 chime/diagnostic mono input (CHIME).

A chime input signal can be sent to any audio output, at any volume level, via the chime/diagnostic mono input.

7.5.2 LOUDNESS

The output of the source selector is fed into the loudness circuit via the external capacitor C_{KVL} (between pins LOPO and LOPI) and C_{KVR} (between pins ROPO and ROPI). Depending on the external circuits for the left and the right channel, only a bass boost or bass and treble boost is available. The external circuits illustrated in Figs 13 and 15 will produce the curves illustrated in Figs 14 and 16 (without the influence of C_{KVL} and C_{KVR} respectively).

7.5.3 VOLUME 1

The volume 1 control circuit follows the loudness circuit. The control range of volume 1 is between +20 and –36 dB in steps of 1 dB.

7.5.4 TREBLE

The output signal of the volume 1 control circuit is fed into the treble control stage. The control range is between +14 and –14 dB in steps of 2 dB. Fig.20 shows the control characteristic with external capacitors of 10 nF.

7.5.5 BASS

The bass control is the next stage. The characteristic of the bass curves depends upon the external circuits connected to pins LBO and LBI (left channel) and pins RBO and RBI (right channel) and also upon the setting of bit BSYM (MSB of the bass control byte). When BSYM = 1, an equalizer characteristic is obtained and when BSYM = 0, a shelving characteristic is obtained.

Figures 17 and 18 show the bass curves with an external circuit of 2 × 220 nF capacitors and a resistor of 3.3 kΩ for each channel with different values for BSYM. Figure 19 shows the bass curves with an external capacitor of 47 nF for each channel and BSYM = 0, for boost and cut.

7.5.6 VOLUME 2

The four volume 2 blocks are located at the end of the tone/volume control. In addition to volume control (same settings as volume 2) the balance and fader functions are also performed by individual attenuation offsets for the four attenuators. The control range of these attenuators is 56 dB in steps of 1 dB and the additional steps of –58.5 dB, –62 dB, –68 dB, and a mute step.

7.5.7 RSA SELECTOR

The RSA selector provides the possibility to select an alternative source for the rear channels. In this event rear channels are only controlled by the volume 2 function.

7.5.8 CHIME ADDER

The chime adder circuit enables the chime input signal to be summed with the left front and/or right front audio, or be turned off.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.3	+10	V
V_i	voltage at all pins (except SCL and SDA)	$V_{CC} \leq 10$ V	V_{SS} – 0.3	V_{CC}	V
	voltage at pins SCL and SDA		V_{SS} – 0.3	9.7	V
P_{tot}	total power dissipation		–	480	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage for all pins	note 1	–200	+200	V
		note 2	–2000	+2000	V

Notes

1. Machine model: R = 0 Ω, C = 200 pF.
2. Human body model: R = 1.5 kΩ, C = 100 pF.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	54	K/W

10 CHARACTERISTICS

FM part: input signal $V_{i(MPX)(p-p)}$ = 1.89 V; m = 100% (Δf = ±75 kHz, f_{mod} = 400 Hz); de-emphasis of 75 µs and series resistor at input R_{IN} = 182 kΩ; FM audio measurements are taken at pins LOPO and ROPO. Tone part: R_S = 600 Ω; R_L = 10 kΩ, AC-coupled; C_L = 2.5 nF; CLK = square wave (5 to 0 V) at 100 kHz; stereo source = A channel input; volume 1 attenuator = 0 dB; loudness = 0 dB, off; volume 2 attenuators = 0 dB; bass linear; treble linear; input voltage = 1 V, f = 1 kHz. Tone part audio measurements are taken at RF and LF. V_{CC} = 8.3 to 8.7 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified. This IC shall not radiate noise in the audio system such that it disturbs any other circuit. This IC shall also not be susceptible to the radiation of any other circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.8	8.5	9.2	V
I_{CC}	supply current	V_{CC} = 8.5 V	32	40	48	mA
V_{HS}	half supply voltage	V_{CC} = 8.5 V	3.75	4.25	4.75	V
I_{ref}	reference current	V_{CC} = 8.5 V; R_{ext} = 100 kΩ	35	37	39	µA
FM signal path						
$V_{i(MPX)(p-p)}$	MPX input signal (peak-to-peak value)	R_i = 182 kΩ	–	1.89	–	V
$\Delta V_{i(MPX)}$	overdrive margin of MPX input signal	THD = 1%	6	–	–	dB
I_i	AF input current		–	3.66	–	µA
$I_{i(max)}$	maximum AF input current	THD = 1%	7.32	–	–	µA
$V_{o(rms)}$	AF mono output signal (RMS value)	91% modulation without pilot	890	1000	1110	mV
ΔV_{out}	AF mono channel balance	without pilot; V_{LOPO}/V_{ROPO}	–1	–	+1	dB
α_{cs}	channel separation	aligned setting of data byte 1, bit 0 to bit 3; m = 30% modulation plus 9% pilot				
		L = 1; R = 0	40	47	70	dB
		L = 0; R = 1	40	47	70	dB
THD	total harmonic distortion	$V_{i(MPX)(p-p)}$ = 1.89 V; f_{mod} = 1 kHz without pilot	–	0.1	0.3	%
		$V_{i(MPX)(p-p)}$ = 1.89 V; f_{mod} = 5 kHz				
		L = 1; R = 0	–	0.1	0.3	%
		L = 0; R = 1	–	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 Hz to 15 kHz	75	78	–	dB
α_{19}	pilot signal suppression	f = 19 kHz	40	50	–	dB
α_{38}	subcarrier suppression	f = 38 kHz	35	50	–	dB
α_{57}		f = 57 kHz	40	–	–	dB
α_{76}		f = 76 kHz	50	60	–	dB
IM2	second order intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz; note 1	–	60	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IM3	third order intermodulation for f_{spur} = 1 kHz	f_{mod} = 13 kHz; note 1	–	58	–	dB
$\alpha_{57(RDS)}$	traffic radio (RDS)	f = 57 kHz; note 2	–	70	–	dB
α_{67}	Subsidiary Communication Authorization (SCA)	f = 67 kHz; note 3	70	–	–	dB
α_{114}	Adjacent Channel Interference (ACI)	f = 114 kHz; note 4	–	80	–	dB
α_{190}		f = 190 kHz; note 4	–	70	–	dB
PSRR	power supply ripple rejection	f = 100 Hz; V_{ripple} = 100 mV (RMS)	–	30	–	dB
R_{SDEEML}; R_{SDEEMR}	de-emphasis output source resistance	data byte 3, bit 5 = 1; 75 μs	20	22.7	25.4	kΩ
		data byte 3, bit 5 = 0; 50 μs	13.4	15.2	17	kΩ
I_{FMLBUF}; I_{FMRBUF}	current capacity of FM buffer	$V_{FMLBUF,FMRBUF}$ = 5.5 ±1 V	50	–	200	μA
PLL VCO						
f_{osc}	oscillator frequency		–	228	–	kHz
	frequency range of free running oscillator		190	–	270	kHz
f_{ref}	reference frequency		–	75.4	–	kHz
$V_{i(fref)}$	reference frequency input voltage		30	100	500	mV
$Z_{i(fref)}$	input impedance		100	–	–	kΩ
PLL pilot detector						
$V_{i(pilot)(rms)}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)	stereo on; STIN = 1	–	27	37	mV
		stereo off; STIN = 0	9	22	–	mV
$hys_{(pilot)}$	hysteresis of pilot threshold voltage		–	2	–	dB
V_{PILOT}	switching voltage for external mono control (PILOT)		0.3	–	0.7	V
AM signal path						
V_{LOPO}; V_{ROPO}	AC output voltage at LOPO and ROPO	AMON = 1 and AMST = 0; R_i = 220 kΩ; $V_{iAM(mono)}$ = 250 mV	195	245	295	mV
G_v	AM stereo audio buffer voltage gain	subaddress 0H: AMON = 1 and AMST = 1; input signal at pins DEEML or DEEMR; coupled with 220 nF; $V_{i(DEEML,DEEMR)}$ = 200 mV; f_i = 1 kHz; note 5	7	8	9	dB
$R_{i(DEEML,DEEMR)}$	input resistance for AM stereo left and right	AMON = 1 and AMST = 1; note 6	80	100	120	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Noise blanker						
FM PART						
t_{sup}	interference suppression time		20	30	40	µs
I_{offset}	gate input offset current at pins during suppression pulse duration	during AF suppression time	–	20	50	nA
$I_{ch(FMNCAP)}$	charge current	no input signal; $V_{FMNCAP} = V_{FMNCAP(int)} - 0.7$ V	–16	–12.5	–9.5	µA
$I_{dch(FMNCAP)}$	discharge current	no input signal; $V_{FMNCAP} = V_{FMNCAP(int)} + 0.7$ V	45	70	100	µA
Trigger Threshold Control (TTC), dependency on MPX signal at MPXRDS input						
V_{FMNCAP}	trigger threshold variation voltage	$V_{i(MPXRDS)} = 0$ V	4.5	5	5.5	V
ΔV_{FMNCAP}	trigger threshold voltage	$V_{i(MPXRDS)} = 10$ mV; f = 120 kHz	15	40	80	mV
		$V_{i(MPXRDS)} = 100$ mV; f = 120 kHz	75	100	200	mV
ΔV_{TBL}	trigger threshold variation with audio frequency f = 15 kHz	$V_{i(MPXRDS)} = 670$ mV	–	500	–	mV
Trigger Threshold Control (TTC), dependency on level detector input signal						
V_{FMNCAP}	trigger threshold voltage	$V_{LEVEL(AC)} = 0$ V	4.5	5	5.5	V
ΔV_{FMNCAP}	trigger threshold voltage as a function of $V_{LEVEL(AC)}$	$V_{LEVEL(AC)} = 10$ mV; f = 120 kHz	–	0	–	mV
		$V_{LEVEL(AC)} = 200$ mV; f = 120 kHz	–	40	–	mV
Trigger sensitivity measurement with pulse (on MPX signal) at MPXRDS input						
V_{pulse}	trigger sensitivity	$t_{pulse} = 10$ µs; write mode; data byte 3, bits 6 and 7:				
		NBS1 = 0; NBS0 = 0	–	60	–	mV
		NBS1 = 0; NBS0 = 1	–	100	–	mV
		NBS1 = 1; NBS0 = 0	–	150	–	mV
		NBS1 = 1; NBS0 = 1	–	200	–	mV
Trigger sensitivity measurement with pulse (on level signal) at AM/FM level input						
V_{pulse}	trigger sensitivity	$t_{pulse} = 10$ µs; $V_{LEVEL} = 0.5$ V; write mode; data byte 3, bits 6 and 7:				
		NBS1 = 0; NBS0 = 0	–	250	–	mV
		NBS1 = 0; NBS0 = 1	–	275	–	mV
		NBS1 = 1; NBS0 = 0	–	300	–	mV
		NBS1 = 1; NBS0 = 1	–	320	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM PART						
m_{mod}	trigger threshold		–	140	–	%
$V_{AMPCAP(AC)}$	AF voltage at AMHCAP	$V_{iAM(mono)}$ = 50 mV (RMS); f = 1 kHz	16	22	30	mV
α_{AMGATE}	attenuation of blanking gate	$V_{iAM(mono)}$ = 50 mV (RMS); gate open: internal voltage; gate closed: $V_{AMHOLD(DC)}$ = 4 V; note 7	–60	–70	–80	dB
$t_{sup(AMHOLD)}$	suppression time at AMHOLD	t_{pulse} = 10 µs; repetition rate = 50 Hz; V_{pulse} = 1.7 V (AMNBIN); V_{LEVEL} = 0.5 V	400	500	600	µs
$V_{(AMNCAP)DC}$	detector voltage; $V_{ext(AMNBIN)DC}$ – 0.7 V	$V_{AMNBIN(AC)}$ = 0 V; $V_{(LEVEL)DC}$ = 3.5 V	3	3.5	4	V
f_{AMHOLD}	trigger sensitivity	t_{pulse} = 10 µs; repetition rate = 50 Hz; V_{pulse} = 1.7 V (AMNBIN); V_{LEVEL} = 4 V	45	50	55	Hz
I_{offset}	gate input offset current at pins during suppression pulse duration	during AF suppression time	–50	0	+50	nA
Muting average detector (TMUTE); see Fig.12						
$V_{i(LEVEL)}$	input voltage on LEVEL		0.5	–	4	V
G_v	voltage gain LEVEL to TMUTE		–	0	–	dB
ΔV_{TMUTE}	offset between TMUTE and LEVEL		–	1.5	–	V
$\Delta V_{TMUTE/K}$	temperature dependence at TMUTE		–	3.3	–	mV/K
MUTING AVERAGE DETECTOR TIME CONSTANT						
$I_{ch(TMUTE)}$	TMUTE charge current		–	–0.2	–	µA
$I_{dch(TMUTE)}$	TMUTE discharge current		–	0.2	–	µA
V_O	DC output voltage		2	–	5	V
TEST CONDITION						
$I_{ch(test)}$	capacitor charge current	data byte 6, bit 7 = 1	–	–12	–	µA
$I_{dch(test)}$	capacitor discharge current	data byte 6, bit 7 = 1	–	12	–	µA
AM wideband average detector (TWBAM1); see Fig.6						
V_{TWBAM1}	DC voltage at TWBAM1 with respect to AGND	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VC_{TWBAM1}	DC voltage coefficient	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; note 8; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V_O	DC output voltage		1.5	–	5.5	V
AM WIDEBAND AVERAGE DETECTOR TIME CONSTANT						
$I_{ch(TWBAM1)}$	TWBAM1 charge current		–19.5	–15	–11.5	μA
$I_{dch(TWBAM1)}$	TWBAM1 discharge current		11.5	15	19.5	μA
Ultrasonic noise average detector (TUSN1); see Fig.5						
V_{TUSN1}	DC voltage at TUSN1 with respect to AGND	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
VC_{TUSN1}	DC voltage coefficient	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; note 9; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.44	0.52	0.62	
V_O	DC output voltage		1.5	–	5.5	V
ULTRASONIC NOISE AVERAGE DETECTOR TIME CONSTANT						
$I_{ch(TUSN1)}$	TUSN1 charge current		–19.5	–15	–11.5	μA
$I_{dch(TUSN1)}$	TUSN1 discharge current		11.5	15	19.5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Peak detector for stereo noise control (TSNC)						
DEPENDENCY ON LEVEL VOLTAGE; see Fig.12						
V_{LEVEL}	input voltage		0.5	–	4.75	V
G	gain LEVEL to TSNC		–	0	–	dB
V_{TSNC}	DC voltage at TSNC referred to DC level voltage at LEVEL	without MPXRDS and LEVEL (AC) input				
		$V_{(LEVEL)DC}$ = 0.5 V	1.75	2.00	2.25	V
		$V_{(LEVEL)DC}$ = 3.5 V	4.50	5.00	5.50	V
$\Delta V_{TSNC/K}$	temperature dependence at TSNC		–	3.3	–	mV/K
DEPENDENCY ON ULTRASONIC NOISE; see Fig.5						
V_{TSNC}	DC voltage at TSNC w.r.t. AGND	$V_{MPXRDS(AC)}$ = 350 mV; $V_{(LEVEL)DC}$ = 3.5 V; f_i = 80 kHz; write mode; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
VC_{TSNC}	DC voltage coefficient	$V_{MPXRDS(AC)}$ = 350 mV; $V_{(LEVEL)DC}$ = 3.5 V; f_i = 80 kHz; write mode; note 10; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.40	0.52	0.62	
V_O	DC output voltage		2	–	5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEPENDENCY ON AM WIDEBAND NOISE; see Fig.6						
V_{TSNC}	DC voltage at TSNC	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
VC_{TSNC}	DC voltage coefficient	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; note 11; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	–
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	–
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	–
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	–
V_O	DC output voltage		1.5	–	5.5	V
DETECTOR TIME CONSTANT						
$I_{ch(TSNC)}$	TSNC charge current		–	–2.5	–	μA
$I_{dch(TSNC)}$	TSNC discharge current		–	65	–	μA
TEST CONDITION						
$I_{ch(test)}$	charge current for testing	data byte 6, bit 7 = 1; $V_{(LEVEL)DC}$ = 2 V; $V_{(TSNC)DC}$ = 2.8 V	–	–1.5	–	mA
$I_{dch(test)}$	discharge current for testing	data byte 6, bit 7 = 1; $V_{(LEVEL)DC}$ = 2 V; $V_{(TSNC)DC}$ = 4.2 V	–	200	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ultrasonic noise peak detector (TUSN2); see Fig.5						
V_{TUSN2}	DC voltage at TUSN2 w.r.t. AGND	$V_{MPXRDS(AC)}$ = 350 mV; $V_{(LEVEL)DC}$ = 3.5 V; f_i = 80 kHz; write mode; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
VC_{TUSN2}	DC voltage coefficient	$V_{MPXRDS(AC)}$ = 350 mV; $V_{(LEVEL)DC}$ = 3.5 V; f_i = 80 kHz; write mode; note 12; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.40	0.52	0.62	
V_O	DC output voltage		1.5	–	5.5	V
DETECTOR TIME CONSTANT						
$I_{ch(TUSN2)}$	TUSN2 charge current		–	–1.6	–	μA
$I_{dch(TUSN2)}$	TUSN2 discharge current		–	21	–	μA
AM wideband peak detector (TWBAM2); see Fig.6						
V_{TWBAM2}	DC voltage at TWBAM2 with respect to AGND	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
VC_{TWBAM2}	DC voltage coefficient	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; note 13; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V_O	DC output voltage		2	–	5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DETECTOR TIME CONSTANT						
$I_{ch(TWBAM2)}$	TWBAM2 charge current		–	–1.6	–	μA
$I_{dch(TWBAM2)}$	TWBAM2 discharge current		–	21	–	μA
Soft mute; see Figs 7 and 4						
α_{0dB}	attenuation at LOPO and ROPO	V_{TMUTE} = 3.5 V; V_{TUSN1} = 3.5 V	–0.5	0	+0.5	dB
α_{6dB}	start of muting; AC attenuation at LOPO and ROPO	see Fig.4; write mode; data byte 0, bits 0 and 1; MSL0 = 1; MSL1 = 1				
		MST1 = 0; MST0 = 0; $V_{TMUTE} = 0.42V_{TUSN1}$ without AC	3	6	9	dB
		MST1 = 0; MST0 = 1; $V_{TMUTE} = 0.45V_{TUSN1}$ without AC	3	6	9	dB
		MST1 = 1; MST0 = 0; $V_{TMUTE} = 0.47V_{TUSN1}$ without AC	3	6	9	dB
		MST1 = 1; MST0 = 1; $V_{TMUTE} = 0.49V_{TUSN1}$ without AC	3	6	9	dB
α_{10dB}	AC attenuation for setting of mute slope at LOPO and ROPO	MST1 = 0; MST0 = 0; see Fig.7				
		MSL1 = 0; MSL0 = 0; $V_{TMUTE(DC)} = 0.35V_{TUSN1}$ without AC	7	10	13	dB
		MSL1 = 0; MSL0 = 1; $V_{TMUTE(DC)} = 0.38V_{TUSN1}$ without AC	7	10	13	dB
		MSL1 = 1; MSL0 = 0; $V_{TMUTE(DC)} = 0.39V_{TUSN1}$ without AC	7	10	13	dB
		MSL1 = 1; MSL0 = 1; $V_{TMUTE(DC)} = 0.395V_{TUSN1}$ without AC	7	10	13	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo Noise Control (SNC)						
$\alpha_{cs(start)}$	start of channel separation	aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1111; V_{TSNC} or V_{TUSN1} or $V_{TWBAM1} = 0.63V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
		aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1000; V_{TSNC} or V_{TUSN1} or $V_{TWBAM1} = 0.70V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
		aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 0000; V_{TSNC} or V_{TUSN1} or $V_{TWBAM1} = 0.74V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
$\alpha_{cs(slope)}$	slope of channel separation	aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1000; $V_{TSNC} = 0.72V_{TUSN1}$ without AC; see note 15 and Fig.8; data byte 2, bits 4 and 5:				
		SSL1 = 0; SSL0 = 0	3	5	7	dB
		SSL1 = 0; SSL0 = 1	5	7	9	dB
		SSL1 = 1; SSL0 = 0	11	13	15	dB
		SSL1 = 1; SSL0 = 1 (not defined)				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High Cut Control (HCC)						
$\alpha_{HCC(start)}$	AC attenuation for start of HCC	AF = 10 kHz; V_{MPXIN} = 200 mV; HSL1 = 1; HSL0 = 0; data byte 0, SMUT = 0 and MONO = 1; write mode; see note 16 and Fig.10; data byte 3, bits 2 and 3:				
		HST1 = 1; HST0 = 1; $V_{(LEVEL)DC}$ = 1.00 V	1.5	3	4.5	dB
		HST1 = 1; HST0 = 0; $V_{(LEVEL)DC}$ = 1.25 V	1.5	3	4.5	dB
		HST1 = 0; HST0 = 1; $V_{(LEVEL)DC}$ = 1.50 V	1.5	3	4.5	dB
		HST1 = 0; HST0 = 0; $V_{(LEVEL)DC}$ = 1.75 V	1.5	3	4.5	dB
$\alpha_{HCC(slope)}$	AC attenuation for slope of HCC	AF = 10 kHz; V_{MPXIN} = 200 mV; C_{FMLBUF}, C_{FMRBUF} = 2.7 nF; HST1 = 1; HST0 = 1; data byte 0, SMUT = 0 and MONO = 1; see note 16 and Fig.11; data byte 3, bits 0 and 1:				
		HSL1 = 1; HSL0 = 1	5.5	7.5	9.5	dB
		HSL1 = 1; HSL0 = 0	4	6	8	dB
		HSL1 = 0; HSL0 = 1	2	4	6	dB
		HSL1 = 0; HSL0 = 0	1	3	5	dB
$\alpha_{HCC(max)}$	maximum HCC attenuation	AF = 10 kHz; V_{TMUTE} = 2 V; data byte 0, SMUT = 0 and MONO = 1; data byte 3, bit 1 = bit 0 = 1				
		C_{FMLBUF}, C_{FMRBUF} = 2.7 nF; data byte 3, bit 4 = 1	8	10	14.5	dB
		C_{FMLBUF}, C_{FMRBUF} = 680 pF; data byte 3, bit 4 = 0	8	10	14.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converters						
LEVEL ANALOG-TO-DIGITAL CONVERTER (6-BIT)						
$V_{LEVEL(min)}$	lower limit of conversion range		–	740	–	mV
$V_{LEVEL(max)}$	upper limit of conversion range		–	3.4	–	V
ΔV_{LEVEL}	bit resolution		–	42.5	–	mV
ULTRASONIC NOISE ANALOG-TO-DIGITAL CONVERTER (3-BIT)						
$V_{TUSN(min)}$	lower limit of conversion range		–	2.1	–	V
$V_{TUSN(max)}$	upper limit of conversion range		–	4	–	V
ΔV_{TUSN}	bit resolution		–	320	–	mV
AM WIDEBAND NOISE ANALOG-TO-DIGITAL CONVERTER (3-BIT)						
$V_{TWBAM(min)}$	lower limit of conversion range		–	2.1	–	V
$V_{TWBAM(max)}$	upper limit of conversion range		–	4	–	V
ΔV_{TWBAM}	bit resolution		–	320	–	mV
Tone/volume control						
$G_{v(max)}$	maximum voltage gain	$R_S \leq 10\ \Omega$; $R_L \geq 10\ M\Omega$	19	20	21	dB
$G_{v(signal)}$	signal voltage gain	T_{amb} = 25 °C	–0.75	0	+0.75	dB
		T_{amb} = –40 to +85 °C	–1	0	+1	dB
$V_{o(rms)}$	output voltage level	THD ≤ 0.5%	–	2000	–	mV
		THD = 1%; G_v = 3 dB	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	V_o = 500 mV; G_v = 20 dB	–	50	–	mV
f_{ro}	roll-off frequency	high frequency (–1 dB)	20000	–	–	Hz
		input A; $C_{KIL} = C_{KIR}$ = 100 nF; $C_{KVL} = C_{KVR}$ = 220 nF				
		low frequency (–1 dB)	–	35	45	Hz
		low frequency (–3 dB)	–	20	25	Hz
		input C; $C_{KICL} = C_{KICR}$ = 1 μF; $C_{KVL} = C_{KVR}$ = 220 nF				
		low frequency (–1 dB)	–	18	23	Hz
		low frequency (–3 dB)	–	10	13	Hz
α_{cs}	channel separation	V_i = 1 V; frequency range 250 Hz to 20 kHz	74	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	valid for input channel A, B or C; same for all 4 outputs refer to inputs				
		$V_{i(rms)}$ = 1 V; f = 1 kHz; volume 1 attenuator: –6 dB; equalizer bands flat	–	0.05	0.1	%
		$V_{i(rms)}$ = 2 V; f = 1 kHz; V_{CC} = 8.3 V; volume 1 attenuator: –13 dB; equalizer bands flat	–	0.1	0.3	%
		$V_{i(rms)}$ = 2 V; f = 1 kHz; V_{CC} = 8.5 V; volume 1 attenuator: 0 dB; equalizer bands flat	–	0.05	0.1	%
		$V_{i(rms)}$ = 1 V; f = 1 kHz; V_{CC} = 8.3 V; volume 1 attenuator: 0 dB; equalizer bands flat	–	0.01	0.1	%
		$V_{i(rms)}$ = 2.3 V; f = 1 kHz; V_{CC} = 9 V; volume 1 attenuator: –13 dB; equalizer bands flat	–	0.13	0.3	%
		$V_{i(rms)}$ = 1 V; f = 20 Hz to 20 kHz; volume 1 attenuator: –6 dB; equalizer bands flat	–	0.05	0.2	%
		$V_{i(rms)}$ = 2 V; f = 20 Hz to 20 kHz; V_{CC} = 8.3 V; volume 1 attenuator: –13 dB; equalizer bands flat	–	0.1	0.3	%
		$V_{i(rms)}$ = 2.3 V; f = 20 Hz to 20 kHz; V_{CC} = 9 V; volume 1 attenuator: –13 dB; equalizer bands flat	–	0.1	0.3	%
		$V_{i(rms)}$ = 0.5 V; f = 25 Hz; volume 1 attenuator: 0 dB; equalizer bass boost: +8 dB	–	0.1	0.2	%
		$V_{i(rms)}$ = 0.5 V; f = 4 kHz; volume 1 attenuator: 0 dB; equalizer treble boost: +8 dB	–	0.15	0.3	%
	chime adder total harmonic distortion	$V_{i(rms)}$ = 0.5 V; f = 1 kHz; V_{CC} = 8.5 V; no input signal at input A	–	0.04	0.1	%
PSRR	power supply ripple rejection C_{VHS} = 47 µF; C_{SCAP} = 22 µF	stereo source: A, B, C or mono; V_{CC} = 8.5 V + 0.2 V (RMS)				
		f = 20 to 100 Hz	35	46	–	dB
		f = 1 to 20 kHz	50	65	–	dB
		f = 1 kHz	50	75	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{noise(rms)}$	noise voltage CCIR-ARM weighted (RMS value) without input signal and shorted AF inputs	volume 1 attenuator: +20 dB	–	65	100	µV
		volume 1 attenuator: +20 dB; symmetrical input	–	100	140	µV
		volume 1 attenuator: 0 dB	–	10	14	µV
		volume 1 attenuator: 0 dB; symmetrical input	–	12.5	18	µV
		volume 1 attenuator: 0 dB; bass and treble boost: 6 dB	–	16	25	µV
		volume 1 attenuator: 0 dB; bass and treble boost: 6 dB; symmetrical input	–	22	32	µV
		volume 1 attenuator: –9 dB	–	9	14	µV
		minimum volume; volume 1 attenuator: –18 dB; loudness: –20 dB; volume 2 attenuator: –22 dB	–	5	8	µV
		mute selected: data byte 8, AMUT = 1	–	3.5	5	µV
		volume setting: –20 dB; volume 1 attenuator: –10 dB; loudness: –10 dB; A-weighted	–	5.7	8	µV
CMRR	input common mode rejection	C channel input; $V_{i(rms)}$ = 1 V; f = 20 Hz to 20 kHz on CLIP, CRIP and CCOM	48	53	–	dB
		C channel input; $V_{i(rms)}$ = 1 V; f = 1 kHz on CLIP, CRIP and CCOM	48	53	–	dB
		C channel input; $V_{i(rms)}$ = 1 V; f = 20 Hz to 20 kHz on CLIP, CRIP and CCOM; volume attenuator: –15 dB	63	68	–	dB
$CMRR_{mono}$	mono input common mode rejection	source = mono input	40	45	–	dB
α_{ct}	crosstalk between bus inputs and signal outputs	clock frequency = 50 kHz; repetition burst rate = 300 Hz; total initialization; note 17	–	110	–	dB
t_{ABC}	Audio Blend Control (ABC) step time	C_{ASICAP} = 22 nF; write mode; data byte 4, bits 6 and 7:				
		ASI1 = 0; ASI0 = 0	–	0.83	–	ms
		ASI1 = 0; ASI0 = 1	–	3.33	–	ms
		ASI1 = 1; ASI0 = 0	–	8.33	–	ms
		ASI1 = 1; ASI0 = 1	–	20	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source selector						
$Z_{i(stereo)}$	stereo input impedance (A and B input)		80	100	120	kΩ
$Z_{i(sym)}$	symmetrical input impedance (C and mono input)		24	30	36	kΩ
$Z_{i(CHIME)}$	CHIME input impedance (chime input)		80	100	120	kΩ
Z_o	output impedance at ROPO and LOPO		–	80	100	Ω
R_L	output load resistance at ROPO and LOPO		10	–	–	kΩ
C_L	output load capacitance at ROPO and LOPO		0	–	2500	pF
G_v	source selector voltage gain		–0.2	0	+0.2	dB
α_S	input isolation of one selected source to any other input	f = 1 kHz	90	105	–	dB
		f = 12.5 kHz	80	95	–	dB
		f = 20 Hz to 20 kHz	75	90	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	2.0	2.15	–	V
		THD < 0.5%; V_{CC} = 7.8 V	1.8	1.9	–	V
Loudness control						
Z_i	input impedance at ROPI and LOPI		80	100	120	kΩ
$G_{loudness}$	loudness control, maximum gain	f = 1 kHz; loudness on/off	–0.2	0	+0.2	dB
	loudness control, minimum gain	f = 1 kHz; loudness on/off	–18.5	–20	–21.5	dB
$\Delta G_{loudness}$	gain, loudness on referred to loudness off	f = 1 kHz; $G_{loudness}$ = –20 dB	–1.5	0	+1.5	dB
G_{step}	step resolution gain	f = 1 kHz	–	1	–	dB
	step error between any adjoining step	f = 1 kHz	–	–	0.5	dB
L_{Bmax}	maximum loudness boost; without influence of coupling capacitors	compared to 1 kHz; loudness on				
		f = 30 Hz	17	18.5	19	dB
		f = 10 kHz	4	5	6	dB
		compared to 1 kHz; loudness off				
		f = 30 Hz	–1	–	0	dB
		f = 10 kHz	–1	–	0	dB
		f_{ref} = 30 Hz; f_{meas} = 300 Hz; bass boost only	12.5	14	15.5	dB
		f_{ref} = 30 Hz; f_{meas} = 300 Hz; bass and treble boost	12	13.5	15	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume 1 control						
G_v	voltage gain		–36	–	+20	dB
G_{step}	step resolution gain		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator gain set error	G_v = +20 to –36 dB	–1	0	+1	dB
ΔG_{track}	gain tracking error	G_v = +20 to –36 dB	–	0	1	dB
Treble control						
G_{treble}	treble gain control, maximum boost	f = 10 kHz; $V_{i(rms)}$ = 200 mV	13	14	15	dB
	maximum attenuation	f = 10 kHz	13	14	15	dB
G_{step}	step resolution gain	f = 10 kHz	–	2	–	dB
	step error between any adjoining step	f = 10 kHz	–	–	0.5	dB
Bass control						
G_{bass}	bass gain control, maximum boost	external T-filter; f = 60 Hz; BSYB = 1; $V_{i(rms)}$ = 200 mV	16	18	20	dB
	maximum attenuation	external T-filter; f = 60 Hz; BSYC = 0	16	18	20	dB
		external T-filter; f = 60 Hz; BSYC = 1	13	14.4	15.5	dB
G_{step}	step resolution gain	f = 60 Hz; boost; BSYB = 1	–	2	–	dB
		f = 60 Hz; cut; BSYC = 0	–	2	–	dB
		f = 60 Hz; cut; BSYC = 1	1.2	1.6	1.9	dB
	step error between any adjoining step	f = 60 Hz	–	–	0.5	dB
f_c	centre frequency	$C_{bass} = 2 \times 220$ nF; R_{bass} = 3.3 kΩ	50	60	70	Hz
Q_e	equalizer quality factor	$V_{i(rms)}$ = 200 mV; boost = 12 dB	0.8	0.9	1.1	
EQ_{bow}	equalizer bowing	$V_{i(rms)}$ = 200 mV; bass and treble boost = 12 dB; reference flat frequency response	–	2.1	3.3	dB
Volume 2 control						
G_v	voltage gain		–68	–	0	dB
G_{step}	step resolution	G_v = 0 to –56 dB	–	1	–	dB
	step error between any adjoining step	G_v = 0 to –56 dB	–	–	0.5	dB
	additional steps		–	–58.5	–	dB
			–	–62	–	dB
			–	–68	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{mute}	mute attenuation		100	110	–	dB
		f = 20 Hz to 20 kHz	75	85	–	dB
ΔG_a	attenuator gain set error	G_v = 0 to –32 dB	–1	–	+1	dB
		G_v = –32 to –68 dB	–2	–	+2	dB
ΔG_{track}	gain tracking error	G_v = 0 to –56 dB	–	0	1	dB
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
$C_{o(L)}$	output load capacitance		0	–	10	nF
$R_{o(L)}$	DC load resistance at output to ground		4.7	–	–	kΩ
Chime adder						
$G_{v(CHIME)}$	chime adder voltage gain	$V_{i(rms)}$ = 1 V; chime input; chime adder on	–21	–20	–19	dB
$V_{i(CHIME)(rms)}$	maximum chime input voltage (sine wave)	main output voltage $V_{o(rms)}$ < 1.5 V; chime input; chime adder on	2.0	–	–	V
k	factor for $V_{i(CHIME)}$ to avoid internal clipping	$k \times V_{i(CHIME)(p-p)} < 5.7\ V - V_{o(p-p)}$	0.22	0.25	0.28	
Digital part (SDA, SDAQ, SCL, SCLQ, FMHOLD, AFSAMPLE); note 18						
V_{IH}	HIGH-level input voltage		3	5	9.7	V
V_{IL}	LOW-level input voltage		–0.3	+0.3	+1.5	V
I_{IH}	HIGH-level input current	V_{CC} = 0 to 9.5 V	–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
V_{OL}	LOW-level output voltage SDA	I_L = 3 mA	–	–	0.4	V
Digital part (SDAQ and SCLQ); note 18						
$I_{o(sink)}$	output sink current		–	–	600	µA
R_{pu}	pull-up resistance		–	–	22	kΩ
C_L	load capacitance		–	–	20	pF
Digital part (ADR); note 18						
V_{IH}	HIGH-level input voltage		3	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–	–	150	µA
I_{IL}	LOW-level input current		–80	–	–	µA

Notes to the characteristics

1. Intermodulation suppression; Beat Frequency Components (BFC):

   a) $IM2 = \frac{V_{o(signal)}(\text{at 1 kHz})}{V_{o(spurious)}(\text{at 1 kHz})}$; $f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$

   b) $IM3 = \frac{V_{o(signal)}(\text{at 1 kHz})}{V_{o(spurious)}(\text{at 1 kHz})}$; $f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$

   c) measured with 91% mono signal; f_{mod} = 10 kHz or 13 kHz; 9% pilot signal.

2. RDS suppression:

   $$\alpha_{57(RDS)} = \frac{V_{o(signal)}(\text{at 1 kHz})}{V_{o(spurious)}(\text{at 1 kHz} \pm 23\ \text{Hz})}$$

   a) measured with 91% stereo signal; f_{mod} = 1 kHz; 9% pilot signal; 5% RDS subcarrier (f_s = 57 kHz; f_{mod} = 23 Hz; AM m = 0.6).

3. Subsidiary Communication Authorization (SCA):

   $$\alpha_{67} = \frac{V_{o(signal)}(\text{at 1 kHz})}{V_{o(spurious)}(\text{at 9 kHz})}\ ;\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

   a) measured with 81% mono signal; f_{mod} = 1 kHz; 9% pilot signal; 10% SCA subcarrier (f_s = 67 kHz, unmodulated).

4. Adjacent Channel Interference (ACI):

   $$\alpha_{114} = \frac{V_{o(signal)}(\text{at 1 kHz})}{V_{o(spurious)}(\text{at 4 kHz})}\ ;\ f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

   a) $\alpha_{190} = \frac{V_{o(signal)}(\text{at 1 kHz})}{V_{o(spurious)}(\text{at 4 kHz})}$; $f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$

   b) measured with 90% mono signal; f_{mod} = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 kHz or 186 kHz, unmodulated).

5. AM stereo audio buffer gain:

   $$G = 20\log\frac{V_{LOPO}}{V_{DEEML}}\ ;\ G = 20\log\frac{V_{ROPO}}{V_{DEEMR}}$$

6. Input resistance for AM stereo left and right:

   $$R_{i(DEEML,DEEMR)} = \frac{\Delta V_{DEEML,DEEMR}}{\Delta I_{i(DEEML,DEEMR)}}$$

7. Attenuation of blanking gate:

   $$\alpha_{AMGATE} = 20\log\frac{V_{AMPCAP}\ \text{at gate open}}{V_{AMPCAP}\ \text{at gate close}}$$

8. TWBAM1 DC voltage coefficient:

   $$VC_{TWBAM1} = \frac{V_{TWBAM1}\ \text{with AC voltage at LEVEL}}{V_{TWBAM1}\ \text{without AC voltage}}$$

9. TUSN1 DC voltage coefficient:

   $$VC_{TUSN1} = \frac{V_{TUSN1}\ \text{with AC voltage at MPXRDS}}{V_{TUSN1}\ \text{without AC voltage}}$$

10. TSNC DC voltage coefficient:

$$VC_{TSNC} = \frac{V_{TSNC}\text{ with AC voltage at MPXRDS}}{V_{TSNC}\text{ without AC voltage}}$$

11. TSNC DC voltage coefficient:

$$VC_{TSNC} = \frac{V_{TSNC}\text{ with AC voltage at LEVEL}}{V_{TSNC}\text{ without AC voltage}}$$

12. TUSN2 DC voltage coefficient:

$$VC_{TUSN2} = \frac{V_{TUSN2}\text{ with AC voltage at MPXRDS}}{V_{TUSN2}\text{ without AC voltage}}$$

13. TWBAM2 DC voltage coefficient:

$$VC_{TWBAM2} = \frac{V_{TWBAM2}\text{ with AC voltage at LEVEL}}{V_{TWBAM2}\text{ without AC voltage}}$$

14. Start of channel separation:

$$\alpha_{cs(start)} = \left|20\log\frac{V_{LOPO(AC)}}{V_{ROPO(AC)}}\right|$$

15. Slope of channel separation:

$$\alpha_{cs(slope)} = \left|20\log\frac{V_{LOPO(AC)}}{V_{ROPO(AC)}}\right|$$

16. AC attenuation for start and slope of HCC:

$$\alpha_{HCC(10\ kHz)} = 20\log\frac{V_{LOPO,ROPO}}{V_{LOPO,ROPO}\text{ without High Cut active}}$$

17. Crosstalk between bus inputs and signal outputs:

$$\alpha_{ct} = 20\log\frac{V_{bus(p\text{-}p)}}{V_{o(rms)}}$$

18. The characteristics are in accordance with the I^2C-bus specification. This specification, *“The I^2C-bus and how to use it”*, can be ordered using the code 9398 393 40011.

11 I^2C-BUS PROTOCOL

Table 1 Write mode

S(1)	CHIP ADDRESS (write)	A(2)	SUBADDRESS	A(2)	DATA BYTE(S)	A(2)	P(3)

Table 2 Read mode

S(1)	CHIP ADDRESS (read)	A(2)	DATA BYTE 1	A(2)	DATA BYTE 2	A(2)	P(3)

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 3 Chip address byte

CHIP ADDRESS							READ/WRITE
0	0	1	1	0	0	0/1(1)	R/$\overline{W}$(2)

Notes

1. Defined by address pin ADR.
2. 0 = receiver and 1 = transmitter.

11.1 Read mode: 1st data byte

Table 4 Format of 1st data byte

7	6	5	4	3	2	1	0
STIN	RDSU	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0

Table 5 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	STIN	**Stereo indicator.** This bit indicates if a pilot signal has been detected. If STIN = 0, then no pilot signal has been detected. If STIN = 1, then a pilot signal has been detected.
6	RDSU	**Measure mode.** This bit selects the measure mode for the RDS flags. If RDSU = 0, then continuous mode is selected. If RDSU = 1, then RDS update mode is selected.
5 to 0	LVL[5:0]	**ADC voltage level.** These 6 bits determine the ADC voltage level; see Table 6.

Table 6 Level setting ADC

V_{LEVEL} (V)	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0
3.600	1	1	1	1	1	1
3.553	1	1	1	1	1	0
3.506	1	1	1	1	0	1
3.460	1	1	1	1	0	0
3.413	1	1	1	0	1	1
3.366	1	1	1	0	1	0
3.319	1	1	1	0	0	1
3.272	1	1	1	0	0	0
3.225	1	1	0	1	1	1
3.179	1	1	0	1	1	0
3.132	1	1	0	1	0	1
3.085	1	1	0	1	0	0
3.038	1	1	0	0	1	1
2.991	1	1	0	0	1	0
2.944	1	1	0	0	0	1
2.898	1	1	0	0	0	0
2.851	1	0	1	1	1	1
2.804	1	0	1	1	1	0
2.757	1	0	1	1	0	1
2.710	1	0	1	1	0	0
2.663	1	0	1	0	1	1
2.617	1	0	1	0	1	0
2.570	1	0	1	0	0	1
2.523	1	0	1	0	0	0
2.476	1	0	0	1	1	1
2.429	1	0	0	1	1	0
2.383	1	0	0	1	0	1
2.336	1	0	0	1	0	0
2.289	1	0	0	0	1	1
2.242	1	0	0	0	1	0
2.195	1	0	0	0	0	1
2.148	1	0	0	0	0	0
2.102	0	1	1	1	1	1
2.055	0	1	1	1	1	0
2.008	0	1	1	1	0	1
1.961	0	1	1	1	0	0
1.914	0	1	1	0	1	1
1.867	0	1	1	0	1	0
1.821	0	1	1	0	0	1
1.774	0	1	1	0	0	0

V_{LEVEL} (V)	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0
1.727	0	1	0	1	1	1
1.680	0	1	0	1	1	0
1.633	0	1	0	1	0	1
1.587	0	1	0	1	0	0
1.540	0	1	0	0	1	1
1.493	0	1	0	0	1	0
1.446	0	1	0	0	0	1
1.399	0	1	0	0	0	0
1.352	0	0	1	1	1	1
1.306	0	0	1	1	1	0
1.259	0	0	1	1	0	1
1.212	0	0	1	1	0	0
1.165	0	0	1	0	1	1
1.118	0	0	1	0	1	0
1.071	0	0	1	0	0	1
1.025	0	0	1	0	0	0
0.978	0	0	0	1	1	1
0.931	0	0	0	1	1	0
0.884	0	0	0	1	0	1
0.837	0	0	0	1	0	0
0.790	0	0	0	0	1	1
0.744	0	0	0	0	1	0
0.697	0	0	0	0	0	1
0.650	0	0	0	0	0	0

11.2 Read mode: 2nd data byte

Table 7 Format of 2nd data byte

7	6	5	4	3	2	1	0
–	USN2	USN1	USN0	–	WBA2	WBA1	WBA0

Table 8 Description of 2nd data byte

BIT	SYMBOL	DESCRIPTION
7	–	This bit is not used and must be set to logic 1.
6	USN2	**Ultrasonic noise ADC.** These 3 bits select the voltage level for the ultrasonic noise ADC; see Table 9.
5	USN1	
4	USN0	
3	–	This bit is not used and must be set to logic 1.
2	WBA2	**AM wideband noise ADC.** These 3 bits select the voltage level for the AM wideband ADC; see Table 10.
1	WBA1	
0	WBA0	

Table 9 Ultrasonic noise ADC

V_{TUSN2} (V)	USN2	USN1	USN0
4.500	1	1	1
4.157	1	1	0
3.814	1	0	1
3.471	1	0	0
3.129	0	1	1
2.786	0	1	0
2.443	0	0	1
2.100	0	0	0

Table 10 AM wideband noise ADC

V_{TWBAM2} (V)	WBA2	WBA1	WBA0
4.500	1	1	1
4.157	1	1	0
3.814	1	0	1
3.471	1	0	0
3.129	0	1	1
2.786	0	1	0
2.443	0	0	1
2.100	0	0	0

11.3 Subaddress byte for write

Table 11 Format for subaddress byte

7	6	5	4	3	2	1	0
AIOF	BOUT	–	–	SAD3	SAD2	SAD1	SAD0

Table 12 Description of subaddress byte

BIT	SYMBOL	DESCRIPTION
7	AIOF	**Auto-increment control.** This bit controls the auto-increment function. If AIOF = 0, then the auto-increment is on. If AIOF = 1, then auto-increment is off.
6	BOUT	**I^2C-bus output control.** This bit enables/disables the I^2C-bus output SDAQ and SCLQ to the TEA6840H. If BOUT = 0, then the I^2C-bus output is disabled. If BOUT = 1, then the I^2C-bus output is enabled.
5	–	These 2 bits are not used; both must be set to logic 0.
4	–	
3	SAD3	**Data byte select.** These 4 bits select which data byte is to be addressed; see Table 13.
2	SAD2	
1	SAD1	
0	SAD0	

Table 13 Selection of data byte

ADDRESSED DATA BYTE	MNEMONIC	SAD3	SAD2	SAD1	SAD0
Alignment 0	ALGN0	0	0	0	0
Alignment 1	ALGN1	0	0	0	1
Alignment 2	ALGN2	0	0	1	0
Alignment 3	ALGN3	0	0	1	1
ASI time source selector	SSEL	0	1	0	0
Bass control	BASS	0	1	0	1
Treble control	TRBL	0	1	1	0
Loudness control	LOUD	0	1	1	1
Volume 1	VOLU1	1	0	0	0
Volume 2, left front	VOL2_LF	1	0	0	1
Volume 2, right front	VOL2_RF	1	0	1	0
Volume 2, left rear	VOL2_LR	1	0	1	1
Volume 2, right rear	VOL2_RR	1	1	0	0
Not used(1)	–	1	1	0	1
Not used(1)	–	1	1	1	0
Not used(1)	–	1	1	1	1

Note

1. Not tested; function not guaranteed.

11.4 Write mode: subaddress 0H

Table 14 Format of data byte Alignment 0 (ALGN0)

7	6	5	4	3	2	1	0
AMON	AMST	SEAR	SMUT	MMUT	MONO	MST1	MST0

Table 15 Description of ALGN0 bits

BIT	SYMBOL	DESCRIPTION
7	AMON	**AM/FM mode selection.** These 2 bits select the AM/FM mode and source; see Table 16.
6	AMST	
5	SEAR	**Search mode selection.** If SEAR = 0, then mute and SNC detectors normal. If SEAR = 1, then mute and SNC detectors fast.
4	SMUT	**Soft mute enable.** If SMUT = 0, then soft mute off. If SMUT = 1, then soft mute enabled.
3	MMUT	**Muting of MPX output.** If MMUT = 0, then MPX output not muted. If MMUT = 1, then MPX output muted.
2	MONO	**Stereo decoder mode selection.** If MONO = 0, then Stereo mode selected. If MONO = 1, then Mono mode selected.
1	MST1	**Start of muting.** These 2 bits determine the value of V_{TMUTE}; see Table 17 and Fig.4.
0	MST0	

Table 16 Setting of AM/FM mode

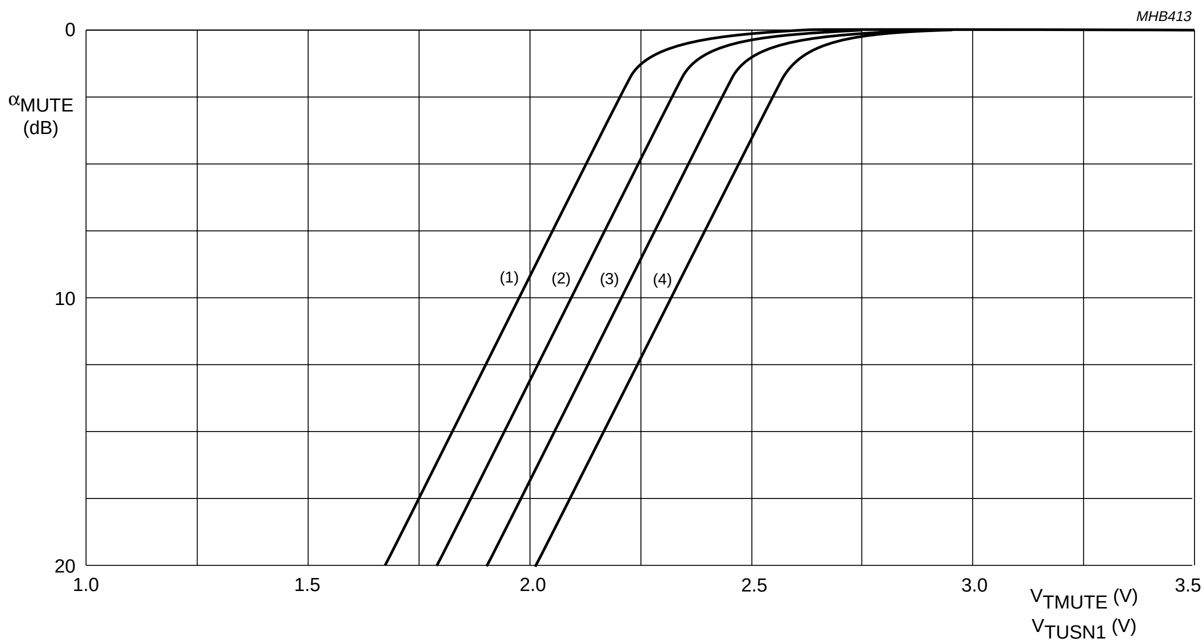
SELECTED MODE	AMON	AMST
AM stereo mode, note 1	1	1
AM mode, active input AMHIN	1	0
Not allowed	0	1
FM mode, active input MPXIN	0	0

Note

1. MPX input (MPXIN) and AM input (AMHIN) muted, stereo decoder in mono mode and de-emphasis terminals (DEEML and DEEMR) are audio signal inputs.

Table 17 Setting of start of muting (α_{MUTE} = 6 dB)

V_{TMUTE} (V)	MST1	MST0
2.45	1	1
2.30	1	0
2.15	0	1
2.00	0	0



Data byte ALGN2: MSL0 = 1, MSL1 = 1

Data byte ALGN0

CURVE	MST1	MST0
(1)	0	0
(2)	0	1
(3)	1	0
(4)	1	1

Fig.4 Soft mute attenuation as a function of V_{TMUTE} and V_{TUSN1} input voltage (fixed slope).

11.5 Write mode: subaddress 1H

Table 18 Format of data byte Alignment 1 (ALGN1)

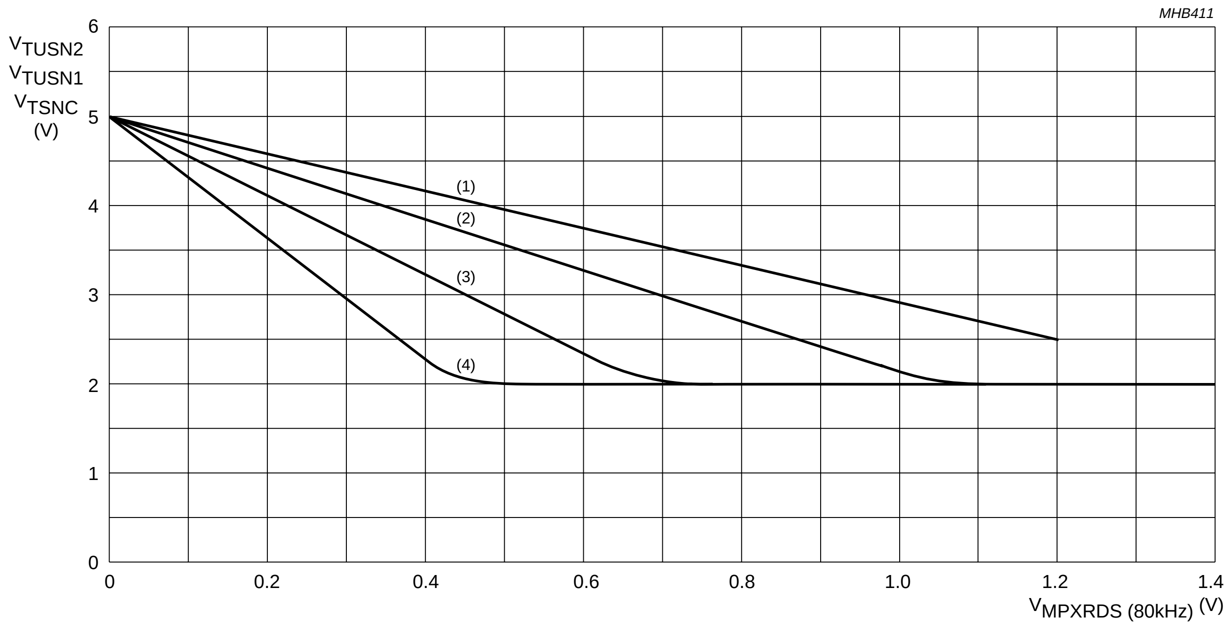
7	6	5	4	3	2	1	0
USS1	USS0	AWS1	AWS0	CHS3	CHS2	CHS1	CHS0

Table 19 Description of ALGN1 bits

BIT	SYMBOL	DESCRIPTION
7	USS1	**Ultrasonic noise sensitivity.** These 2 bits determine the ultrasonic noise sensitivity levels; see Table 20 and Fig.5.
6	USS0	
5	AWS1	**AM wideband sensitivity.** These 2 bits determine the AM wideband sensitivity levels; see Table 21 and Fig.6.
4	AWS0	
3	CHS3	**Channel separation alignment.** These 4 bits select the channel separation alignment; see Table 22.
2	CHS2	
1	CHS1	
0	CHS0	

Table 20 Setting of ultrasonic noise sensitivity ($V_{MPXRDS(AC)}$ = 350 mV)

SLOPE (V/V)	USS1	USS0
–2.1	1	1
–2.9	1	0
–4.4	0	1
–6.8	0	0



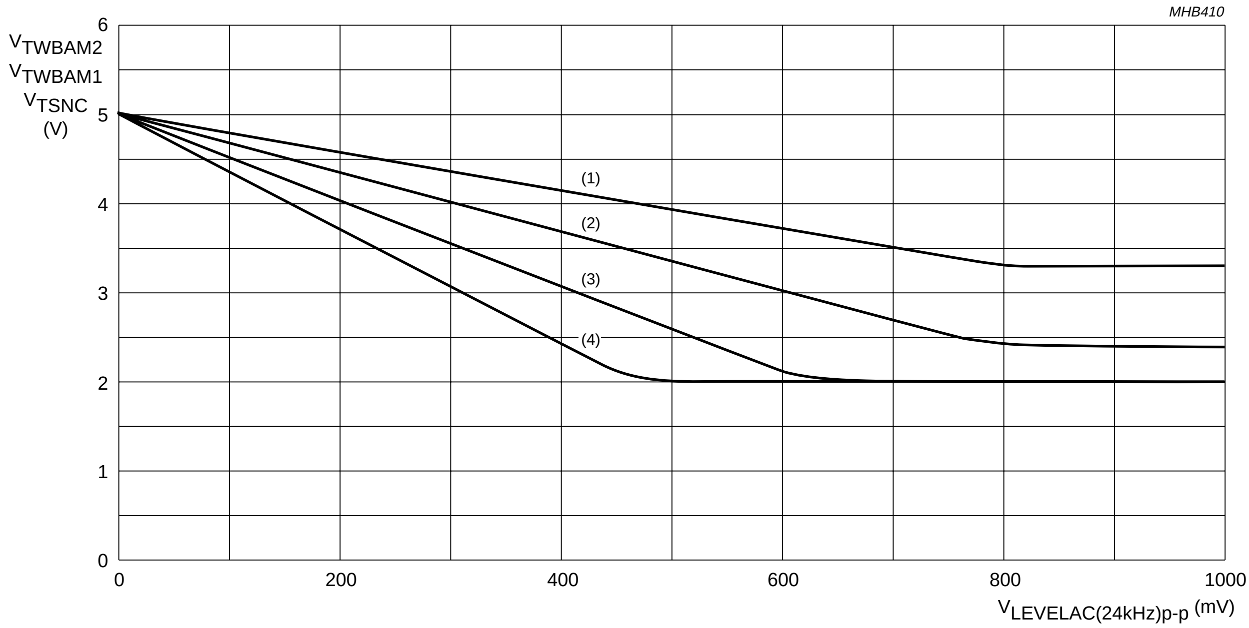
Data byte ALGN1

CURVE	USS1	USS0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

Fig.5 Ultrasonic noise peak and average detector output voltage as a function of MPX signal input, and stereo noise control peak detector output voltage as a function of MPX signal input.

Table 21 Setting of AM wideband sensitivity ($V_{LEVEL(AC)}$ = 400 mV)

SLOPE (V/V)	AWS1	AWS0
–2.2	1	1
–3.3	1	0
–4.9	0	1
–6.5	0	0



Data byte ALGN1

CURVE	AWS1	AWS0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

Fig.6 AM wideband peak and average detector output voltage as a function of level AC signal input, and stereo noise control peak detector output voltage as a function of level AC signal input.

Table 22 Setting of channel separation alignment

CHANNEL SEPARATION ALIGNMENT	CHS3	CHS2	CHS1	CHS0
Not used(1)	1	1	1	1
Not used(1)	1	1	1	0
Not used(1)	1	1	0	1
Not used(1)	1	1	0	0
Not used(1)	1	0	1	1
Not used(1)	1	0	1	0
Setting 9, minimum gain of side signal	1	0	0	1
Setting 8	1	0	0	0
Setting 7	0	1	1	1
Setting 6	0	1	1	0
Setting 5	0	1	0	1
Setting 4	0	1	0	0
Setting 3	0	0	1	1
Setting 2	0	0	1	0
Setting 1	0	0	0	1
Setting 0, maximum gain of side signal	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.6 Write mode: subaddress 2H

Table 23 Format of data byte Alignment 2 (ALGN2)

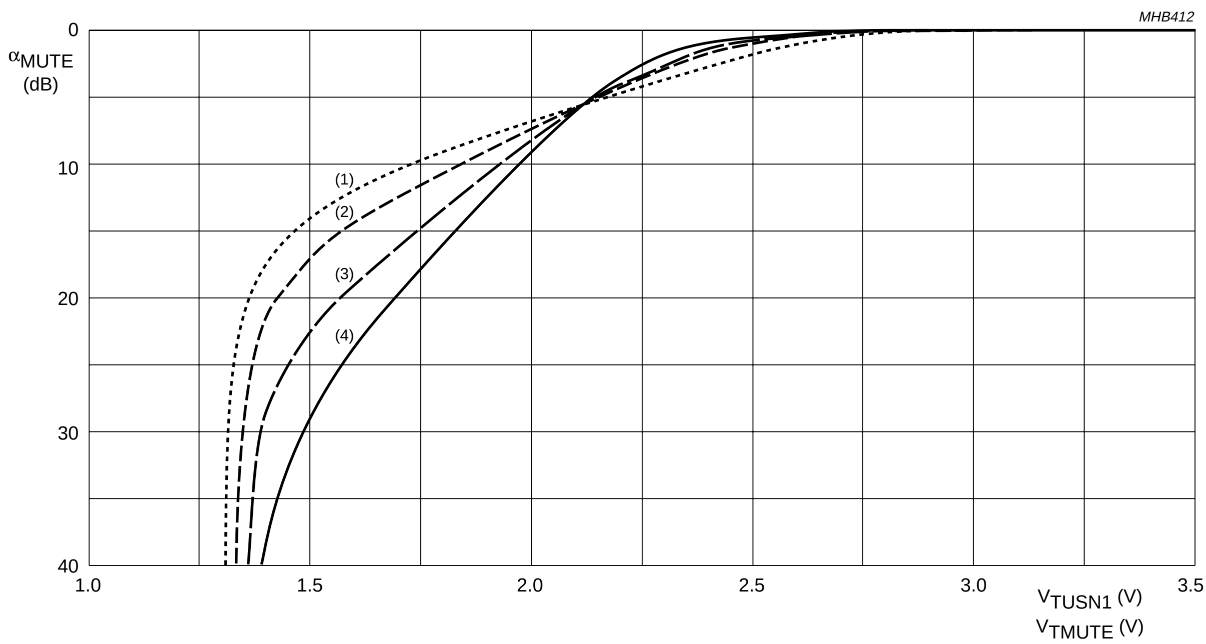
7	6	5	4	3	2	1	0
MSL1	MSL0	SSL1	SSL0	SST3	SST2	SST1	SST0

Table 24 Description of ALGN2 bits

BIT	SYMBOL	DESCRIPTION
7	MSL1	**Soft mute slope alignment.** These 2 bits determine the value of $V_{TMUTE(DC)}$; see Table 25 and Fig.7.
6	MSL0	
5	SSL1	**Stereo noise control slope alignment.** These 2 bits determine the value of α_{cs}; see Table 26 and Fig.8.
4	SSL0	
3	SST3	**Stereo noise control start alignment.** These 4 bits determine the stereo noise control start alignment; see Table 27 and Fig.9.
2	SST2	
1	SST1	
0	SST0	

Table 25 Setting of soft mute slope alignment

$V_{TMUTE(DC)}$	MSL1	MSL0
$0.395V_{TUSN1}$ without AC	1	1
$0.390V_{TUSN1}$ without AC	1	0
$0.380V_{TUSN1}$ without AC	0	1
$0.350V_{TUSN1}$ without AC	0	0



Data byte ALGN0: MST0 = 0, MST1 = 0

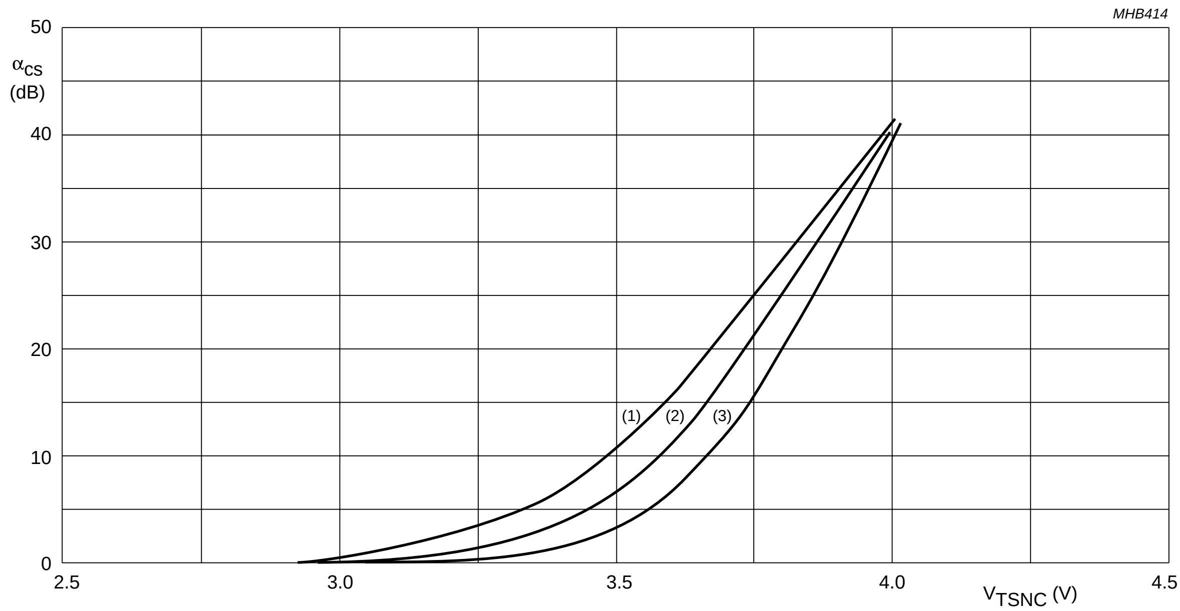
Data byte ALGN2

CURVE	MSL1	MSL0
(1)	0	0
(2)	0	1
(3)	1	0
(4)	1	1

Fig.7 Soft mute attenuation as a function of input voltages V_{TUSN1} and V_{TMUTE} (fixed start).

Table 26 Setting of stereo noise control slope alignment (V_{TSNC} = 0.72V_{TUSN1} without AC)

α_{cs} (dB)	SSL1	SSL0
Not defined	1	1
13	1	0
7	0	1
5	0	0



Data byte ALGN2: SST = 1000

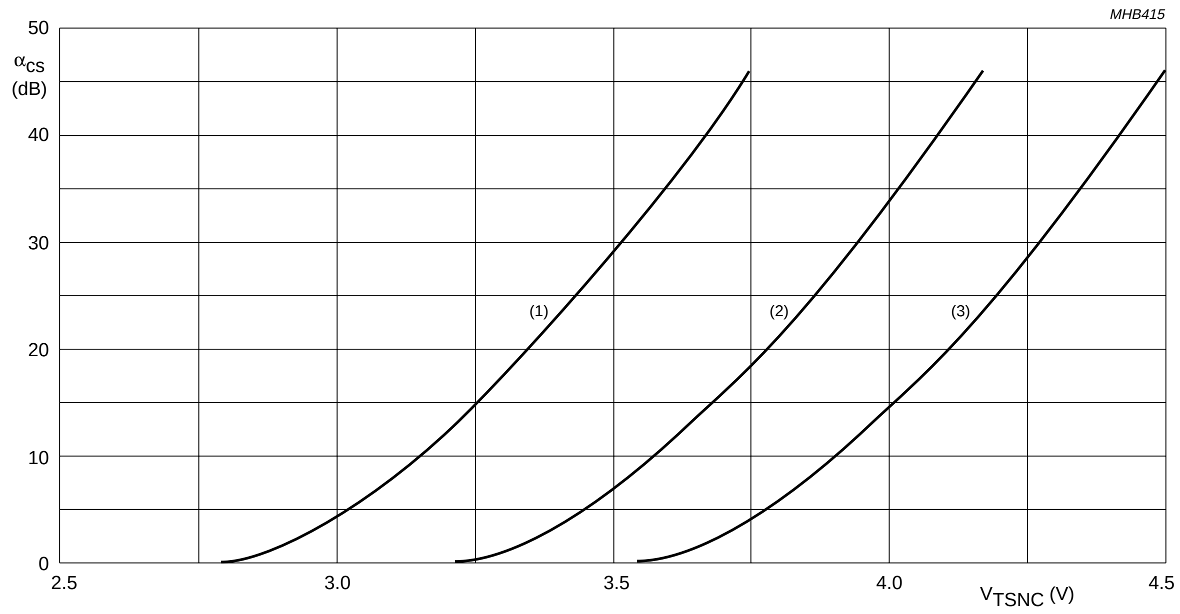
Data byte ALGN2

CURVE	SSL0	SSL1
(1)	0	1
(2)	1	0
(3)	0	0

Fig.8 Channel separation as a function of voltage at pins TSNC, TWBAM1 and TUSN1 (fixed start).

Table 27 Setting of stereo noise control start alignment (α_{cs} = 6 dB)

START ALIGNMENT	SST3	SST2	SST1	SST0
V_{TSNC} = 0.63V_{TUSN1} without AC	1	1	1	1
V_{TSNC}	1	1	1	0
V_{TSNC}	1	1	0	1
V_{TSNC}	1	1	0	0
V_{TSNC}	1	0	1	1
V_{TSNC}	1	0	1	0
V_{TSNC}	1	0	0	1
V_{TSNC} = 0.70V_{TUSN1} without AC	1	0	0	0
V_{TSNC}	0	1	1	1
V_{TSNC}	0	1	1	0
V_{TSNC}	0	1	0	1
V_{TSNC}	0	1	0	0
V_{TSNC}	0	0	1	1
V_{TSNC}	0	0	1	0
V_{TSNC}	0	0	0	1
V_{TSNC} = 0.74V_{TUSN1} without AC	0	0	0	0



Data byte ALGN2: SSL1 = 0, SSL0 = 1

Data byte ALGN2

CURVE	SST3	SST2	SST1	SST0
(1)	0	0	0	0
(2)	1	0	0	0
(3)	1	1	1	1

Fig.9 Channel separation as a function of voltage at pins TSNC, TWBAM1 and TUSN1 (fixed slope).

11.7 Write mode: subaddress 3H

Table 28 Format of data byte Alignment 3 (ALGN3)

7	6	5	4	3	2	1	0
NBS1	NBS0	DE75	HCCS	HST1	HST0	HSL1	HSL0

Table 29 Description of ALGN3 bits

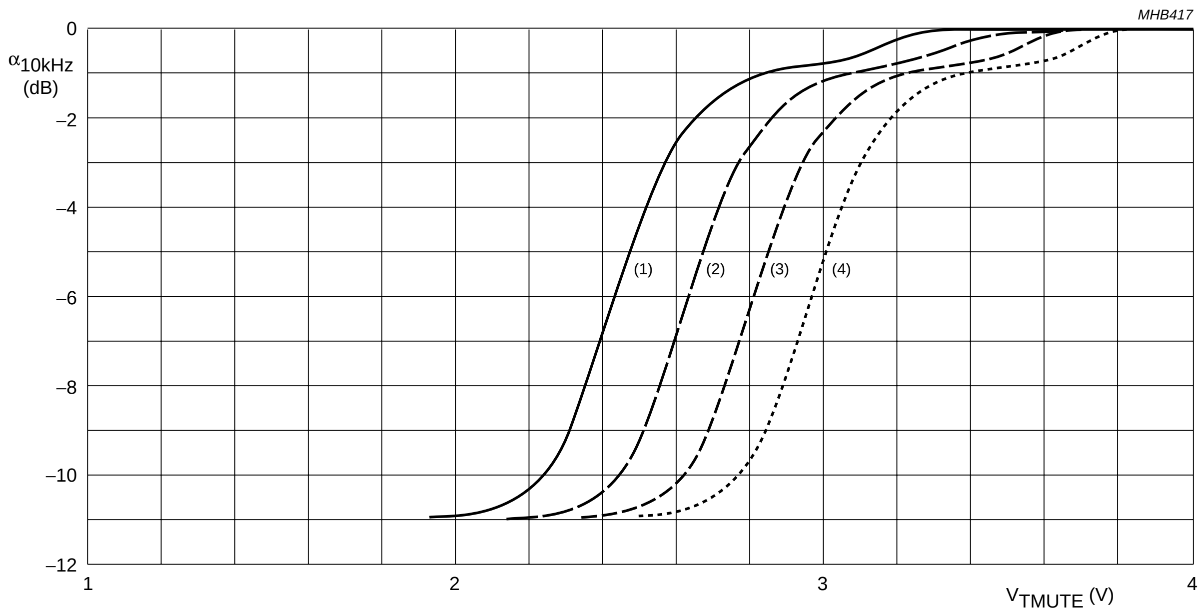
BIT	SYMBOL	DESCRIPTION
7	NBS1	**Noise blanker sensitivity.** These 2 bits determine the noise blanker sensitivity levels; see Table 30.
6	NBS0	
5	DE75	**De-emphasis.** If DE75 = 1, then de-emphasis is 75 µs. If DE75 = 1, then de-emphasis is 50 µs.
4	HCCS	**HCC control switch.** With static roll-off: HCCS = 1, C_{FMLBUF} = C_{FMRBUF} = 2.7 nF. Without static roll-off: HCCS = 0, C_{FMLBUF} = C_{FMRBUF} = 680 pF.
3	HST1	**HCC start alignment.** These 2 bits determine the alignment for the start of high cut control; see Table 31 and Fig.10.
2	HST0	
1	HSL1	**HCC slope alignment.** These 2 bits determine the alignment for the slope of high cut control; see Table 32 and Fig.11.
0	HSL0	

Table 30 Setting of noise blanker sensitivity

$V_{pulse(p)(MPX)}$ (mV)	$V_{pulse(p)(level)}$ (mV)	NBS1	NBS0
12	110	1	1
24	120	1	0
60	150	0	1
120	200	0	0

Table 31 Setting of alignment for start of high cut control (α_{10kHz} = 3 dB)

$V_{(3-10)DC}$ (V)	HST1	HST0
1.30	1	1
1.45	1	0
1.90	0	1
2.10	0	0



Data byte ALGN3: HSL1 = 1, HSL0 = 0

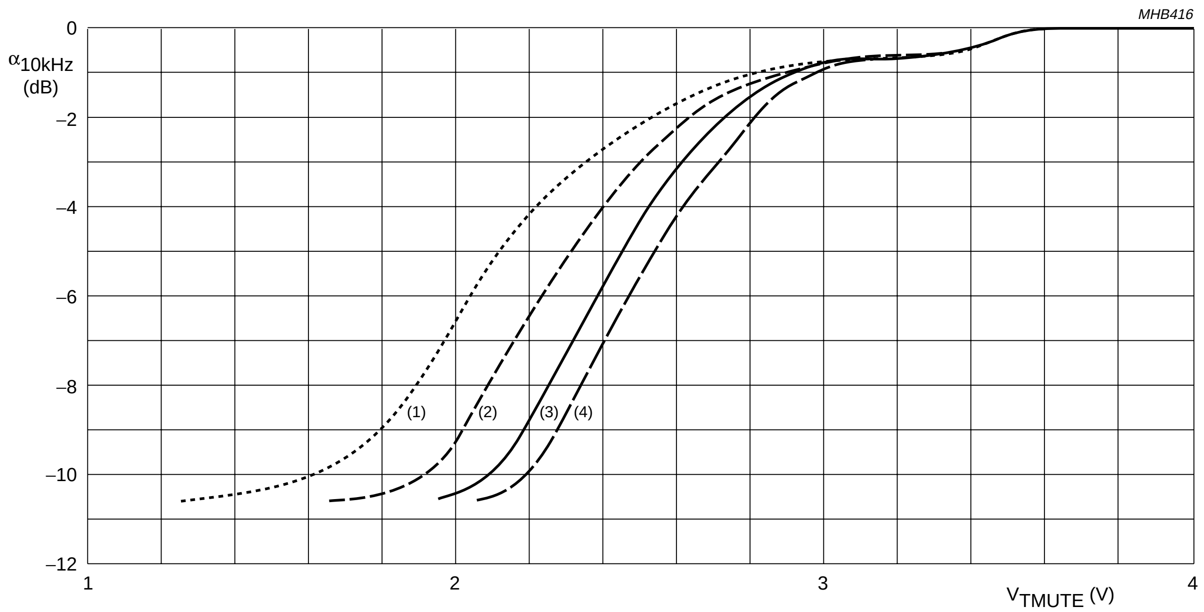
Data byte ALGN3

CURVE	HST1	HST0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

Fig.10 High cut control as a function of V_{TMUTE} (fixed slope).

Table 32 Setting of alignment for slope of high cut control (V_{TMUTE} = 2.4 V)

α_{10kHz} (dB)	HSL1	HSL0
7.5	1	1
6.0	1	0
4.0	0	1
3.0	0	0



Data byte ALGN3: HST1 = 1, HST0 = 1

Data byte ALGN3

CURVE	HSL1	HSL0
(1)	0	0
(2)	0	1
(3)	1	0
(4)	1	1

Fig.11 High cut control as a function of V_{TMUTE} (fixed start).

11.8 Write mode: subaddress 4H

Table 33 Format of data byte Source Selector (SSEL)

7	6	5	4	3	2	1	0
ASI1	ASI0	RSA2	RSA1	RSA0	MSS2	MSS1	MSS0

Table 34 Description of SSEL bits

BIT	SYMBOL	DESCRIPTION
7	ASI1	**ASI/ABC speed selection.** These 2 bits select the ASI/ABC speed (time per step); see Table 35.
6	ASI0	
5	RSA2	**Rear seat audio selector.** These 3 bits select the source for the rear outputs; see Table 36.
4	RSA1	
3	RSA0	
2	MSS2	**Main source selector.** These 3 bits select the source for the main control part; see Table 37.
1	MSS1	
0	MSS0	

Table 35 ASI/ABC speed selection (C_{ASICAP} = 15 nF)

ASI/ABC SPEED (ms)	ASI1	ASI0
20	1	1
8.33	1	0
3.33	0	1
0.83	0	0

Table 36 Selected source for rear outputs

SELECTED SOURCE	RSA2	RSA1	RSA0
Internal, main channel(1)	1	1	1
Internal, main channel(1)	1	1	0
Internal, main channel(1)	1	0	1
Internal, main channel	1	0	0
AM/FM (internal)	0	1	1
Input A (stereo)	0	1	0
Input B (stereo)	0	0	1
Input C (stereo, symmetrical)	0	0	0

Note

1. Not tested; function not guaranteed.

Table 37 Selected source for main control part

SELECTED SOURCE	MSS2	MSS1	MSS0
Chime input[(1)]	1	1	1
Chime input[(1)]	1	1	0
Chime input	1	0	1
Input D (mono, symmetrical)	1	0	0
AM/FM (internal)	0	1	1
Input A (stereo)	0	1	0
Input B (stereo)	0	0	1
Input C (stereo, symmetrical)	0	0	0

Note

1. Not tested; function not guaranteed.

11.9 Write mode: subaddress 5H

Table 38 Format of data byte Bass control (BASS)

7	6	5	4	3	2	1	0
BSYC	–	BSYB	BAS4	BAS3	BAS2	BAS1	BAS0

Table 39 Description of BASS bits

BIT	SYMBOL	DESCRIPTION
7	BSYC	**Bass filter mode for cut.** If BSYC = 0, then shelving characteristic selected. If BSYC = 1, then band-pass filter characteristic selected.
6	–	This bit is not used and must be set to logic 0.
5	BSYB	**Bass filter mode for boost.** If BSYB = 0, then shelving characteristic selected. If BSYB = 1, then band-pass filter characteristic selected.
4	BAS4	**Bass control.** These 5 bits determine the bass control level; see Table 40.
3	BAS3	
2	BAS2	
1	BAS1	
0	BAS0	

Table 40 Setting of bass control level

BASS CONTROL (dB)	BAS4	BAS3	BAS2	BAS1	BAS0
+18(1)	1	1	1	1	1
+18(1)	1	1	1	1	0
+18(1)	1	1	1	0	1
+18(1)	1	1	1	0	0
+18(1)	1	1	0	1	1
+18	1	1	0	1	0
+16	1	1	0	0	1
+14	1	1	0	0	0
+12	1	0	1	1	1
+10	1	0	1	1	0
+8	1	0	1	0	1
+6	1	0	1	0	0
+4	1	0	0	1	1
+2	1	0	0	1	0
+0	1	0	0	0	1
–0	1	0	0	0	0
–2 (–1.8)	0	1	1	1	1
–4 (–3.6)	0	1	1	1	0
–6 (–5.4)	0	1	1	0	1
–8 (–7.1)	0	1	1	0	0
–10 (–8.7)	0	1	0	1	1
–12 (–10.3)	0	1	0	1	0
–14 (–11.7)	0	1	0	0	1
–16 (–13.1)	0	1	0	0	0
–18 (–14.4)	0	0	1	1	1
–18 (–14.4)(1)	0	0	1	1	0
–18 (–14.4)(1)	0	0	1	0	1
–18 (–14.4)(1)	0	0	1	0	0
–18 (–14.4)(1)	0	0	0	1	1
–18 (–14.4)(1)	0	0	0	1	0
–18 (–14.4)(1)	0	0	0	0	1
–18 (–14.4)(1)	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.10 Write mode: subaddress 6H

Table 41 Format of data byte Treble control (TRBL)

7	6	5	4	3	2	1	0
HSTM	–	–	–	TRE3	TRE2	TRE1	TRE0

Table 42 Description of TRBL bits

BIT	SYMBOL	DESCRIPTION
7	HSTM	**Test mode muting average and SNC peak detector.** If HSTM = 0, then normal operation. If HSTM = 1, then increased detector currents.
6	–	These 3 bits are not used; each must be set to logic 0.
5	–	
4	–	
3	TRE3	**Treble control.** These 4 bits determine the treble control level; see Table 43.
2	TRE2	
1	TRE1	
0	TRE0	

Table 43 Setting of treble control level

TREBLE CONTROL (dB)	TRE3	TRE2	TRE1	TRE0
+14	1	1	1	1
+12	1	1	1	0
+10	1	1	0	1
+8	1	1	0	0
+6	1	0	1	1
+4	1	0	1	0
+2	1	0	0	1
+0	1	0	0	0
–0	0	1	1	1
–2	0	1	1	0
–4	0	1	0	1
–6	0	1	0	0
–8	0	0	1	1
–10	0	0	1	0
–12	0	0	0	1
–14	0	0	0	0

11.11 Write mode: subaddress 7H

Table 44 Format of data byte Loudness control (LOUD)

7	6	5	4	3	2	1	0
LOFF	–	–	LSN4	LSN3	LSN2	LSN1	LSN0

Table 45 Description of LOUD bits

BIT	SYMBOL	DESCRIPTION
7	LOFF	**Loudness switch control.** If LOFF = 0, then the loudness switch is on. If LOFF = 1, then loudness switch is off.
6	–	These 2 bits are not used, each must be set to logic 0.
5	–	
4	LSN4	**Loudness control.** These 5 bits determine the attenuation of the loudness block; see Table 46.
3	LSN3	
2	LSN2	
1	LSN1	
0	LSN0	

Table 46 Attenuation of loudness block

ATTENUATION (dB)	LSN4	LSN3	LSN2	LSN1	LSN0
0	1	1	1	1	1
–1	1	1	1	1	0
–2	1	1	1	0	1
–3	1	1	1	0	0
–4	1	1	0	1	1
–5	1	1	0	1	0
–6	1	1	0	0	1
–7	1	1	0	0	0
–8	1	0	1	1	1
–9	1	0	1	1	0
–10	1	0	1	0	1
–11	1	0	1	0	0
–12	1	0	0	1	1
–13	1	0	0	1	0
–14	1	0	0	0	1
–15	1	0	0	0	0
–16	0	1	1	1	1
–17	0	1	1	1	0
–18	0	1	1	0	1
–19	0	1	1	0	0
–20	0	1	0	1	1
–20(1)	0	1	0	1	0
–20(1)	0	1	0	0	1

ATTENUATION (dB)	LSN4	LSN3	LSN2	LSN1	LSN0
−20(1)	0	1	0	0	0
−20(1)	0	0	1	1	1
−20(1)	0	0	1	1	0
−20(1)	0	0	1	0	1
−20(1)	0	0	1	0	0
−20(1)	0	0	0	1	1
−20(1)	0	0	0	1	0
−20(1)	0	0	0	0	1
−20(1)	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.12 Write mode: subaddress 8H

Table 47 Format of data byte Volume 1 control (VOLU1)

7	6	5	4	3	2	1	0
AMUT	–	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

Table 48 Description of VOLU1 bits

BIT	SYMBOL	DESCRIPTION
7	AMUT	**Audio mute switch.** If AMUT = 0, then there is no audio mute. If AMUT = 1, then audio mute on.
6	–	This bit is not used and must be set to logic 0.
5 to 0	VOL[5:0]	**Volume 1 control.** These 6 bits determine the attenuation of volume 1 block; see Table 49.

Table 49 Attenuation of volume 1 block

ATTENUATION (dB)	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
+20(1)	1	1	1	1	1	1
+20(1)	1	1	1	1	1	0
+20(1)	1	1	1	1	0	1
+20	1	1	1	1	0	0
+19	1	1	1	0	1	1
+18	1	1	1	0	1	0
+17	1	1	1	0	0	1
+16	1	1	1	0	0	0
+15	1	1	0	1	1	1
+14	1	1	0	1	1	0
+13	1	1	0	1	0	1
+12	1	1	0	1	0	0
+11	1	1	0	0	1	1

ATTENUATION (dB)	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
+10	1	1	0	0	1	0
+9	1	1	0	0	0	1
+8	1	1	0	0	0	0
+7	1	0	1	1	1	1
+6	1	0	1	1	1	0
+5	1	0	1	1	0	1
+4	1	0	1	1	0	0
+3	1	0	1	0	1	1
+2	1	0	1	0	1	0
+1	1	0	1	0	0	1
0	1	0	1	0	0	0
–1	1	0	0	1	1	1
–2	1	0	0	1	1	0
–3	1	0	0	1	0	1
–4	1	0	0	1	0	0
–5	1	0	0	0	1	1
–6	1	0	0	0	1	0
–7	1	0	0	0	0	1
–8	1	0	0	0	0	0
–9	0	1	1	1	1	1
–10	0	1	1	1	1	0
–11	0	1	1	1	0	1
–12	0	1	1	1	0	0
–13	0	1	1	0	1	1
–14	0	1	1	0	1	0
–15	0	1	1	0	0	1
–16	0	1	1	0	0	0
–17	0	1	0	1	1	1
–18	0	1	0	1	1	0
–19	0	1	0	1	0	1
–20	0	1	0	1	0	0
–21	0	1	0	0	1	1
–22	0	1	0	0	1	0
–23	0	1	0	0	0	1
–24	0	1	0	0	0	0
–25	0	0	1	1	1	1
–26	0	0	1	1	1	0
–27	0	0	1	1	0	1
–28	0	0	1	1	0	0
–29	0	0	1	0	1	1
–30	0	0	1	0	1	0

ATTENUATION (dB)	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
–31	0	0	1	0	0	1
–32	0	0	1	0	0	0
–33	0	0	0	1	1	1
–34	0	0	0	1	1	0
–35	0	0	0	1	0	1
–36	0	0	0	1	0	0
–36(1)	0	0	0	0	1	1
–36(1)	0	0	0	0	1	0
–36(1)	0	0	0	0	0	1
–36(1)	0	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.13 Write mode: subaddress 9H

Table 50 Format of data byte Volume 2, left front (VOL2_LF)

7	6	5	4	3	2	1	0
CHML	–	VLF5	VLF4	VLF3	VLF2	VLF1	VLF0

Table 51 Description of VOL2_LF bits

BIT	SYMBOL	DESCRIPTION
7	CHML	**Chime adder left front select.** If CHML = 1, then chime on. If CHML = 0, then chime off.
6	–	This bit is not used and must be set to logic 0.
5 to 0	VLF[5:0]	**Left front volume 2, balance and fader control.** These 6 bits determine the attenuation of volume 2 left front; see Table 52.

Table 52 Attenuation of volume 2 left front

ATTENUATION (dB)	VLF5	VLF4	VLF3	VLF2	VLF1	VLF0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0

ATTENUATION (dB)	VLF5	VLF4	VLF3	VLF2	VLF1	VLF0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
–56	0	0	0	1	1	1
–58.5	0	0	0	1	1	0
–62	0	0	0	1	0	1
–68	0	0	0	1	0	0
Mute left front	0	0	0	0	1	1
Mute left front(1)	0	0	0	0	1	0
Mute left front(1)	0	0	0	0	0	1
Mute left front(1)	0	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.14 Write mode: subaddress AH

Table 53 Format of data byte Volume 2, right front (VOL2_RF)

7	6	5	4	3	2	1	0
CHMR	–	VRF5	VRF4	VRF3	VRF2	VRF1	VRF0

Table 54 Description of VOL2_RF bits

BIT	SYMBOL	DESCRIPTION
7	CHMR	**Chime adder right front select.** If CHMR = 1, then chime on. If CHMR = 0, then chime off.
6	–	This bit is not used and must be set to logic 0.
5 to 0	VRF[5:0]	**Right front volume 2, balance and fader control.** These 6 bits determine the attenuation of volume 2 right front; see Table 55.

Table 55 Attenuation of volume 2 right front

ATTENUATION (dB)	VRF5	VRF4	VRF3	VRF2	VRF1	VRF0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1

ATTENUATION (dB)	VRF5	VRF4	VRF3	VRF2	VRF1	VRF0
–27	1	0	0	1	0	0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
–56	0	0	0	1	1	1
–58.5	0	0	0	1	1	0
–62	0	0	0	1	0	1
–68	0	0	0	1	0	0
Mute right front	0	0	0	0	1	1
Mute right front(1)	0	0	0	0	1	0
Mute right front(1)	0	0	0	0	0	1
Mute right front(1)	0	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.15 Write mode: subaddress BH

Table 56 Format of data byte Volume 2, left rear (VOL2_LR)

7	6	5	4	3	2	1	0
–	–	VLR5	VLR4	VLR3	VLR2	VLR1	VLR0

Table 57 Description of VOL2_LR bits

BIT	SYMBOL	DESCRIPTION
7	–	These 2 bits are not used, each must be set to logic 0.
6	–	
5 to 0	VLR[5:0]	**Left rear volume 2, balance and fader control.** These 6 bits determine the attenuation of volume 2 left rear; see Table 58.

Table 58 Attenuation of volume 2 left rear

ATTENUATION (dB)	VLR5	VLR4	VLR3	VLR2	VLR1	VLR0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0

ATTENUATION (dB)	VLR5	VLR4	VLR3	VLR2	VLR1	VLR0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
–56	0	0	0	1	1	1
–58.5	0	0	0	1	1	0
–62	0	0	0	1	0	1
–68	0	0	0	1	0	0
Mute left rear	0	0	0	0	1	1
Mute left rear(1)	0	0	0	0	1	0
Mute left rear(1)	0	0	0	0	0	1
Mute left rear(1)	0	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

11.16 Write mode: subaddress CH

Table 59 Format of data byte Volume 2, right rear (VOL2_RR)

7	6	5	4	3	2	1	0
–	–	VRR5	VRR4	VRR3	VRR2	VRR1	VRR0

Table 60 Description of VOL2_RR bits

BIT	SYMBOL	DESCRIPTION
7	–	These 2 bits are not used, each must be set to logic 0.
6	–	
5 to 0	VRR[5:0]	**Right rear volume 2, balance and fader control.** These 6 bits determine the attenuation of volume 2 right rear, see Table 61.

Table 61 Attenuation of volume 2 right rear

ATTENUATION (dB)	VRR5	VRR4	VRR3	VRR2	VRR1	VRR0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0

ATTENUATION (dB)	VRR5	VRR4	VRR3	VRR2	VRR1	VRR0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
–56	0	0	0	1	1	1
–58.5	0	0	0	1	1	0
–62	0	0	0	1	0	1
–68	0	0	0	1	0	0
Mute right rear	0	0	0	0	1	1
Mute right rear(1)	0	0	0	0	1	0
Mute right rear(1)	0	0	0	0	0	1
Mute right rear(1)	0	0	0	0	0	0

Note

1. Not tested; function not guaranteed.

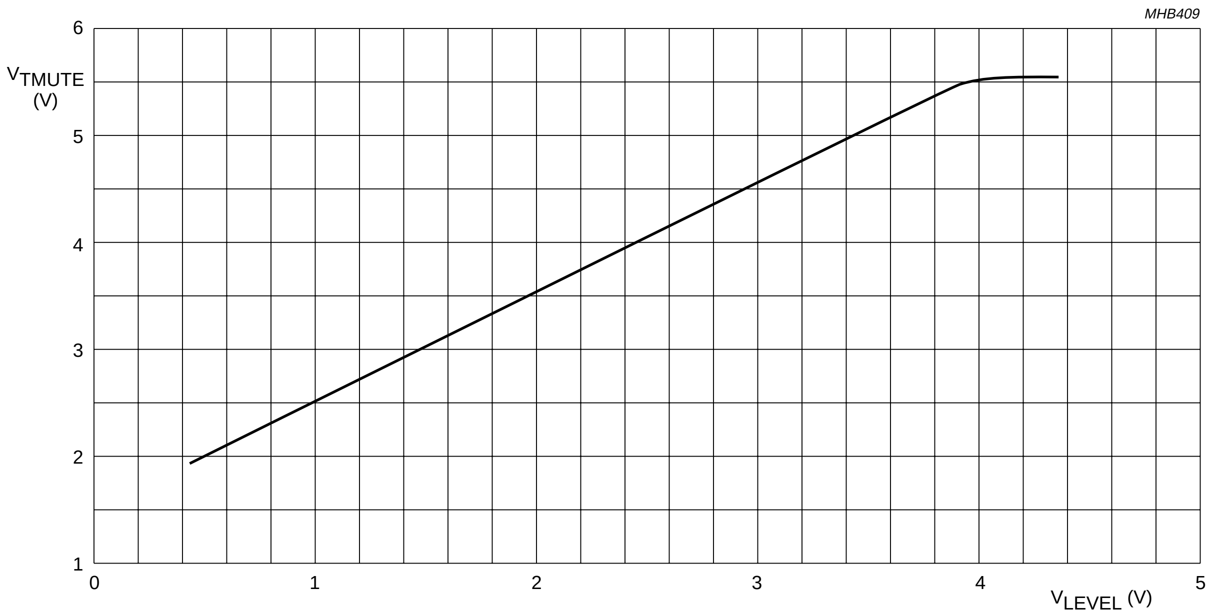


Fig.12 Muting average detector (TMUTE) dependency on level (LEVEL) and stereo noise control peak detector (TSNC) dependency on level (LEVEL).

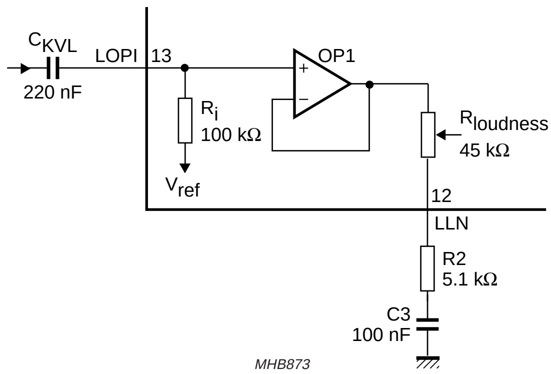


Fig.13 External circuit for loudness with bass boost only.

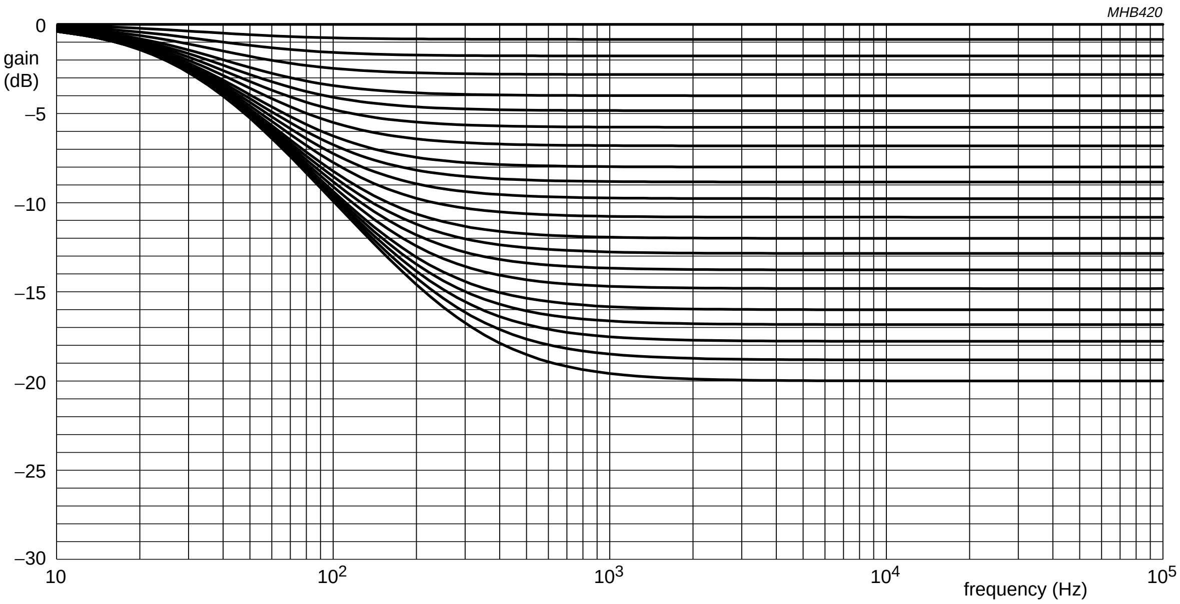


Fig.14 Loudness with bass boost only without influence of coupling capacitors C_{KVL} and C_{KVR}.

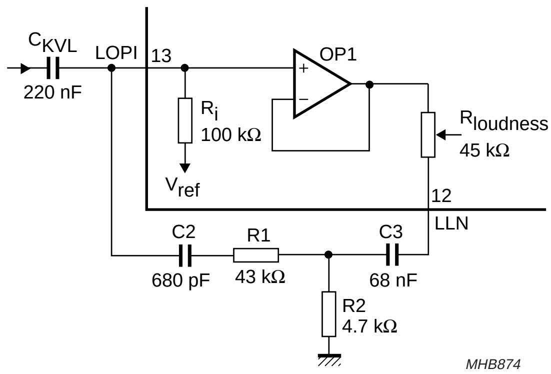


Fig.15 External circuit for loudness with bass and treble boost.

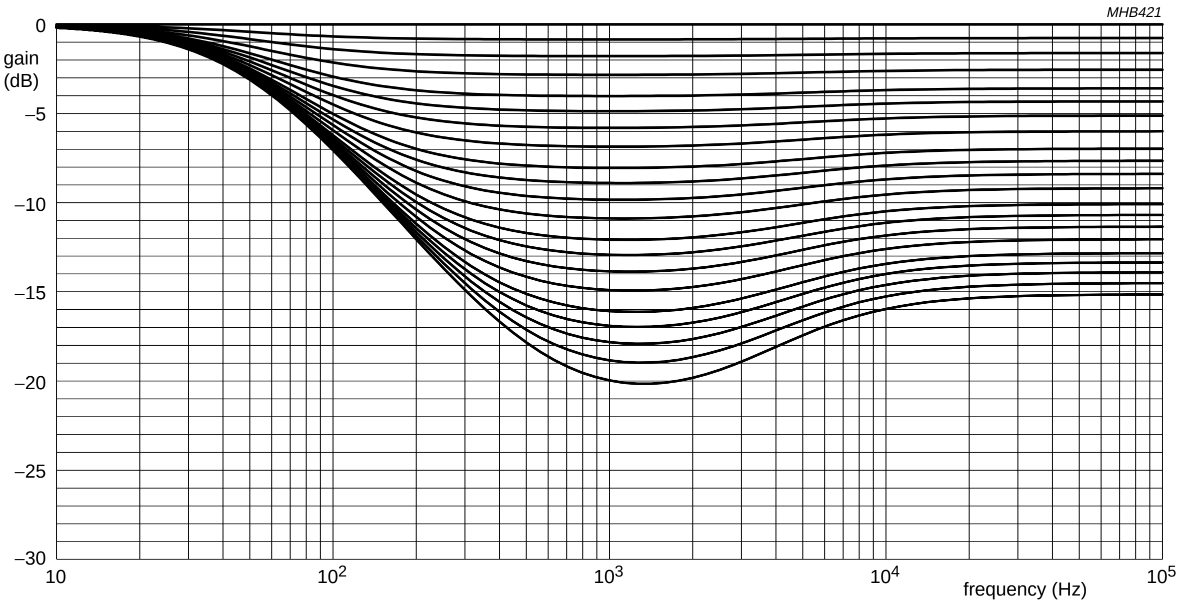


Fig.16 Loudness with bass and treble boost without influence of coupling capacitors C_{KVL} and C_{KVR}.

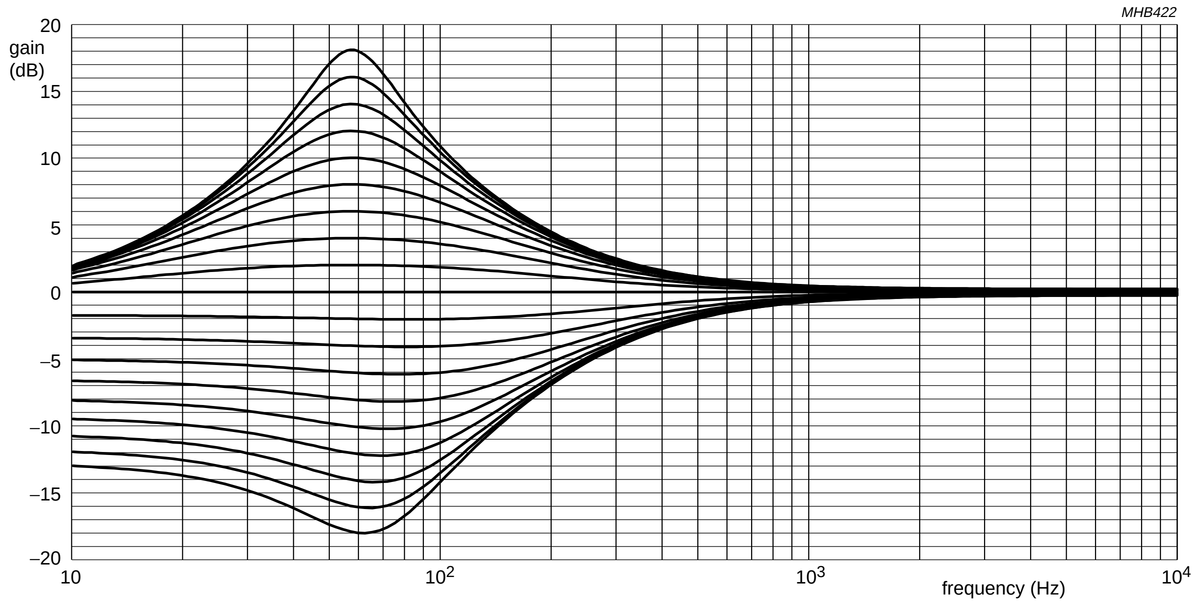


Fig.17 Bass curve with 2 × 220 nF and R = 3.3 kΩ external, BSYB = 1 for gain and BSYC = 0 for cut.

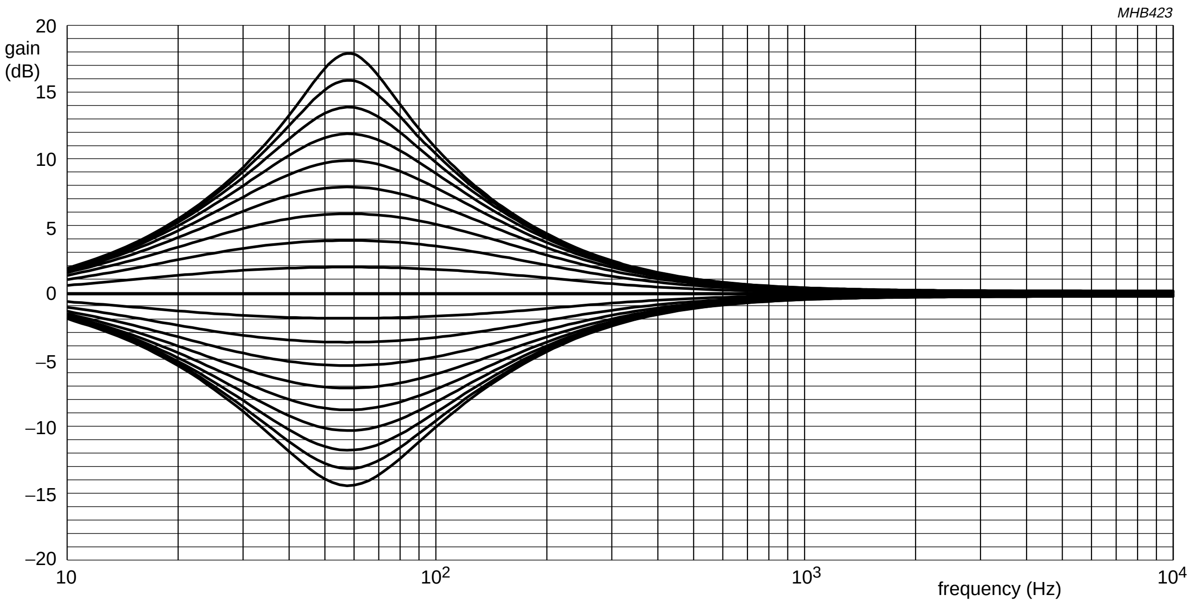


Fig.18 Bass curve with 2 × 220 nF and R = 3.3 kΩ external, BSYB = 1 and BSYC = 1.

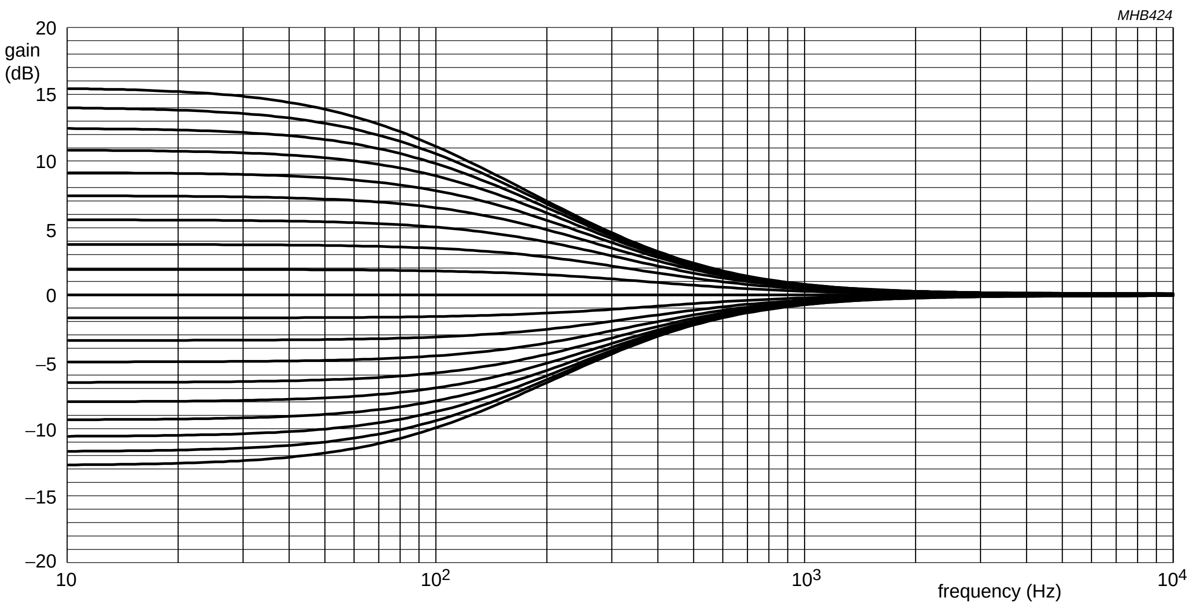


Fig.19 Bass curve with 1 × 47 nF external, between RBI and RBO, BSYB = 0 and BSYC = 0.

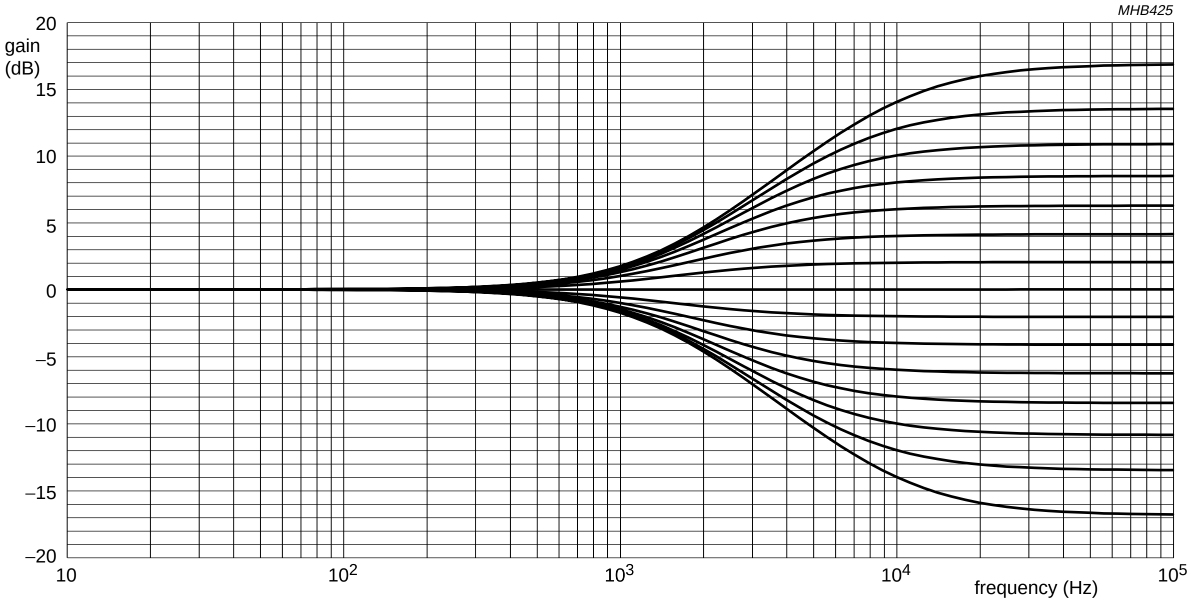
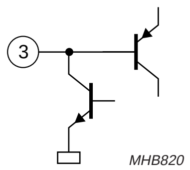
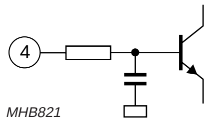
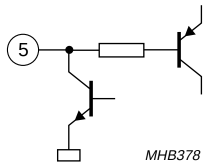
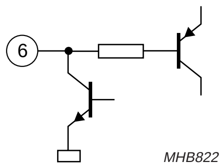
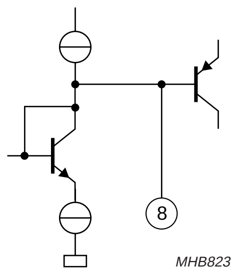
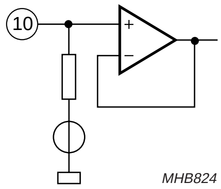
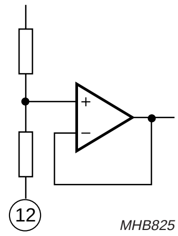
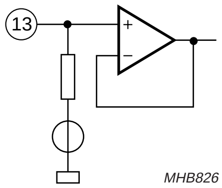
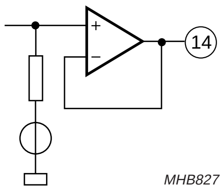
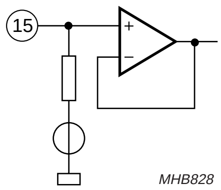


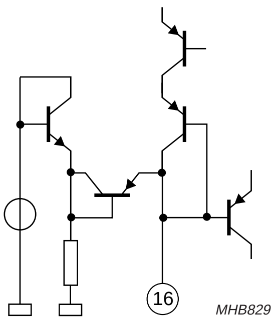
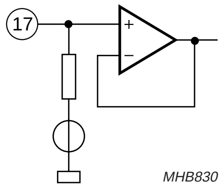
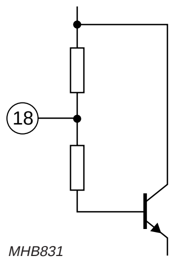
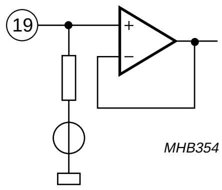
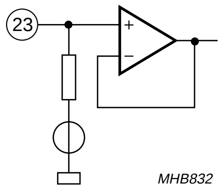
Fig.20 Treble control characteristic.

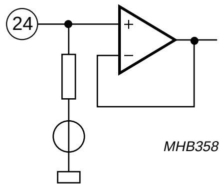
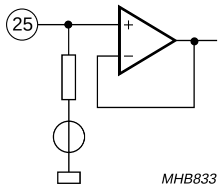
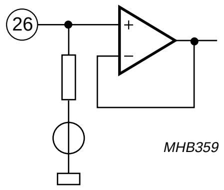
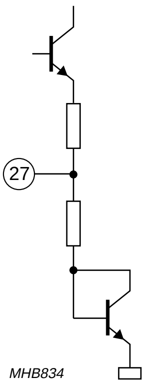
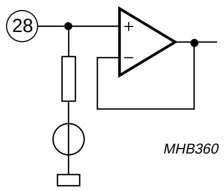
12 INTERNAL CIRCUITRY

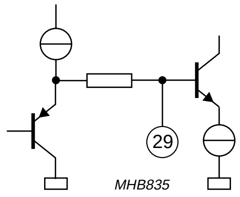
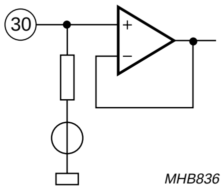
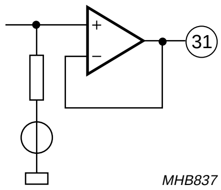
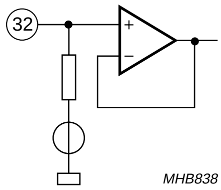
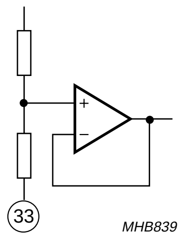
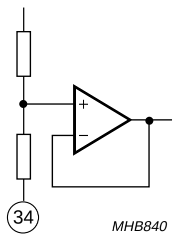
Table 62 Equivalent pin circuits

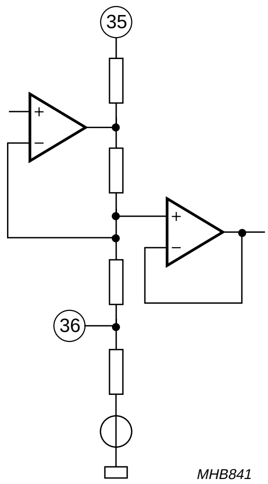
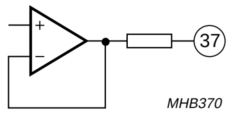
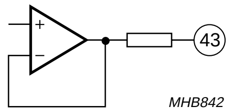
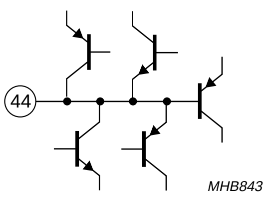
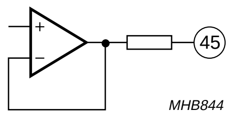
PIN	SYMBOL	EQUIVALENT CIRCUIT
1	n.c.	
2	n.c.	
3	SCLQ	
4	LEVEL	
5	SCL	
6	SDA	
7	DGND	
8	TBL	
9	V_{CC}	

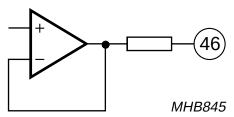
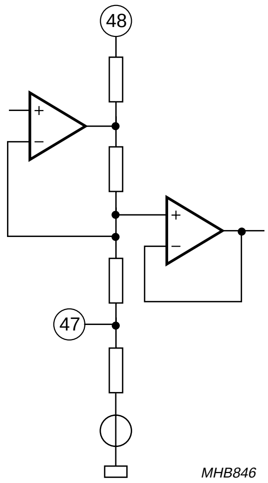
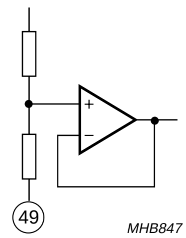
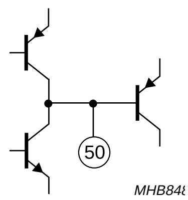
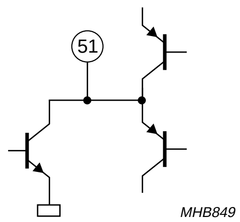
PIN	SYMBOL	EQUIVALENT CIRCUIT
10	CHIME	
11	AGND	
12	LLN	
13	LOPI	
14	LOPO	
15	BRI	

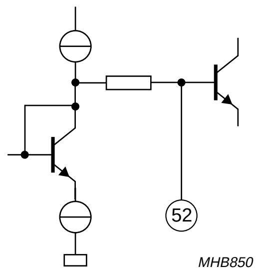
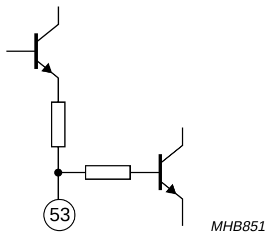
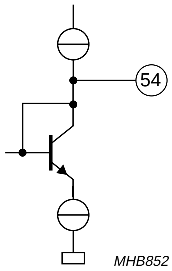
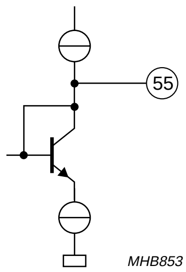
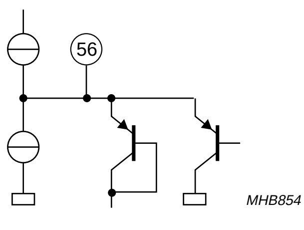
PIN	SYMBOL	EQUIVALENT CIRCUIT
16	ADR	
17	BLI	
18	SCAP	
19	CRIP	
20	n.c.	
21	n.c.	
22	n.c.	
23	CCOM	

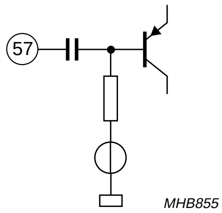
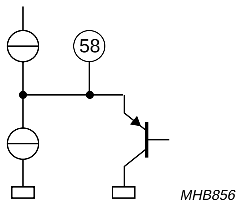
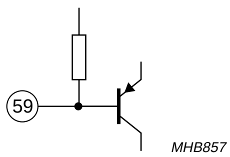
PIN	SYMBOL	EQUIVALENT CIRCUIT
24	CLIP	
25	MONOC	
26	MONOP	
27	VHS	
28	ARI	

PIN	SYMBOL	EQUIVALENT CIRCUIT
29	AMNCAP	
30	ALI	
31	ROPO	
32	ROPI	
33	RLN	
34	RTC	

PIN	SYMBOL	EQUIVALENT CIRCUIT
35	RBI	
36	RBO	
37	RF	
38	n.c.	
39	n.c.	
40	n.c.	
41	n.c.	
42	n.c.	
43	RR	
44	ASICAP	
45	LR	

PIN	SYMBOL	EQUIVALENT CIRCUIT
46	LF	
47	LBO	
48	LBI	
49	LTC	
50	AMPCAP	
51	AMHOLD	

PIN	SYMBOL	EQUIVALENT CIRCUIT
52	AMHCAP	
53	I_{ref}	
54	TWBAM2	
55	TUSN2	
56	PHASE	

PIN	SYMBOL	EQUIVALENT CIRCUIT
57	f_{ref}	
58	PILOT	
59	AFSAMPLE	
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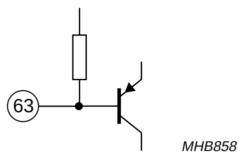
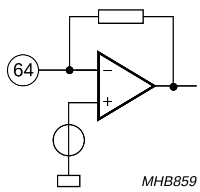
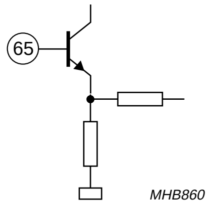
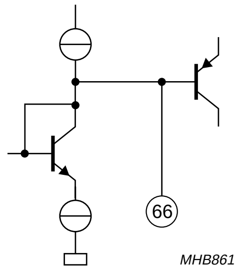
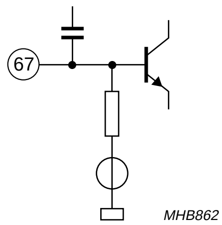
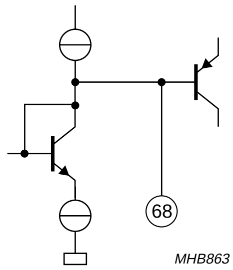
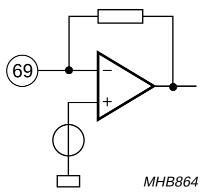
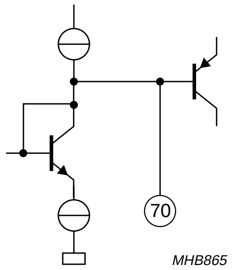
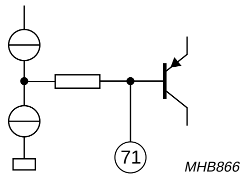
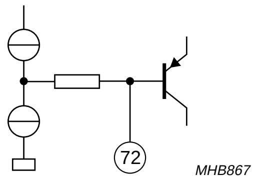
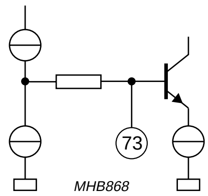
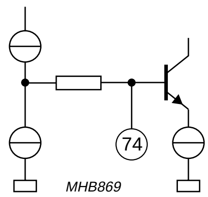
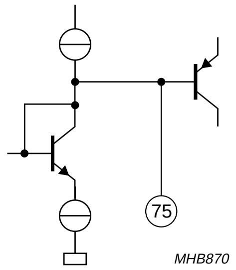
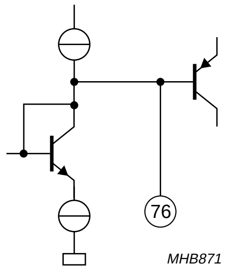
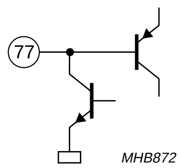
61	n.c.	
62	n.c.	
63	FMHOLD	
64	AMHIN	

PIN	SYMBOL	EQUIVALENT CIRCUIT
65	AMNBIN	
66	TMUTE	
67	MPXRDS	
68	TSNC	
69	MPXIN	

PIN	SYMBOL	EQUIVALENT CIRCUIT
70	FMNCAP	
71	DEEML	
72	DEEMR	
73	FMLBUF	
74	FMRBUF	

PIN	SYMBOL	EQUIVALENT CIRCUIT
75	TWBAM1	
76	TUSN1	
77	SDAQ	
78	n.c.	
79	n.c.	
80	n.c.	

13 TEST CIRCUIT

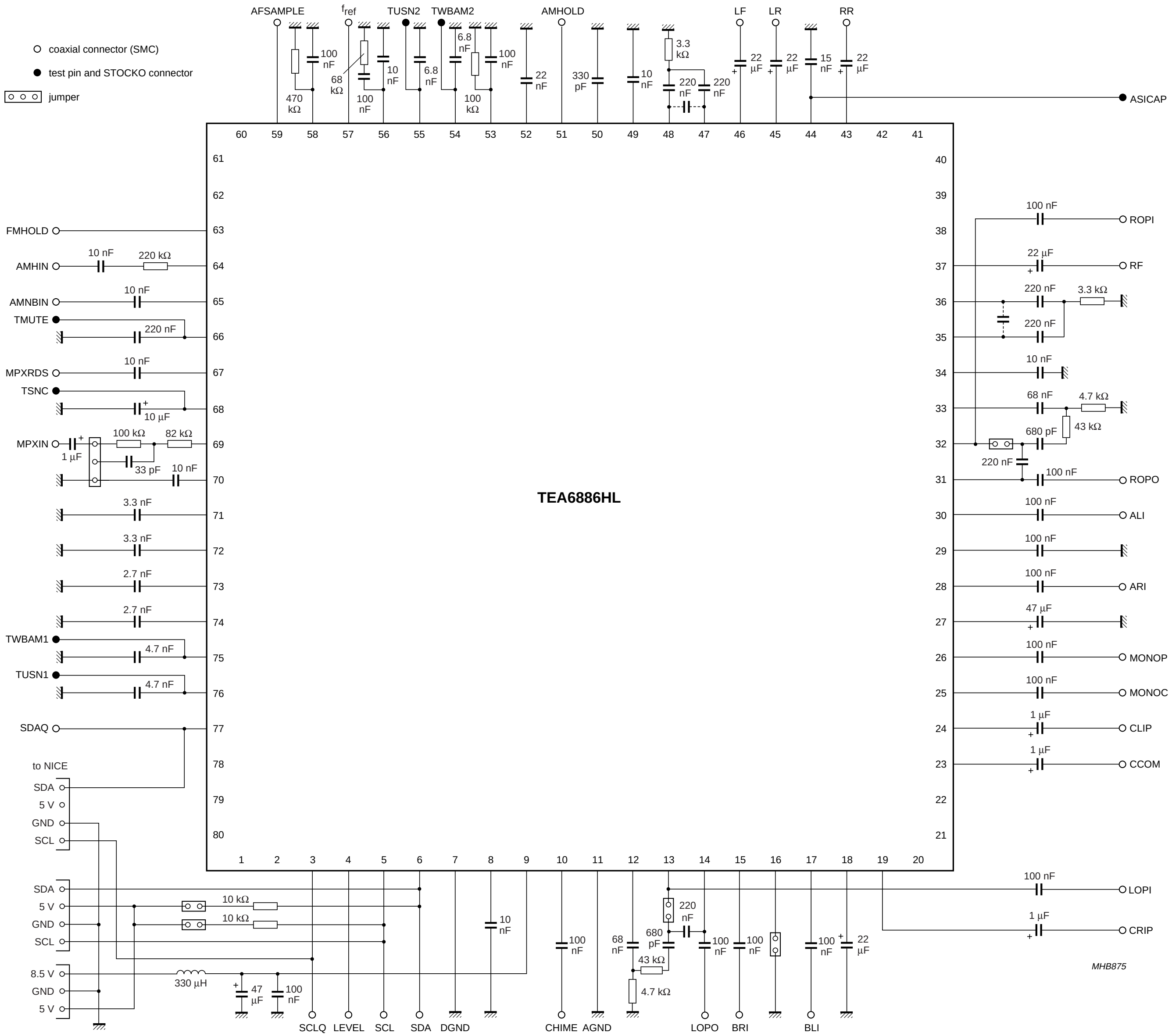
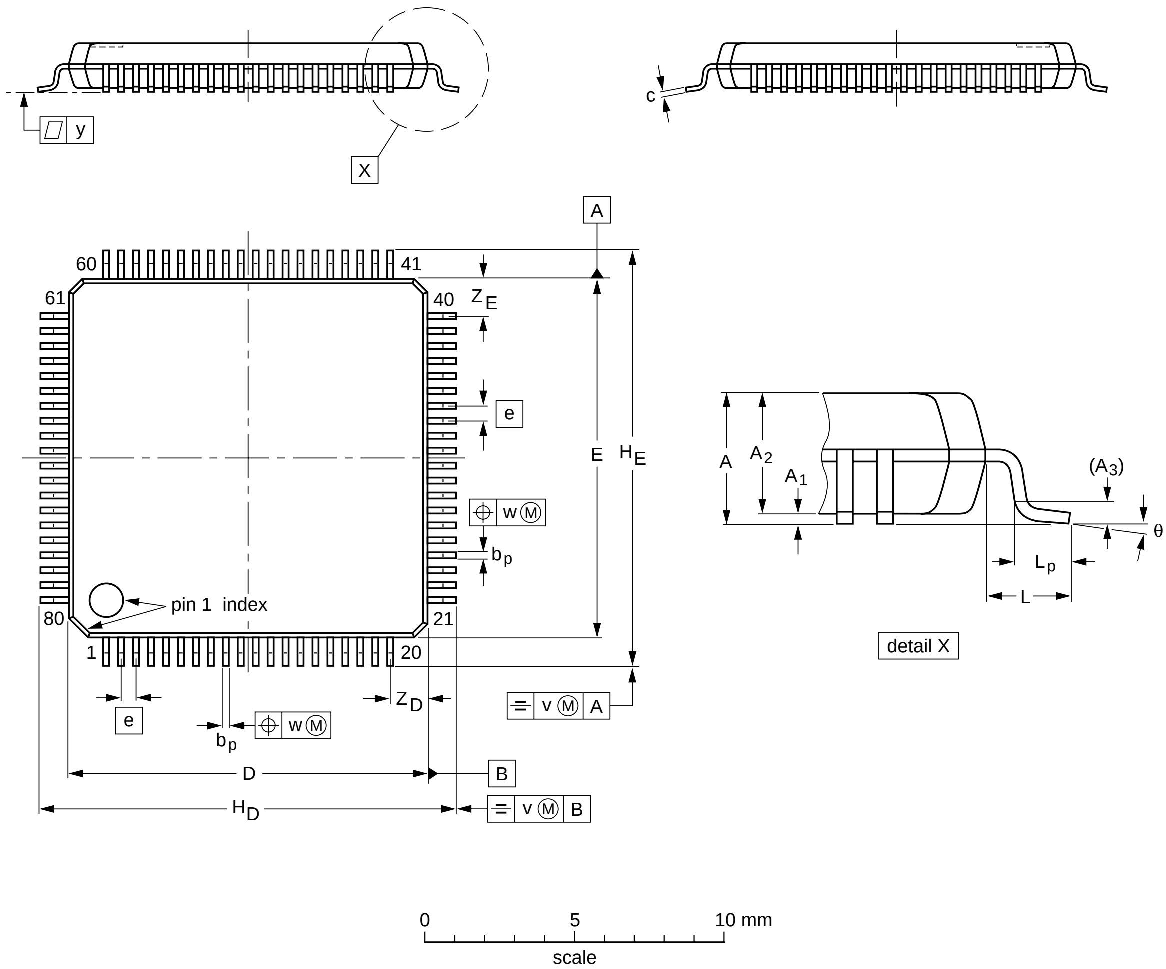


Fig.21 Test circuit.

14 PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1	136E15	MS-026				~~99-12-27~~ 00-01-19

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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