T-51-10-05

TELEDYNE COMPONENTS

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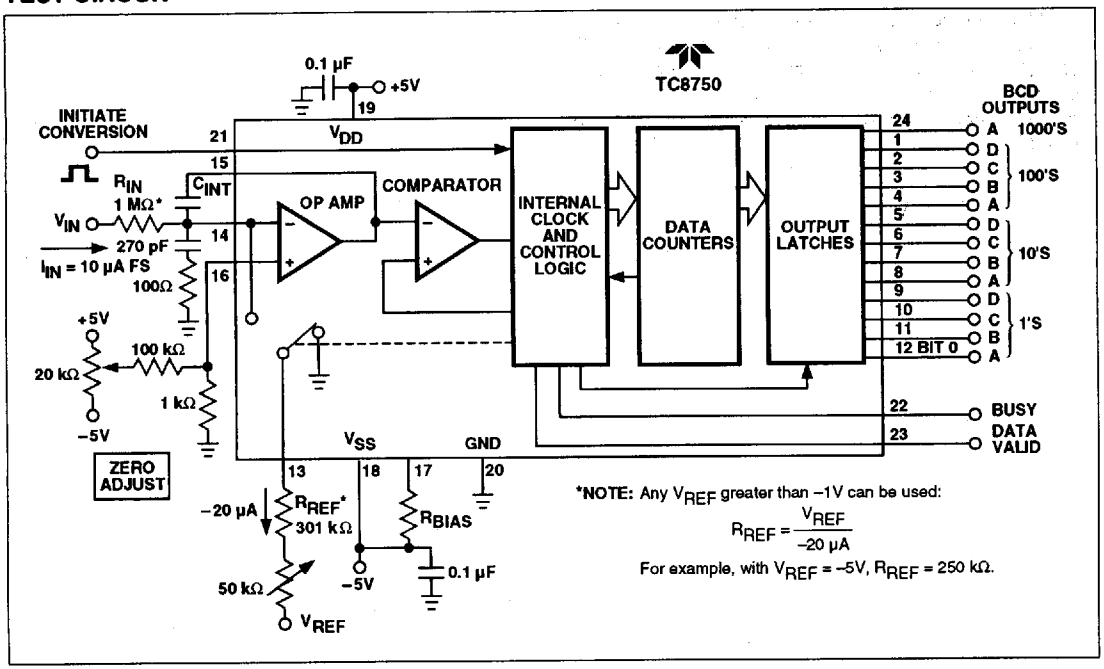
TC8750

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL BDC OUTPUT

FEATURES

- High Accuracy, 3-1/2 Digit Resolution With ≤±0.025% Error
- Military Temperature Range Devices
- Monotonic Performance
  - No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation .....20 mW Typ
- Contains All Required Active Elements
  - Needs Only Passive Support Components, Reference Voltage, and Dual Power Supplies
- High Stability Over Full Temperature Range
  - Gain Temperature Coefficient ...<25 ppm/°C Typ
  - Zero Drift .....<30 µV/°C Typ
  - Differential Nonlinearity Drift ...<2.5 ppm/°C Typ
- Latched Parallel BDC Outputs
- LPTTL and CMOS Compatible Outputs and Control Inputs
- Strobed or Free-Running Conversion
- Infinite Input Range
  - Any Positive Voltage Can Be Applied via a Scaling Resistor

TEST CIRCUIT



*NOTE: Any V_{REF} greater than −1V can be used:

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example, with $V_{REF} = -5V$, $R_{REF} = 250\ k\Omega$.

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3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

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GENERAL DESCRIPTION

The TC8750 is a 3-1/2 digit, monolithic CMOS analog-to-digital converter. Fully self-contained in a single 24-pin dual-in-line package, the converter requires only passive support components, voltage or current references, and power supplies.

Conversion is performed by an incremental charge-balancing technique which has inherently high accuracy, linearity, and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current. The number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion, the total count is latched into the digital outputs in a 3-1/2 digit, parallel BDC digit format.

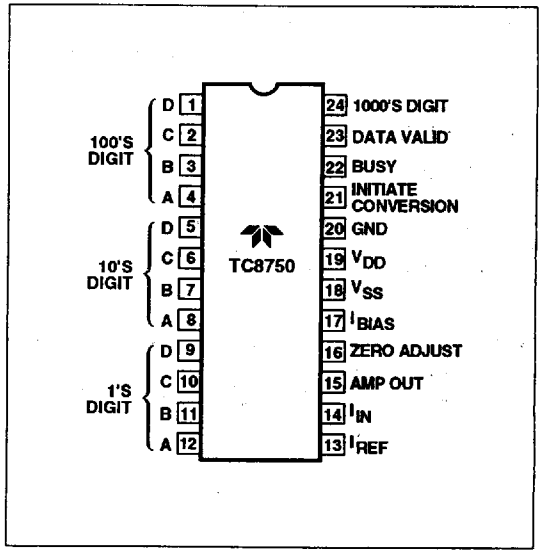
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC8750CPG	24-Pin Plastic DIP	0°C to +70°C
TC8750EHG	24-Pin CerDIP	–40°C to +85°C
TC8750MHG	24-Pin CerDIP	–55°C to +125°C

HANDLING PRECAUTIONS

CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, antistatic tubes or other conductive material. Use proper antistatic handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

PIN CONFIGURATION



3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = +5V, V_{SS} = –5V, V_{GND} = 0V, V_{REF} = –6.4V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = +25°C unless full temperature range is specified (–55°C to +125°C for MH package, –40°C to +85°C for EH package, 0° to +70°C for CP package).

Parameter	Definition	Conditions	Min	Typ	CP/EH Max	MH Max	Unit
Accuracy							
Resolution	BCD Word Length of Digital Output		3-1/2 (1999 Counts)	—	—	—	Digits
Accuracy Relative Accuracy	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input		—	—	0.025	0.025	%
Differential Nonlinearity	Deviation From 1 LSB Between Transition Points		—	—	—	0.025	%
Differential Nonlinearity Temperature Drift	Variation in Differential Nonlinearity Due to Temperature Change	Full Temperature Range	—	±2.5	±5	±5	ppm/°C
Gain Variance	Variation From Exact (Compensate By Trimming R_{IN} or R_{REF})		—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Variation In A Due to Temperature Change	Full Temperature Range	—	±25	±75	±80	ppm/°C
Zero Offset	Correction at Zero Adjust to Give Zero Output When Input is Zero	I_{IN} = 0	—	±10	±50	±50	mV
Zero Temperature Drift	Variation in Zero Offset Due to Temperature Change	Full Temperature Range	—	±3	±5	±8	ppm/°C
Analog Input (See Note)							
I_{IN} Full Scale	Full-Scale Analog Input Current to Achieve Specified Activity		—	10	—	—	µA
I_{REF}	Reference Current Input to Achieve Specified Accuracy		—	–20	—	—	µA
Digital Input							
$V_{IN}^{(1)}$	Logical "1" Input Threshold Current to Achieve Specified Activity		—	10	—	—	µA
$V_{IN}^{(0)}$	Logical "0" Input Threshold for Initiate Conversion Input	Full Temperature Range	—	—	1.5	1.5	V
Digital Output							
$V_{OUT}^{(1)}$	Logical "1" Output Voltage for Digits Out, Busy, and Data Valid Outputs	Full Temperature Range I_{OUT} = –10 µA I_{OUT} = –500 µA	4.5	—	—	—	V
$V_{OUT}^{(0)}$	Logical "0" Output Voltage for Digits Out, Busy, and Data Valid Outputs	Full Temperature Range V_{DD} = 4.75V I_{OUT} = 500 µA	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Time Required to Perform One Complete A/D Conversion	Full Temperature Range	—	10	12	12	ms

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ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Definition	Conditions	Min	Typ	CP/EH Max	MH Max	Unit
Dynamic (Cont.)							
Conversion Rate in Free-Run Mode		$V_{INT\ CONV}$ = +5V	84	100	—	—	Conv per sec
Minimum Pulse Width for Initiate Conversion		Full Temperature Range	500	—	—	—	ns
Supply Current							
I_{DD} Quiescent (H Package)	Current Required From Positive Supply During	Full Temperature Range	—	1.4	2.5	3.5	mA
(P Package)	Operation	$V_{INT\ CONV}$ = 0V	—	1.4	5		mA
I_{SS} Quiescent (H Package)	Current Required From Negative Supply During	Full Temperature Range	—	−1.6	−2.5	−3.5	mA
(P Package)	Operation	$V_{INT\ CONV}$ = 0V	—	−1.6	−5		mA
Supply Sensitivity	Change in Full-Scale Gain vs Supply Voltage Change	V_{DD} ± 1V, V_{SS} ±1V	—	±0.5	±1	±1	%/V
$\|V_{DD}\| = \|V_{SS}\|$ = 5V ±1V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies		±0.05	±0.1	±0.1	±0.1	%/V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

CIRCUIT DESCRIPTION

During conversion, the sum of a continuous current (I_{IN}) and pulses of a reference current (I_{REF}) are integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge is counted and the result (in BCD) is latched into the outputs at the end of conversion.

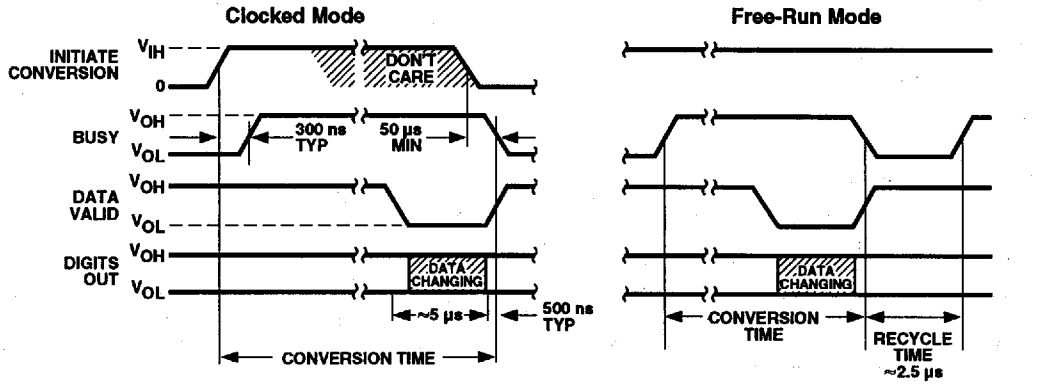
The conversion contains two counters and a clock, in addition to an operational amplifier, comparator, latching, output buffers, and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times I_{REF} is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 µs (times given are appropriate) start-up cycle begins. The integrating capacitor is discharged and both counters are reset during this start-up period. Conversion begins at the end of the reset pulse and ends with a pulse generated by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 µs shutdown cycle. During the shutdown cycle, Data Valid goes low for 5 µs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

TIMING DIAGRAMS



NOTE: Rise and fall times = 200 ns typical, C_L = 50 pF.

PIN FUNCTIONS

Initiate Conversion Input

Accepts CMOS and most 5V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 µA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 µA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 µs before the completion of a conversion cycle. During this 5 µs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Output (1's, 10's, 100's, 1000's)

The BDC digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

APPLICATIONS INFORMATION

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \bullet A \bullet R_{REF}}{R_{IN} \bullet V_{REF}}$$

$$A = 4128$$

where digital counts is the value of the BCD output word presented at Digits Out pins in response to V_{IN}.

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The digital output code format is as follows:

Analog Input	Digital Output
$V_{IN} \leq$ Full Scale	1100110011001
= Full Scale –1 LSB	1100110011001
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

External Component Selection

Obtaining a high-accuracy conversion system depends on the voltage regulation of V_{REF}, and thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. Supply connections V_{DD} and V_{SS} should have bypass capacitors of 0.1 µF or larger value right at the device pins.

R_{IN}, R_{REF}

Values of these components are chosen to give a full-scale input current of approximately 10 µA and a reference current of approximately –20 µA.

$$R_{IN} \approx \frac{V_{IN}\ \text{Full Scale}}{10\ \mu A} \qquad R_{REF} \approx \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \approx \frac{10V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \approx \frac{-6.4V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations; the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TC8750 are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and supply current. By decreasing R_{BIAS}, the ADC will convert much faster and the supply current will be much higher (e.g., when R_{BIAS} = 20 kΩ, the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA). Likewise, if R_{BIAS} is increased, the conversion time will be longer and the supply current will be much lower. (e.g., when R_{BIAS} = 1 MΩ, the conversion time will be six times longer, and the supply current is now reduced to 0.5 mA).

For details of this relationship, refer to the typical performance curves in Application Note 9.

R_{DAMP}

Exact value not critical, but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical, but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical, but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded, Locate as close as possible to pins 14 and 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended with 0.05% line and load regulation and 0.1 µF decoupling capacitors.

Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e., below zero and above full scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

1. Set the initiate conversion control high to provide free-run operation, and verify that converter is operating.
2. Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1-1/2 LSB, and trim the gain adjust circuit for a 1100110011000 to 1100110011001 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

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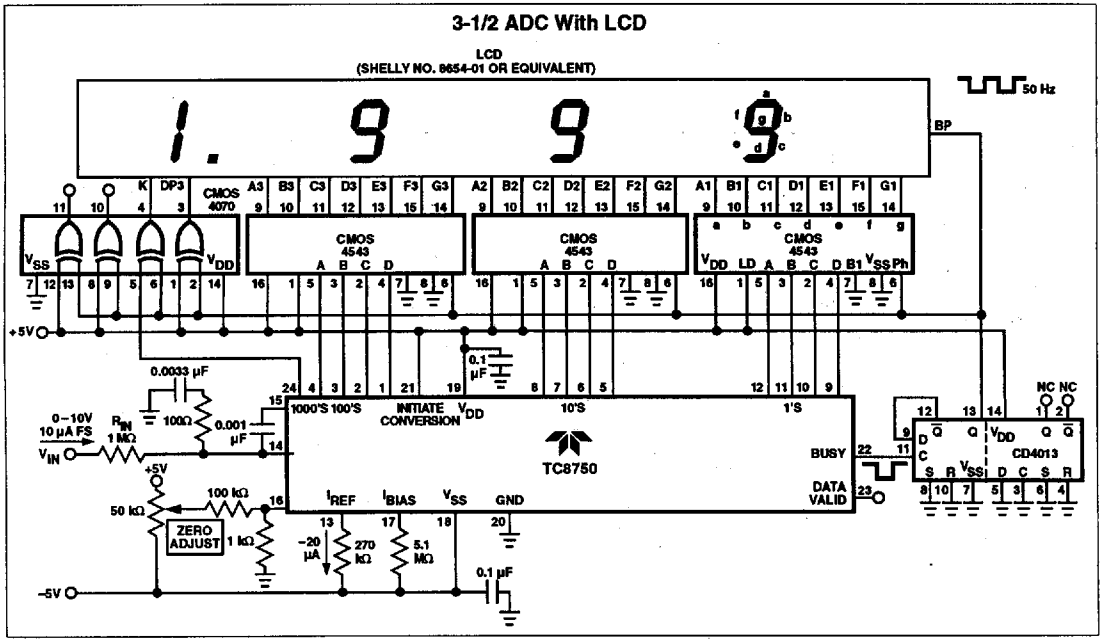
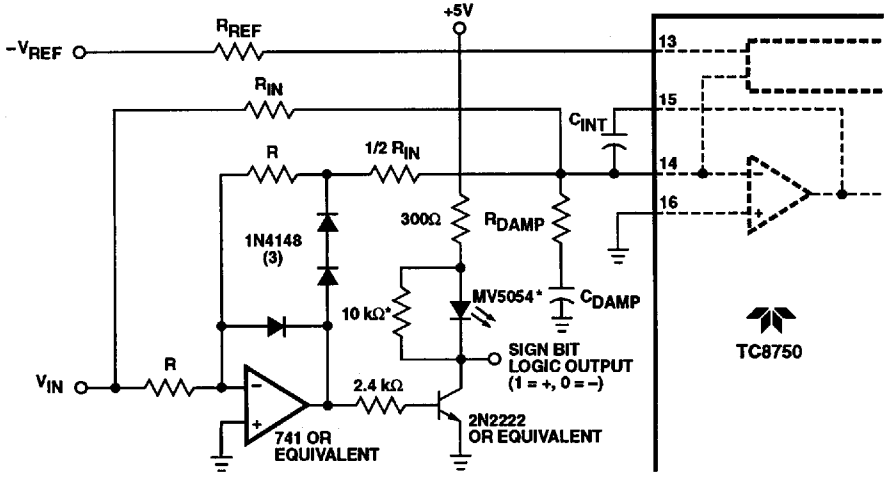
APPLICATION/DESIGN CIRCUITS

3-1/2 ADC With LCD



Bipolar Operation (+ and – Inputs)

ABSOLUTE VALUE CIRCUIT WITH SIGN



*Optional visual indication of negative input.
NOTE: Values for R should be between 10 kΩ and 100 kΩ.

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APPLICATION/DESIGN CIRCUITS (Cont.)

Microprocessor-Based ADC System