DATASHEET

SUNPLUS

SPL02E2

19.5KB LCD Controller/Driver

APR. 10, 2003

Version 1.0

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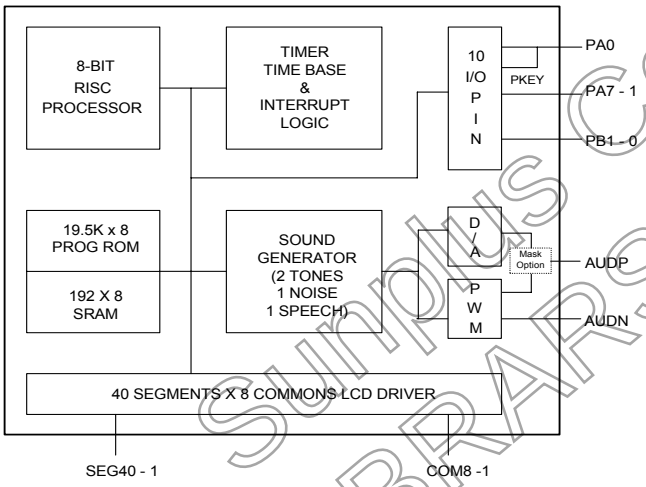
19.5KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPL02E2 is a CMOS 8-bit single chip micro-processor. With SUNPLUS state-of-the-art technology, it contains RAM, ROM, I/Os, one interrupt controller, two tone-generator, one noise generator, and one automatic display controller/driver. In addition, both PWM and current DAC audio outputs are provided in SPL02E2. Depending on the application, users are welling to select one of the audio types through mask option. To reduce power consumption, a software controllable standby switch is built-in to save the power. The SPL02E2 is a low cost but powerful IC that targets to fulfill various LCD application needs.

2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit RISC processor
- 192-byte SRAM
- 19.5K-byte ROM
- Max. CPU clock: 1.5MHz @ 4.5V
- Widely operating voltage: 2.4V - 5.5V @ 1.5MHz
- Built-in RC oscillator (only one resistor is needed)
- One 7-bit D/A for audio output or PWM audio output (mask option)
- Provides standby function
- Operating current (enable LVRST)
  PWM: 480μA (700KHz @ 4.5V)
  DAC: 720μA (700KHz @ 4.5V)
- Rather low standby current
  In standby mode: I_{STBY} < 1.0μA
- LCD matrix: 40 segments x 8 commons
  LCD bias: 1/4, 1/5
  LCD duty: 1/4, 1/8
- 2 tone channels and one noise channel for coding audio sound in
- 10 general I/O pins for key input

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG40 - 23 SEG22 - 1	18 - 1 64 - 43	O	LCD driver segment output
COM8 - 1	26 - 19	O	LCD driver common output
PA7 - 0	34 - 41	I/O	I/O port
PB1 - 0	32 - 33	I/O	I/O port
ROSC	42	I	R-osc input, connect to VDD through resistor
RESET	27	I	System reset input
AUDP	29	O	Current DAC audio output, or PWM audio output (Mask Option)
AUDN	31	O	PWM audio output
VDD	30	I	Power input
VSS	28	I	Ground input

4.1. Ordering Information

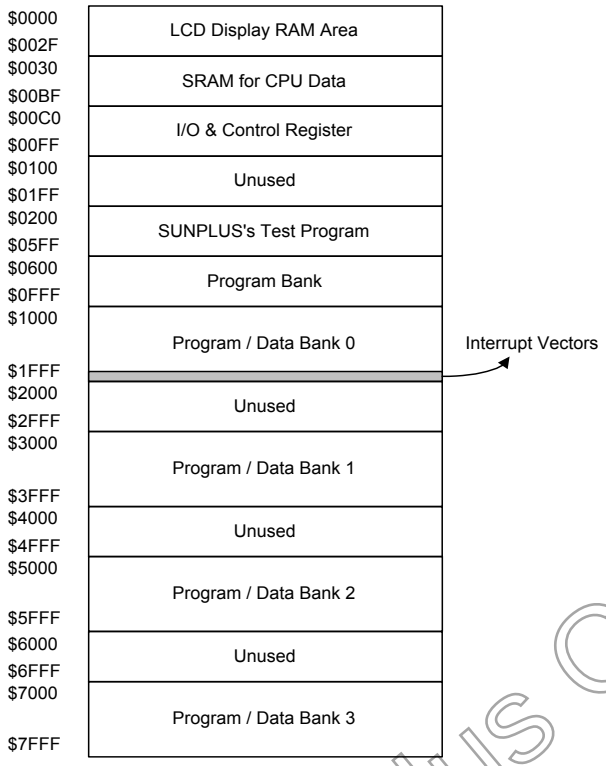
Product Number	Package Type
SPL02E2-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z, nn = 00 - 99); version (V = A - Z).

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area



To access ROM, users should program the BANK SELECT Register ($D7) first and then access the bank #1, #2, or bank #3 by addressing the higher bank to fetch data.

5.2. System Operation Mode (R/W)

The SPL02E2 provides normal mode and standby mode for user's options.

5.3. Interrupt (R/W)

The SPL02E2 provides three interrupt sources

1). 2Hz interrupt

2). Sound generator

3). Power key

5.4. Low Voltage Reset (LVRST)

The SPL02E2 provides a low voltage reset function. Once LVRST function is enabled (by mask option), the entire system will enter into RESET state if and only if the power supply voltage VDD is lower than 2.2V (typical).

5.5. I/O Port

5.5.1. IOA (R/W)

b7, 6, 5, 4 -nibble 1

b3, 2, 1, 0 -nibble 0

5.5.2. IOB (R/W)

b1, 0 -nibble 2

5.6. LCD Display Controller

There are total of 8 commons and 40 segments available in the SPL02E2. The 40-byte SRAM are allocated at $00-$2Fh for displaying LCD data.

5.7. Control Byte of I/O Port and LCD Duty Rate Port (W)

1). Set IOA, IOB as input status or output status

2). Set LCD duty

3). Set CPU clock rate: non-divided or divided-by-8

5.8. Tone and Noise

The SPL02E2 provides two tone-generator and one noise generator. Totally, 10 bits are used for programming the tone frequency, and two registers for controlling the amplitude of ToneA and ToneB. Two types of noise can be chosen and one register can be used to control the amplitude of noise.

5.9. Speech Play Control Port (W)

b0 = 0:non play mode

1:speech play mode

5.10. Speech Port (R/W)

In speech play mode, once data is written to the speech port, it is pumped to speaker through D/A or PWM (mask option) converter. The bit7 is a sign bit; '0' represents positive data and '1' represents negative data. The bit0 to bit5 are magnitude bits

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

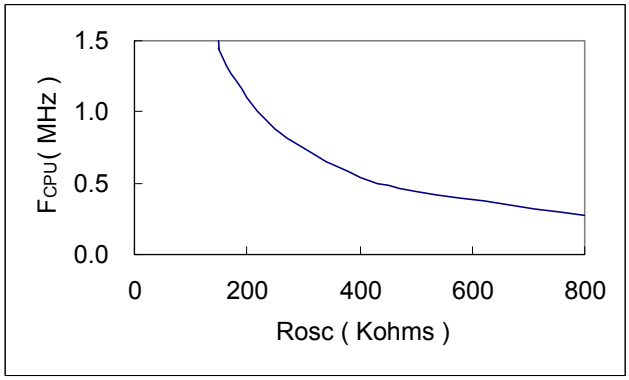
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery application
Operating Current	I_{OP}	-	380	-	µA	VDD = 3.0V, F_{CPU} = 700KHz
Standby Current	I_{STBY}	-	-	1.0	µA	VDD = 3.0V
Audio output current	I_{OH}	-	-35	-	mA	VDD = 3.0V, V_{OH} = 2.0V
	I_{OL}	-	40	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I	I_{OH}	-	-1.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I	I_{OL}	-	1.1	-	mA	VDD = 3.0V, V_{OL} = 0.8V

6.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

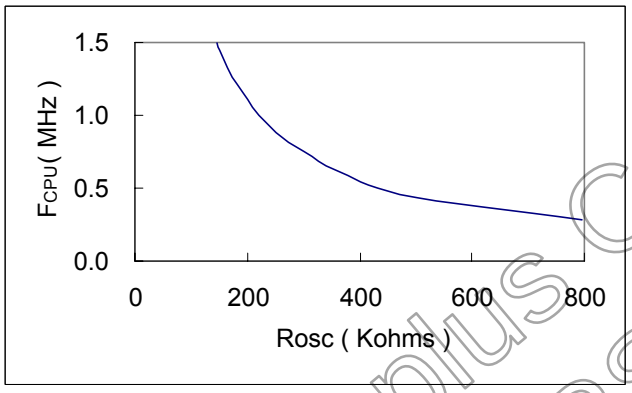
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery application
Operating Current	I_{OP}	-	720	-	µA	VDD = 4.5V, F_{CPU} = 700KHz
Standby Current	I_{STBY}	-	-	1.0	µA	VDD = 4.5V
Audio output current	I_{OH}		- 45	-	mA	VDD = 4.5V, V_{OH} = 3.5V
	I_{OL}	-	50	-	mA	VDD = 4.5V, V_{OL} = 0.8V
Input High Level	V_{IH}	2.4	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output High I	I_{OH}	-	-1.3	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I	I_{OL}	-	1.4	-	mA	VDD = 4.5V, V_{OL} = 0.8V

6.4. The Relationships between the R_{OSC} and the F_{OSC}

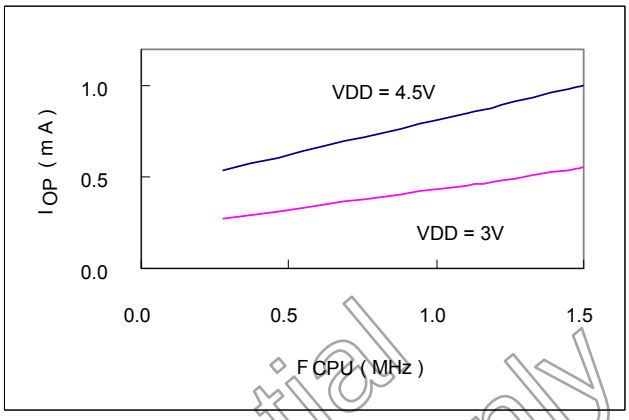
6.4.1. VDD = 3.0V, T_A = 25℃



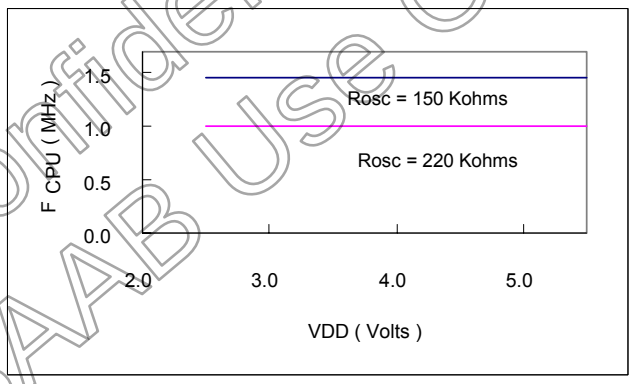
6.4.2. VDD = 4.5V, T_A = 25℃



6.5. The Relationships between the F_{CPU} and the I_{OP}

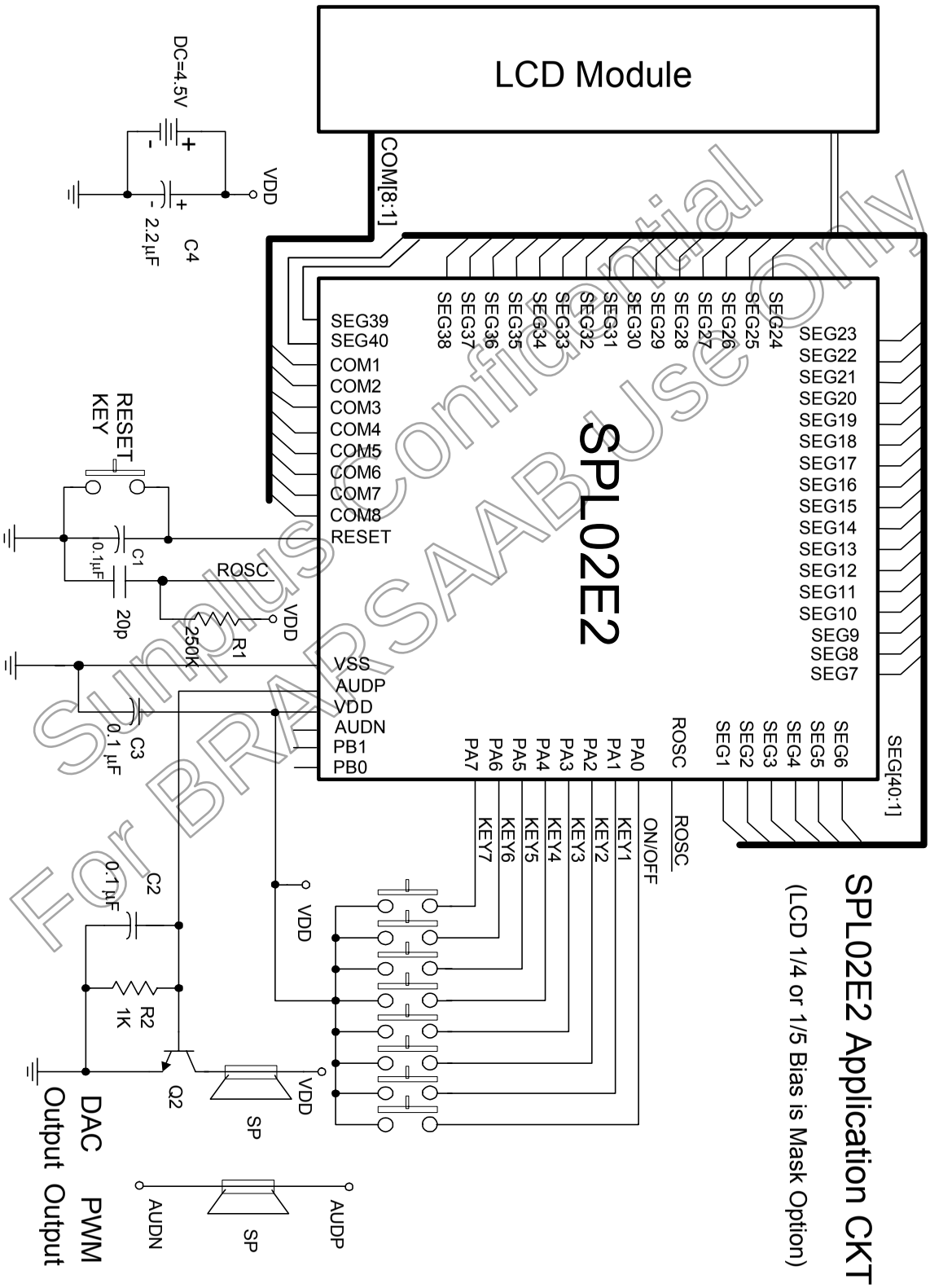


6.6. The Relationships between the F_{CPU} and the VDD



7. APPLICATION CIRCUITS

7.1. Application Circuit



7.2. Current Mode DAC Speaker Driver

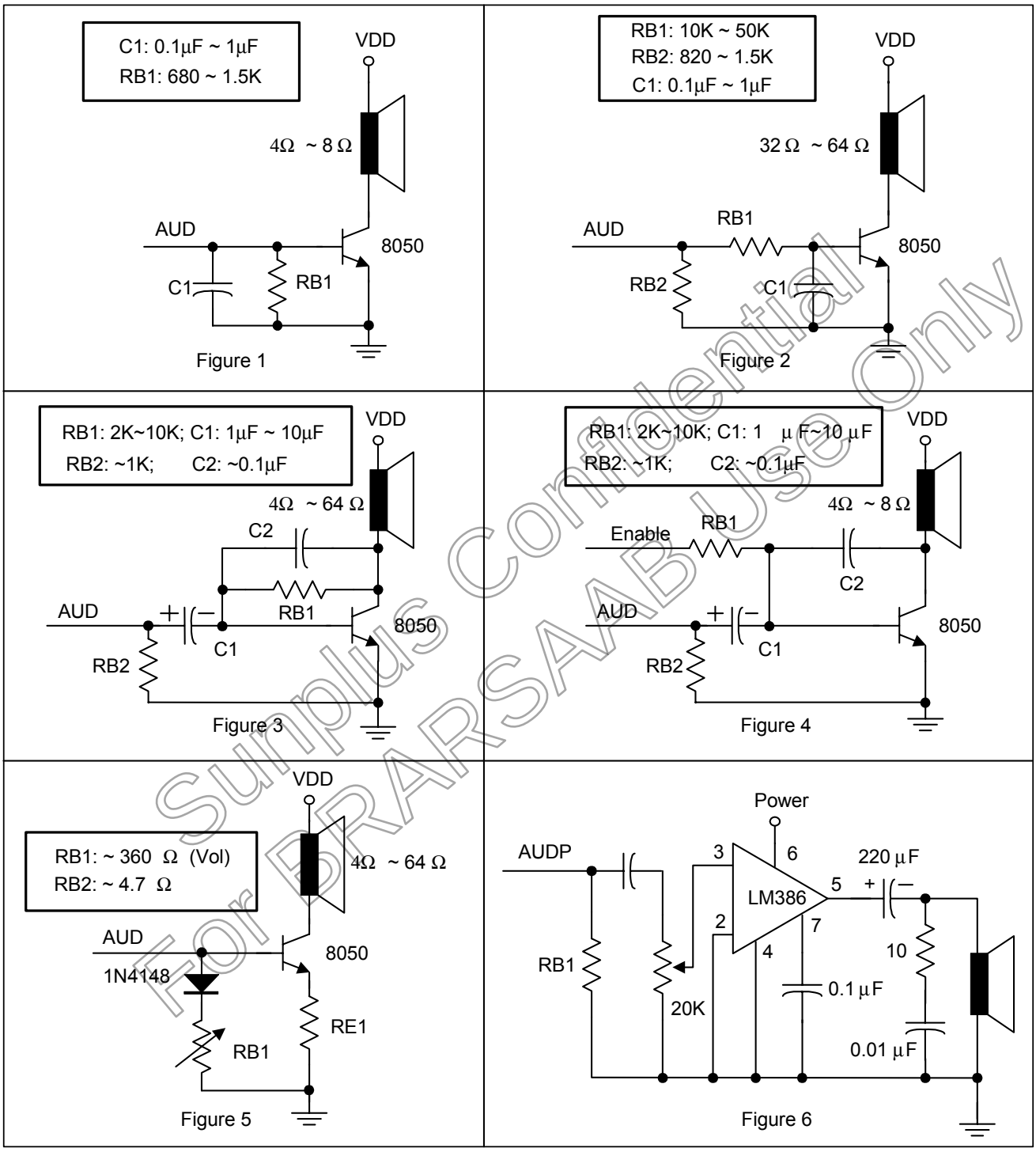


Figure 1: The simplest CKT uses a low impedance speaker. It has high operation current, but the cost is the cheapest.
Figure 2: It is the same as Figure 1 but a high impedance speaker is used.
Figure 3: The CKT contains a low pass filter. It is capable of providing higher speech quality, but it always takes higher operation current.
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.
Figure 5: The current mirror mode. It is able to control the volume. In addition, it is more stable and has lower operation current than Figure 1-3.
Figure 6: High quality, low operation current CKT, but more expensive.

8. PACKAGE/PAD LOCATIONS

Please contact Sunplus sales representatives for more information.

9. DISCLAIMER

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10. REVISION HISTORY

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