REALTEK

RTL8169SB(L)

INTEGRATED GIGABIT ETHERNET CONTROLLER (NIC)

DATASHEET

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USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8169SB(L) controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/11/17	First release.
1.1	2004/01/28	EEDI/AUX and EEDO description changed in Table 3, page 7. Pin 11 changed from NC to VSS (see Table 8, page 9). Pin 12 changed from NC to AVDDH (see Table 8, page 9).
1.2	2004/04/16	Add CardBus, Boot ROM function related content (see Table 1, page 4).
1.3	2004/07/09	Revised VDD25 parameters (see Table 12, page 26, and Table 15, page 27). Corrected 'VDD25' pin name to 'AVDDL'.
1.4	2004/07/26	Revised AVDDL parameters (see Table 12, page 26, and Table 15, page 27).
1.5	2004/08/10	Revised Pin 126 (VDD12A) description (see Table 8, page 9, Table 11, page 26, Table 12, page 26, and Table 15, page 27).

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8169SB(L) NIC Gigabit Ethernet controllers (RTL8169SB (128-QFP) & RTL8169SBL (128-LQFP)) combine a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, 32-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI v2.3 and CardBus (RTL8169SBL only) bus interfaces for host communications with power management, and comply with the IEEE 802.3 specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. They also support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

They support the Advanced Configuration Power management Interface (ACPI)--power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)--to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, the RTL8169SB(L) supports remote wake-up (including AMD Magic Packet, Re-LinkOk, and Microsoft® Wake-up frame) in both ACPI and APM (Advanced Power Management) environments. The LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. To support WOL from a deep power down state (e.g. D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8169SB(L).

The RTL8169SB(L) is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server. Also, the devices boost their PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving. To better qualify for server use, the RTL8169SB(L) support the PCI Dual Address Cycle (DAC) command when the assigned buffers reside at a physical memory address higher than 4 Gigabytes.

2. Features

- Integrated 10/100/1000 transceiver

- Auto-Negotiation with Next Page capability

- Supports PCI rev.2.3, 32-bit, 33/66MHz

- The RTL8169SBL supports CardBus mode. The CIS data can be stored in either EEPROM or expansion ROM

- Supports pair swap/polarity/skew correction

- Crossover Detection & Auto-Correction

- Wake-on-LAN and remote wake-up support

- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and largesend offload support

- Supports Full Duplex flow control (IEEE 802.3x)

- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

- Supports IEEE 802.1P Layer 2 Priority Encoding

- Supports IEEE 802.1Q VLAN tagging

- Serial EEPROM

- Supports up to 128Kbytes Boot ROM

- 3.3V signaling, 5V PCI I/O tolerant

- Transmit/Receive FIFO (8K/64K) support

- Supports power down/link down power saving

- Supports PCI Message Signaled Interrupt (MSI)

- 128-pin QFP package (RTL8169SB) and 128-pin LQFP package (RTL8169SBL)

3. System Applications

- Gigabit Ethernet Network Interface Card
- Gigabit Ethernet CardBus Card

4. Pin Assignments

20	AVDDL
21	VSSPST
22	GND
23	ISOLATEB
24	VDD12
25	INTAB
26	VDD33
27	PCIRSTB
28	PCICLK
29	GNTB
30	REQB
31	PMEB
32	VDD12
33	PCIAD31
34	PCIAD30
35	GND
36	PCIAD29
37	PCIAD28
38	VSSPST

19	MDI3-
18	MDI3+
17	VSS
16	AVDDL
15	MDI2-
14	MDI2+
13	VSS
12	AVDDH
11	VSS
10	AVDDH
9	VSS
8	CTRL25
7	AVDDL
6	MDI1-
5	MDI1+
4	VSS
3	AVDDL
2	MDI0-
1	MDI0+

39	PCIAD27
40	PCIAD26
41	VDD33
42	PCIAD25
43	PCIAD24
44	CBEB3
45	VDD12
46	IDSEL
47	PCIAD23
48	GND
49	PCIAD22
50	PCIAD21
51	VSSPST
52	GND
53	PCIAD20
54	VDD12
55	PCIAD19
56	VDD33
57	PCIAD18
58	PCIAD17
59	PCIAD16
60	CBEB2
61	FRAMEB
62	GND
63	IRDYB
64	VDD12

RTL8169SB(L)

128	VSS
127	RSET
126	VDD12A
125	CTRL12
124	VSS
123	VSS
122	XTAL2
121	XTAL1
120	AVDDH
119	VSSPST
118	GND
117	LED0
116	VDD12
115	LED1
114	LED2
113	LED3
112	GND
111	EESK
110	VDD12
109	EEDI
108	EEDO
107	VDD33
106	EECS
105	LANWAKE/CSTSCHG
104	PCIAD0
103	PCIAD1

65	CLKRUNB on SBL Version. NC on SB Ver.
66	VSSPST
67	TRDYB
68	DEVSELB
69	STOPB
70	PERRB
71	VDD33
72	NC
73	GND
74	NC
75	SERRB
76	PAR
77	CBEB1
78	VDD12
79	PCIAD15
80	GND
81	VSSPST
82	PCIAD14
83	PCIAD13

| 102	PCIAD2
101	VSSPST
100	GND
99	VDD12
98	PCIAD3
97	PCIAD4
96	PCIAD5
95	PCIAD6
94	VDD33
93	PCIAD7
92	CBEB0
91	VSSPST
90	PCIAD8
89	PCIAD9
88	M66EN
87	PCIAD10
86	PCIAD11
85	PCIAD12
84	VDD33

Figure 1.   RTL8169SB(L) 128-Pin (L)QFP Pin Assignments

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input.

O: Output.

T/S: Tri-State bi-directional input/output pin.

S/T/S: Sustained Tri-State.

O/D: Open Drain.

5.1. Power Management/Isolation

Table 1.   Power Management/Isolation

Symbol	Type	Pin No	Description
PMEB (PME#)	O/D	31	Power Management Event: Open drain, active low. Used to request a change in the current power management state and/or to indicate that a power management event has occurred.
ISOLATEB (ISOLATE#)	I	23	Isolate Pin: Active low. Used to isolate the RTL8169SB(L) from the PCI bus. The RTL8169SB(L) will not drive its PCI outputs (excluding PME#) and will not sample its PCI input (including PCIRSTB and PCICLK) as long as the Isolate pin is asserted.
LANWAKE/ CSTSCHG	O	105	LAN WAKE-UP Signal (When CardB_En=0, bit2 Config3): This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output that may be asserted from the LANWAKE pin (active high, active low, positive pulse, and negative pulse). We can configure the LANWAKE output via two CONFIG bits: LWACT(Config1.4) and LWPTN(Config4.2).

LWAKE Output		LWACT	
		0	1
LWPTN	0	Active high	Active low
	1	Positive pulse	Negative pulse

The default output is an active high signal. Once a PME event is received, the LANWAKE and PMEB assert at the same time when the LWPME (bit4, CONFIG4) is set to 0. If the LWPME is set to 1, the LANWAKE asserts only when PMEB asserts and ISOLATEB is low.

CSTSCHG Signal (When CardB_En=1, bit2 Config3):
This signal is used by the RTL8169SBL in CardBus applications only and is used to inform the motherboard to execute the wake-up process whenever a PME event occurs. This is always an active high signal, and the setting of LWACT (bit 4, Config1), LWPTN (bit2, Config4), and LWPME (bit4, Config4) is irrelevant in this case.

5.2. PCI Interface

Table 2. PCI Interface

Symbol	Type	Pin No	Description
PCIADPIN31-0	T/S	33, 34, 36, 37, 39, 40, 42, 43, 47, 49, 50, 53, 55, 57, 58, 59, 79, 82, 83, 85, 86, 87, 89, 90, 93, 95, 96, 97, 98, 102, 103, 104	AD31-0: Low 32-bit PCI address and data multiplexed pins. The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, it is a double-word address. The RTL8169SB(L) supports both big-endian and little-endian byte ordering. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted. PCIADPIN31-24 are shared with Boot ROM data pins, while PCIADPIN16-0 are shared with Boot ROM address pins.
CBEBPIN7-4	T/S		PCI bus command and Byte Enables multiplex pins. During the address phase of a transaction, CBEBPIN7-4 defines the bus command. During the data phase, CBEBPIN7-4 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBEBPIN4 applies to byte 4, and CBEBPIN7 applies to byte 7.
CBEBPIN3-0	T/S	44, 60, 77, 92	PCI bus command and Byte Enables multiplex pins. During the address phase of a transaction, CBEBPIN3-0 defines the bus command. During the data phase, CBEBPIN3-0 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBEBPIN0 applies to byte 0, and CBEBPIN3 applies to byte 3.
PCICLK	I	28	PCI clock: This clock input provides timing for all PCI transactions and is input to the PCI device. Supports up to a 66MHz PCI clock.
CLKRUNB on the RTL8169SBL NC on the RTL8169SB	I/O	65	Clock Run: On the RTL8169SB this pin is Not Connected. This signal is used by the RTL8169SBL to request starting (or speeding up) of the PCICLK clock. CLKRUNB also indicates the clock status. For the RTL8169SBL, CLKRUNB is an open drain output as well as an input. The RTL8169SBL requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.
DEVSELB	S/T/S	68	Device Select: As a bus master, the RTL8169SB(L) samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8169SB(L) asserts this signal low when it recognizes its target address after FRAMEB is asserted.
FRAMEB	S/T/S	61	Cycle Frame: As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is de-asserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.

Symbol	Type	Pin No	Description
GNTB	I	29	Grant: This signal is asserted low to indicate to the RTL8169SB(L) that the central arbiter has granted the ownership of the bus to the RTL8169SB(L). This input is used when the device is acting as a bus master.
REQB	T/S	30	Request: The RTL8169SB(L) will assert this signal low to request the ownership of the bus from the central arbiter.
IDSEL	I	46	Initialization Device Select: This pin allows the device to identify when configuration read/write transactions are intended for it.
INTAB	O/D	25	Interrupt A: Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask.
IRDYB	S/T/S	63	Initiator Ready: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the device is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	67	Target Ready: This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations, or is ready to provide the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK, when both IRDYB and TRDYB are asserted low.
PAR	T/S	76	Parity: This signal indicates even parity across PCIADPIN31-0 and CBEB3-0 including the PAR pin. PAR is stable and valid one clock after each address phase. For data phase, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
M66EN	I	88	66MHZ_ENABLE: This pin indicates to the device whether the bus segment is operating at 66 or 33MHz. When this pin (active high) is asserted, the current PCI bus segment that the device resides on operates in 66MHz mode. If this pin is de-asserted, the current PCI bus segment operates in 33MHz mode.
PERRB	S/T/S	70	Parity Error: This pin is used to report data parity errors during all PCI transactions except a Special Cycle. PERRB is driven active (low) two clocks after a data parity error is detected by the device receiving data, and the minimum duration of PERRB is one clock for each data phase with parity error detected.
SERRB	O/D	75	System Error: If an address parity error is detected and Configuration Space Status register bit 15 (detect parity error) is enabled, the device asserts the SERRB pin low and bit 14 of the Status register in Configuration Space.

Symbol	Type	Pin No	Description
STOPB	S/T/S	69	Stop: Indicates that the current target is requesting the master to stop the current transaction.
PCIRSTB	I	27	Reset: When PCIRSTB is asserted low, the device performs an internal system hardware reset. PCIRSTB must be held for a minimum period of 120ns.

5.3. EEPROM

Table 3.   EEPROM

Symbol	Type	Pin No	Description
EESK	O	111	Serial data clock.
EEDI/AUX	O/I	109	EEDI: Output to serial data input pin of EEPROM AUX: Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8169SB(L) assumes that no Aux. Power exists.
EEDO	I	108	Input from serial data output pin of EEPROM.
EECS/BROMCSB	O	106	EECS: EEPROM chip select. BROMCSB: This is the chip select signal of the Boot PROM.

5.4.   Transceiver Interface

Table 4.   Transceiver Interface

Symbol	Type	Pin No	Description
MDI[0]+	I/O	1	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[0]−	I/O	2	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+	I/O	5	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[1]−	I/O	6	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+	I/O	14	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDI[2]−	I/O	15	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+	I/O	18	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDI[3]−	I/O	19	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.5. Clock

Table 5.   Clock

Symbol	Type	Pin No	Description
Xtal1	I	121	Input of 25MHz clock reference.
Xtal2	O	122	Output of 25MHz clock reference.

5.6.   Regulator & Reference

Table 6.   Regulator & Reference

Symbol	Type	Pin No	Description
CTRL25	O	8	Regulator Control. Voltage control to external 2.5V regulator.
CTRL12	O	125	Regulator Control. Voltage control to external 1.2V regulator.
RSET	I	127	Reference. External Resistor Reference.

5.7.   LEDs

Table 7.   LEDs

Symbol	Type	Pin No	Description				
LED0	O	117	LEDS1-0	00	01	10	11
LED1	O	115	LED0	Tx/Rx	ACT(Tx/Rx)	Tx	LINK10/ ACT
LED2	O	114					
LED3	O	113	LED1	LINK100	LINK10/100/ 1000	LINK10/100 /1000	LINK100/ ACT
			LED2	LINK10	FULL	Rx	FULL
			LED3	LINK1000	-	FULL	LINK1000/ ACT

Note 1: LED0 is also BROMOEB to enable BROM's output buffer during BROM read operation.

Note 2: During power down mode, the LED signals are logic high.

Note 3: LEDS1-0's initial value comes from 93C46/93C56/93C66.

5.8. Power & Ground

Table 8.   Power & Ground

Symbol	Type	Pin No	Description
VDD12A	Power	126	Analog 1.2V power supply.
VDD12	Power	24, 32, 45, 54, 64, 78, 99, 110, 116	Digital 1.2V power supply.
VDD33	Power	26, 41, 56, 71, 84, 94, 107	Digital 3.3V power supply.
GND/VSSPST	Power	21, 22, 35, 38, 48, 51, 52, 62, 66, 73, 80, 81, 91, 100, 101, 112, 118, 119	Digital Ground.
AVDDL	Power	3, 7, 16, 20	Analog 2.5V power supply.
AVDDH	Power	10, 12, 120	Analog 3.3V power supply.
VSS	Power	4, 9, 11, 13, 17, 123, 124, 128	Analog Ground.

5.9.   NC (Not Connected) Pins

Table 9.   NC (Not Connected) Pins

Symbol	Type	Pin No	Description
NC		65	Not Connected on RTL8169SB. CLKRUNB on RTL8169SBL.
NC		72, 74	Not Connected.

6. Functional Description

6.1. PCI Bus Interface

The RTL8169SB(L) implements the PCI bus interface as defined in the PCI Local Bus Specifications Rev. 2.3. When internal registers are being accessed, the RTL8169SB(L) acts as a PCI target (slave mode). When accessing host memory for descriptor or packet data transfer, the RTL8169SB(L) acts as a PCI bus master.

All of the required pins and functions are implemented in the RTL8169SB(L) as well as the optional pin, INTAB for support of interrupt requests. The bus interface supports 32-bit and 66MHz operation in addition to the more common 32-bit and 33MHz capabilities. For more information, refer to the PCI Local Bus Specifications Rev. 2.3, March 29, 2002.

6.1.1. Byte Ordering

The RTL8169SB(L) can be configured to order the bytes of data on the PCI AD bus to conform to little-endian or big-endian ordering through the use of the ENDIAN bit of the C+ Command Register. When the RTL8169SB(L) is configured in big-endian mode, all the data in the data phase of either memory or I/O transaction to or from the RTL8169SB(L) is in big-endian mode. All data in the data phase of any PCI configuration transaction to RTL8169SB(L) should be little-endian, no matter whether the RTL8169SB(L) is set to big-endian or little-endian mode.

When configured for little-endian (ENDIAN bit=0), the byte orientation for receive and transmit data and descriptors in system memory is as follows:

31 ~ 24	23 ~ 16	15 ~ 8	7 ~ 0
Byte 3	Byte 2	Byte 1	Byte 0
C/BE[3] (MSB)	C/BE[2]	C/BE[1]	C/BE[0] (LSB)

Figure 2.   Little-Endian Byte Ordering

When configured for big-endian mode (ENDIAN bit=1), the byte orientation for receive and transmit data and descriptors in system memory is as follows:

31 ~ 24	23 ~ 16	15 ~ 8	7 ~ 0
Byte 0	Byte 1	Byte 2	Byte 3
C/BE[3] (LSB)	C/BE[2]	C/BE[1]	C/BE[0] (MSB)

Figure 3.   Big-Endian Byte Ordering

6.1.2.   Interrupt Control

Interrupts are performed by asynchronously asserting the INTAB pin. This pin is an open drain output. The source of the interrupt can be determined by reading the Interrupt Status Register (ISR). One or more bits in the ISR will be set, denoting all currently pending interrupts. Writing 1 to any bit in the ISR register clears that bit. Masking of specific interrupts can be accomplished by using the Interrupt Mask Register (IMR). Assertion of INTAB can be prevented by clearing the Interrupt Enable bit in the Interrupt Mask Register. This allows the system to defer interrupt processing as needed.

6.1.3.   Latency Timer

The PCI Latency Timer described in LTR defines the maximum number of bus clocks that the device will hold the bus. Once the device gains control of the bus and issues FRAMEB, the Latency Timer will begin counting down. The LTR register specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8169SB(L). When the RTL8169SB(L) asserts FRAMEB, it enables its latency timer to count. If the RTL8169SB(L) deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8169SB(L) initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write to LTR, and the default value is 00H.

6.1.4.   64-Bit Addressing

The RTL8169SB(L) supports 64-bit addressing (Dual Address Cycle) as a bus master for transferring descriptor and packet data information. Dual Address Cycle (DAC) mode can be enabled or disabled through software. The RTL8169SB(L) only supports 32-bit addressing as a target.

6.2. PCI Bus Operation

6.2.1. Target Read

A Target Read operation starts with the system generating FRAMEB, Address, and either an IO read (0010b) or Memory Read (0110b) command. If the 32-bit address on the address bus matches the IO address range specified in IOAR (for I/O reads) or the memory address range specified in MEM (for memory reads), the RTL8169SB(L) will generate DEVSELB 2 clock cycles later (medium speed). The system must tri-state the address bus, and convert the C/BE bus to byte enables after the address cycle. On the 2nd cycle after the assertion of DEVSELB, all 32-bits of data and TRDYB will become valid. If IRDYB is asserted at that time, TRDYB will be forced HIGH on the next clock for 1 cycle, and then tri-stated.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8169SB(L) will still make data available as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.
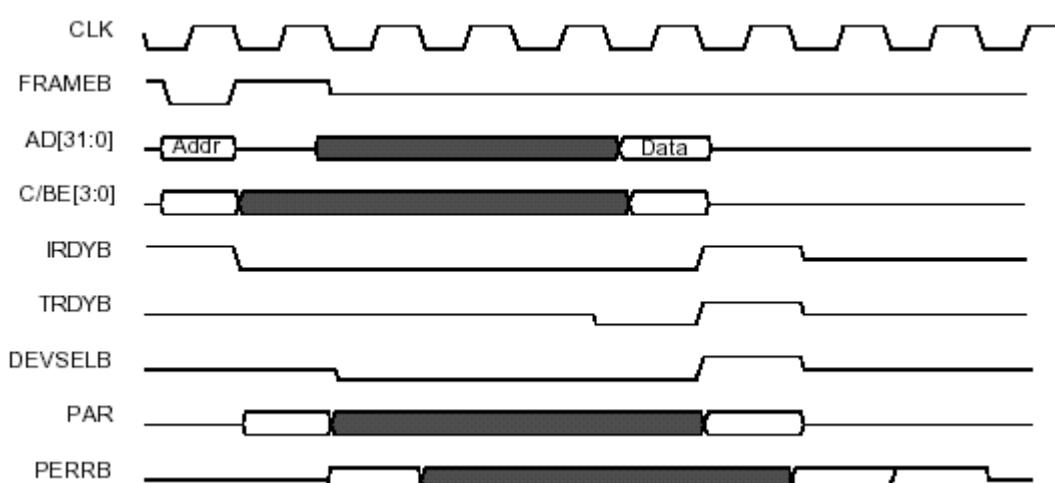
Figure 4.   Target Read Operation

6.2.2. Target Write

A Target Write operation starts with the system generating FRAMEB, Address, and Command (0011b or 0111b). If the upper 24 bits on the address bus match IOAR (for I/O reads) or MEM (for memory reads), the RTL8169SB(L) will generate DEVSELB 2 clock cycles later. On the 2nd cycle after the assertion of DEVSELB, the device will monitor the IRDYB signal. If IRDYB is asserted at that time, the RTL8169SB(L) will assert TRDYB. On the next clock the 32-bit double word will be latched in, and TRDYB will be forced HIGH for 1 cycle and then tri-stated. Target write operations must be 32-bits wide.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8169SB(L) will still latch the first double word as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.
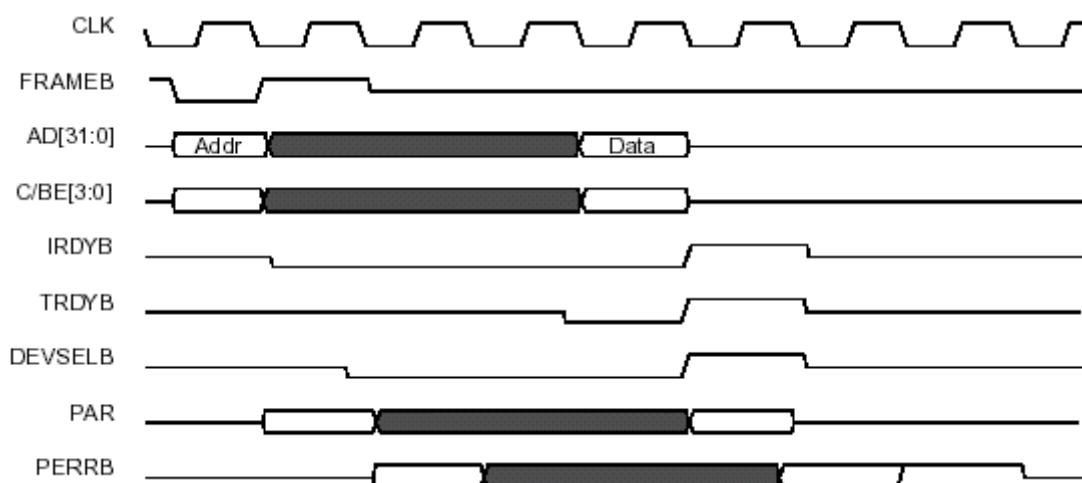

Figure 5.   Target Write Operation

6.2.3. Master Read

A Master Read operation starts with the RTL8169SB(L) asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a master abort by asserting FRAMEB HIGH for 1 cycle, and IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the address bus will become tri-state, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, data will be latched in (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last read cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It too will be tri-stated 1 cycle later. This will conclude the read operation. The RTL8169SB(L) will never force a wait state during a read operation.
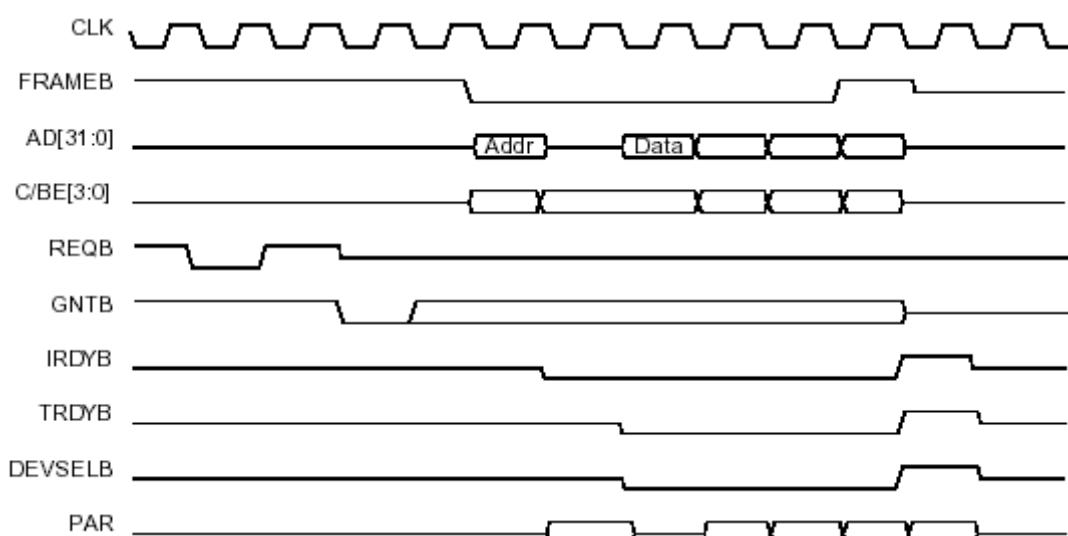
**Figure 6.   Master Read Operation**

6.2.4. Master Write

A Master Write operation starts with the RTL8169SB(L) asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a Master Abort by asserting FRAMEB HIGH for 1 cycle. IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the data bus will become valid, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, valid data for the next cycle will become available (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last write cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It too will be tri-stated 1 cycle later. This will conclude the write operation. The RTL8169SB(L) will never force a wait state during a write operation.
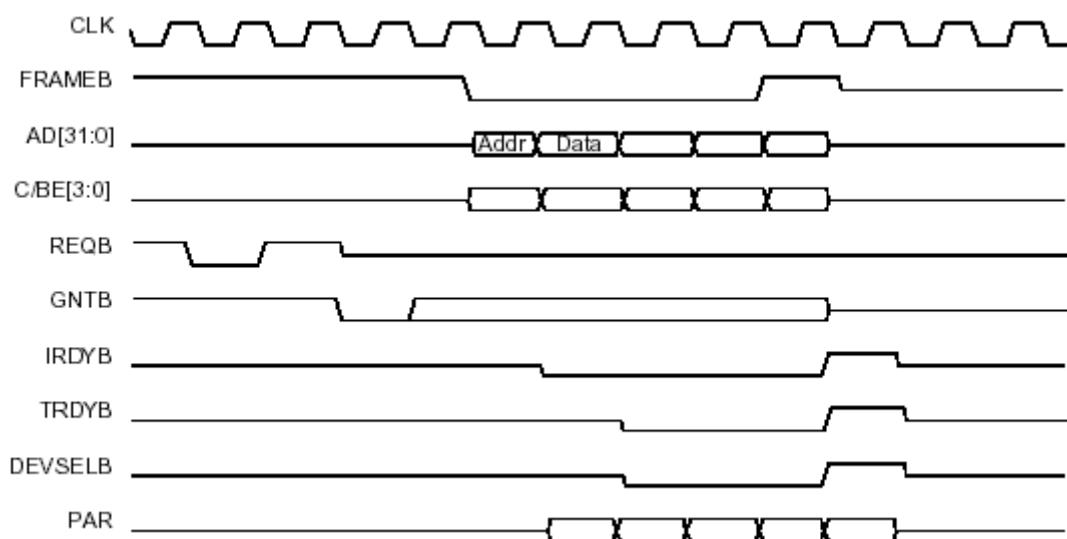
Figure 7.   Master Write Operation

6.2.5. Configuration Access

Configuration register accesses are similar to target reads and writes in that they are single data word transfers and are initiated by the system. For the system to initiate a Configuration access, it must also generate IDSEL as well as the correct Command (1010b or 1011b) during the Address phase. The RTL8169SB(L) will respond as it does during Target operations. Configuration reads must be 32-bits wide, but writes may access individual bytes.

6.3. LED Functions

The RTL8169SB(L) supports 4 LED signals in 4 different configurable operation modes. The following sections describe the different LED actions.

6.3.1. Link Monitor

The Link Monitor senses the link integrity or if a station is down, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.3.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.
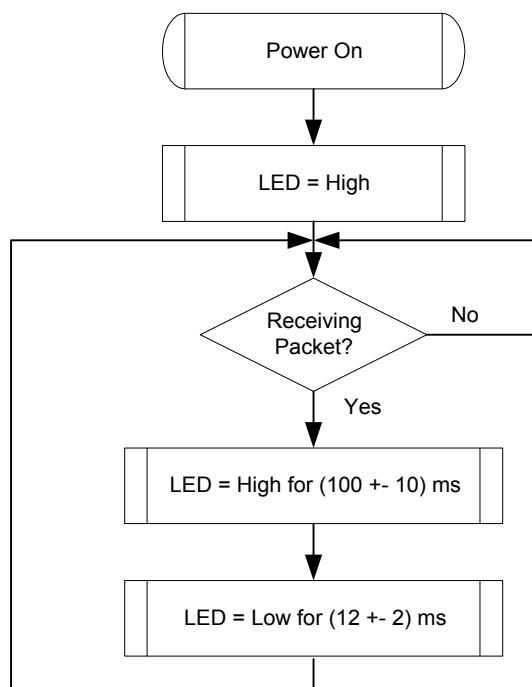
Figure 8.   Rx LED

6.3.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.
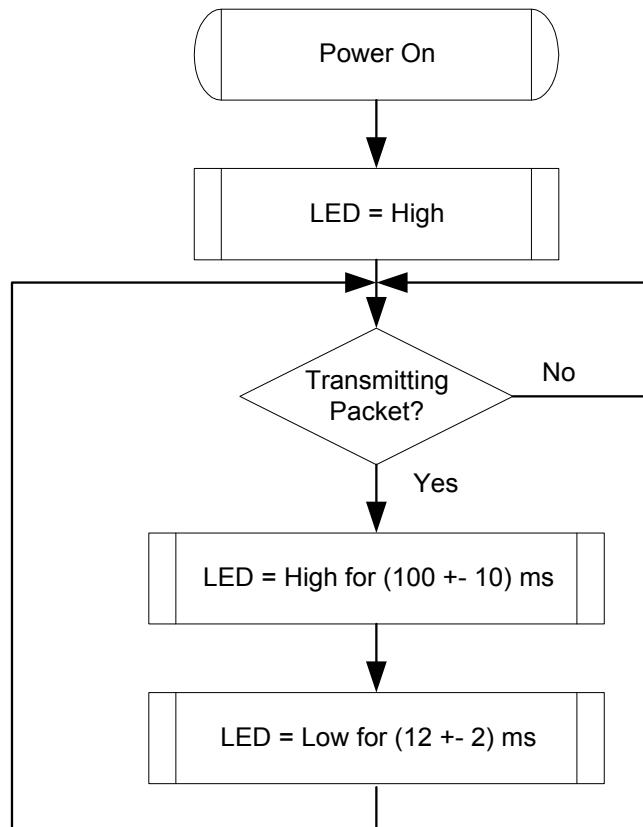
Figure 9.   Tx LED

6.3.4. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.
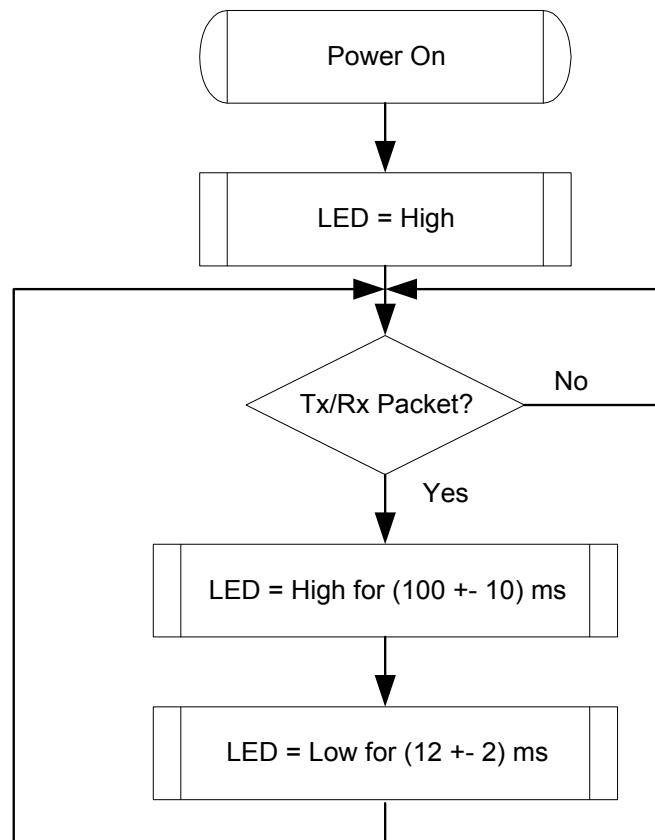
Figure 10. Tx/Rx LED

6.3.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8169SB(L) is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.
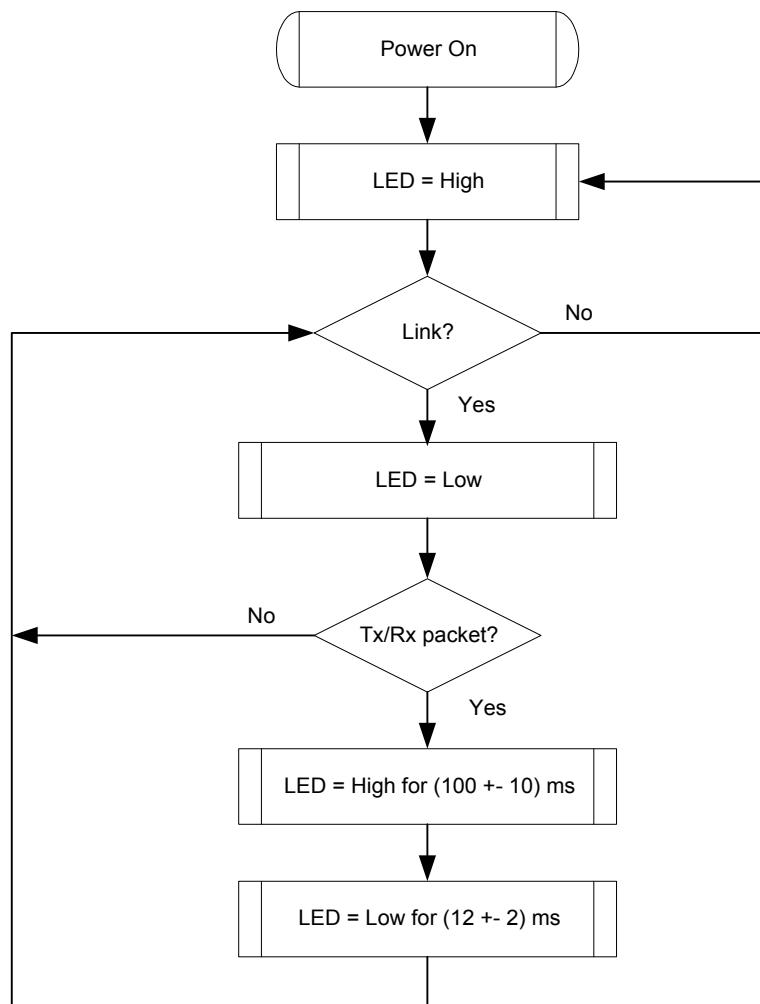
Figure 11. LINK/ACT LED

6.4. PHY Transceiver

6.4.1. PHY Transmitter

In 10Mbps mode, the Tx MAC retrieves packet data from the Tx Buffer Manager and sends it out through the transmitting physical layer interface. The transmit 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. Then, the 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the DAC converter.

In 100Mbps mode, the transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code via 4B/5B coding technology, scrambling, and serializing before being converted to 125MHz NRZ and NRZI signals. After that, the NRZI signal is passed to the MLT-3 encoder, then to the DAC converter for transmission onto the media.

In 1000Mbps mode, the RTL8169SB(L)'s PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. Then those code groups are passed through a waveform shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a DAC.

6.4.2. PHY Receiver

In MII (10Mbps) mode, the received differential signal is converted into a Manchester-encoded data stream. The stream is processed with a Manchester decoder, and is de-serialized into 4-bit wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz. In 100Mbps mode, the MLT-3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT-3 and NRZI decoder, descrambler, 4B/5B decoder, and then is presented to the MII interface in 4-bit wide nibbles at a clock speed of 25MHz.

In GMII mode, the input signal from the media first passes through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then the 8-bit wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

6.5. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.6. EEPROM Interface

The RTL8169SB(L) requires the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM, the 93C66 is a 4K-bit EEPROM). The EEPROM interface provides the ability for the RTL8169SB(L) to read from and write data to an external serial EEPROM device.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8169SB(L) will auto-load values from the EEPROM. If the EEPROM is not present, the RTL8169SB(L) initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD. The interface consists of EESK, EECS, EEDO, and EEDI.

Table 10. EEPROM Interface

EEPROM	Description
EECS	93C46 (93C56/93C66) chip select.
EESK	EEPROM serial data clock.
EEDI/Aux	Input data bus/Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to Boot PROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8169SB(L) assumes that no Aux. Power exists.
EEDO	Output data bus

6.7. Power Management

The RTL8169SB(L) is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-Directed Power Management (OSPM) environment.

The RTL8169SB(L) can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via PME# when such a packet or event occurs. Then, the whole system can be restored to a normal state to process incoming jobs.

When the RTL8169SB(L) is in power down mode (D1 ~ D3):

- The Rx state machine is stopped, and the RTL8169SB(L) monitors the network for wakeup events such as a Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8169SB(L) will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO buffer.

- The FIFO status and packets that have already been received into the Rx FIFO before entering power down mode are held by the RTL8169SB(L).

- Transmission is stopped. PCI bus master mode is stopped. The Tx FIFO buffer is held.

- After restoration to a D0 state, the RTL8169SB(L) transfers data that was not moved into the Tx FIFO buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power (bit15, PMC) = 1.

If EEPROM D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0's.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 F7, then PCI PMC = C2 F7)

- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C2 F7, then PCI PMC = 02 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C2 F7 (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 77, then PCI PMC = C2 77)

- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C2 77, then PCI PMC = 02 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8169SB(L), e.g. a broadcast, multicast, or unicast packet addressed to the current RTL8169SB(L) adapter.

- The received Magic Packet does not contain a CRC error.

- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.

- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid (Fast) Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8169SB(L), e.g. a broadcast, multicast, or unicast address to the current RTL8169SB(L) adapter.

- The received Wakeup Frame does not contain a CRC error.

- The PMEn bit (CONFIG1#0) is set to 1.

- The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC* of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8169SB(L) is configured to allow direct packet wakeup, e.g. a broadcast, multicast, or unicast network packet.

16-bit CRC: The RTL8169SB(L) supports two normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and three long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The PME# signal is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8169SB(L) may assert PME# in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8169SB(L) to stop asserting a PME# (if enabled).

When the device is in power down mode, e.g. D1-D3, the IO, MEM, and Boot ROM spaces are all disabled. After a RST# assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required. The RTL8169SB(L) also supports the legacy LAN WAKE-UP function. The LWAKE pin is used to notify legacy motherboards to execute the wake-up process whenever the device receives a wakeup event, such as Magic Packet.

The LWAKE signal is asserted according to the following settings:

1. LWPME bit (bit4, CONFIG4):

- LWAKE can only be asserted when PMEB is asserted and ISOLATEB is low.
- LWAKE is asserted whenever a wakeup event occurs.

2. Bit1 of DELAY byte (offset 1Fh, EEPROM):

- LWAKE signal is enabled.
- LWAKE signal is disabled.

7. Characteristics

7.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 11.   Absolute Maximum Ratings

Description/Symbol	Minimum	Maximum	Unit
Supply Voltage (VDD33, AVDDH)	-0.5	4	V
Supply Voltage (AVDDL)	-0.5	3	V
Supply Voltage (VDD12, VDD12A)	-0.5	1.5	V
Input Voltage (DCinput)	-0.5	VDD33 + 0.5	V
Output Voltage (DCoutput)	-0.5	VDD33 + 0.5	V
Storage Temperature	-55	+125	°C

7.2. Recommended Operating Conditions

Table 12.   Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD33, AVDDH	3.0	3.3	3.6	V
	AVDDL	2. 32	2.5	2.67	V
	VDD12, VDD12A	1.13	1.2	1.28	V
Ambient Temperature T_A		0		70	°C
Maximum Junction Temperature				125	°C

7.3. Crystal Requirements

Table 13.   Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.		25		MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a=25°C.	-50		+50	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a=-20°C ~+70°C.	-30		+30	ppm

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref} Duty Cycle	Reference clock input duty cycle	40		60	%
C_L	Load Capacitance			27	pF
ESR	Equivalent Series Resistance			10	Ω
DL	Drive Level			0.5	mW

7.4. Thermal Characteristics

Table 14.   Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	°C
Operating temperature	0	70	°C

7.5. DC Characteristics

Table 15.   DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage		3.0	3.3	3.6	V
AVDDL	2.5V Supply Voltage		2.32	2.5	2.67	V
VDD12, VDD12A	1.2V Supply Voltage		1.13	1.2	1.28	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -8mA	0.9 * VDD33		VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 8mA			0.1 * VDD33	V
V_{ih}	Minimum High Level Input Voltage		0.5 * VDD33		VDD33+0.5	V
V_{il}	Maximum Low Level Input Voltage		-0.5		0.3 * VDD33	V
I_{in}	Input Current	V_{in} =VDD33 or GND	-1.0		1.0	uA
I_{oz}	Tri-State Output Leakage Current	V_{out} =VDD33 or GND	-10		10	uA
Icc33	Average Operating Supply Current from 3.3V			TBD		mA
$I_{cc}12$	Average Operating Supply Current from 1.2V			TBD		mA

7.6. AC Characteristics

7.6.1. Serial EEPROM Interface Timing

93C46(64*16)/93C56(128*16)/93C66(256*16)
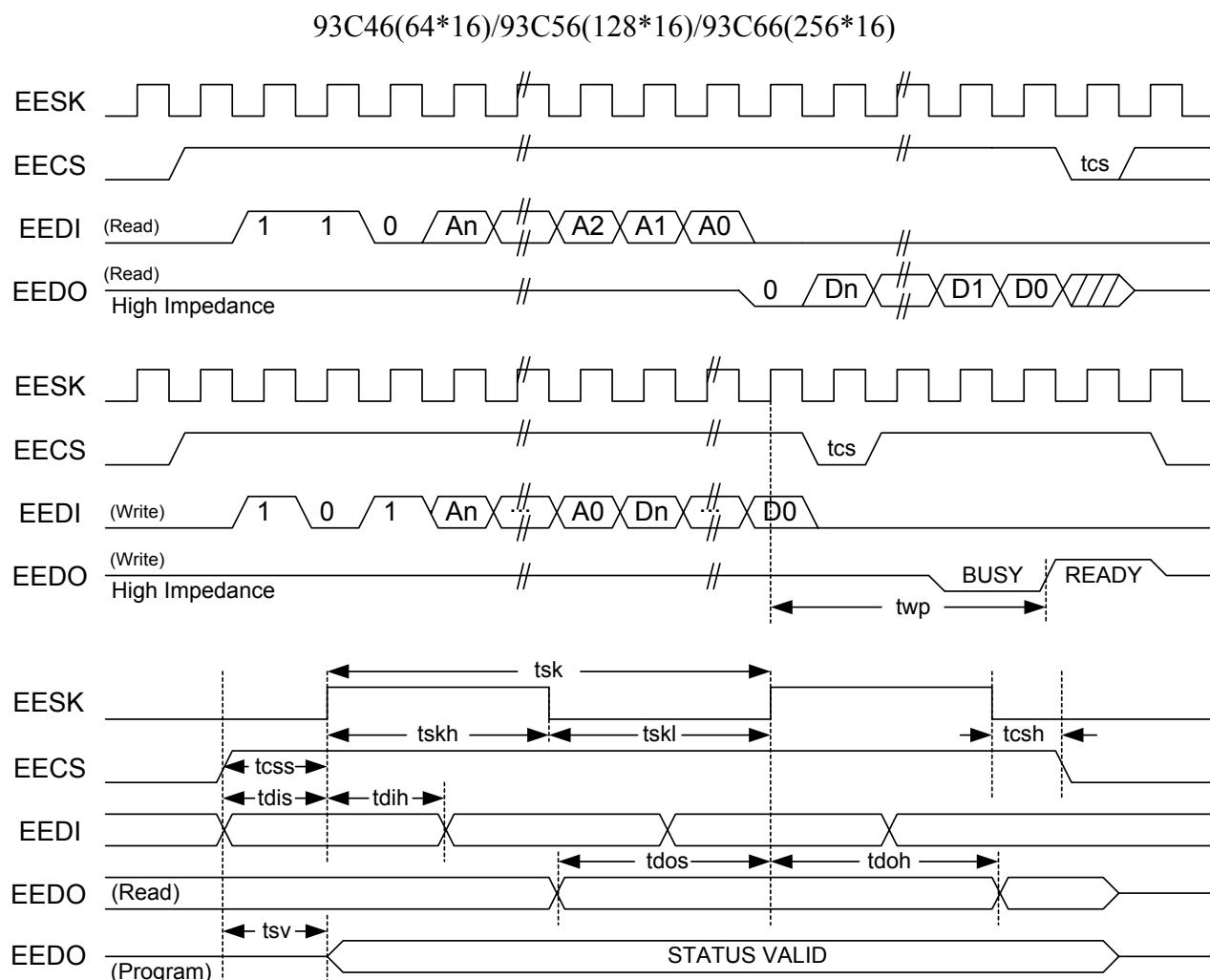
Figure 12.   Serial EEPROM Interface Timing

Table 16.   EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346/9356(9366)	1000/250		ns
twp	Write Cycle Time	9346/9356(9366)		10/10	ms
tsk	SK Clock Cycle Time	9346/9356(9366)	4/1		µs
tskh	SK High Time	9346/9356(9366)	1000/500		ns
tskl	SK Low Time	9346/9356(9366)	1000/250		ns

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcss	CS Setup Time	9346/9356(9366)	200/50		ns
tcsh	CS Hold Time	9346/9356(9366)	0/0		ns
tdis	DI Setup Time	9346/9356(9366)	400/50		ns
tdih	DI Hold Time	9346/9356(9366)	400/100		ns
tdos	DO Setup Time	9346/9356(9366)	2000/500		ns
tdoh	DO Hold Time	9346/9356(9366)		2000/500	ns
tsv	CS to Status Valid	9346/9356(9366)		1000/500	ns

7.7. PCI Bus Operation Timing

7.7.1.   PCI Bus Timing Parameters

Table 17.   PCI Bus Timing Parameters

Symbol	Parameter	66MHz		33MHz		Parameter
		Min	Max	Min	Symbol	
T val	CLK to Signal Valid Delay-bused signals	2	6	2	11	ns
T val(ptp)	CLK to Signal Valid Delay-point to point	2	6	2	12	ns
T on	Float to Active Delay	2		2		ns
T off	Active to Float Delay		14		28	ns
T su	Input Setup Time to CLK-bused signals	3		7		ns
T su(ptp)	Input Setup Time to CLK-point to point	5		10		ns
T h	Input Hold Time from CLK	0		0		ns
T rst	Reset active time after power stable	1		1		ms
T rst-clk	Reset active time after CLK STABLE	100		100		μs
T rst-off	Reset Active to Output Float delay		40		40	ns
T rhfa	RSTB High to First configuration Access	2^25		2^25		clocks
T rhff	RSTB High to First FRAMEB assertion	5		5		clocks
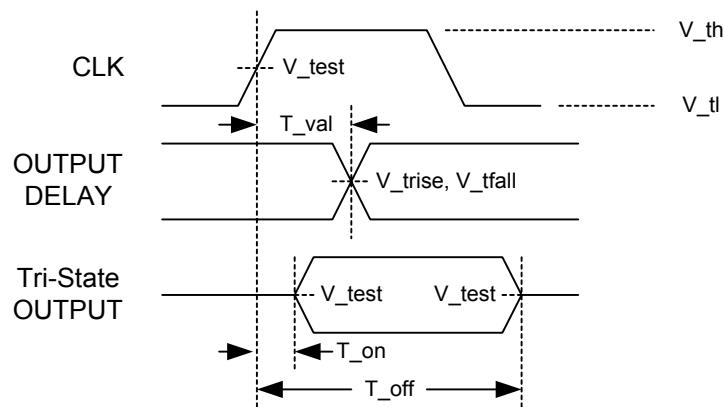
Figure 13.   Output Timing Measurement Conditions
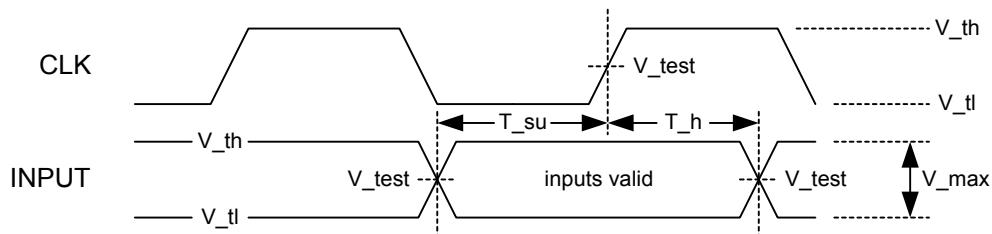

Figure 14.   Input Timing Measurement Conditions

Table 18.   Measurement Condition Parameters

Symbol	Level	Units
Vth	0.6Vcc	V
Vtf	0.2Vcc	V
Vtest	0.4Vcc	V
Vtrise	0.285Vcc	V
Vtfall	0.615Vcc	V
Vmax	0.4Vcc	V
Input Signal Edge Rate	1	V/ns

7.7.2. PCI Clock Specification
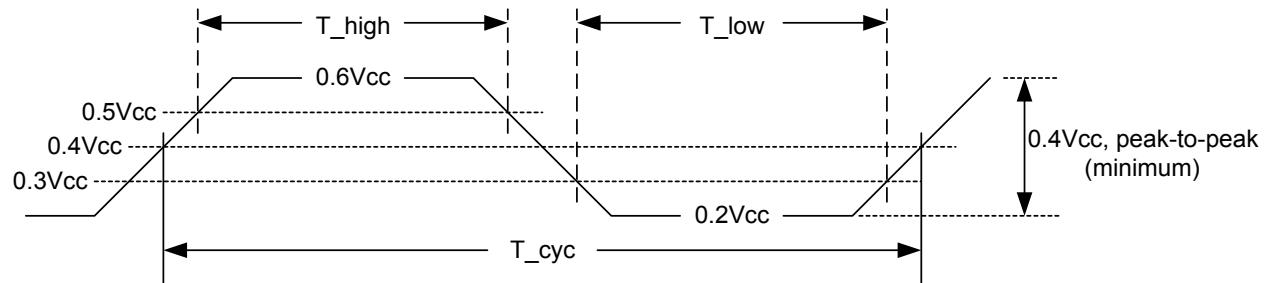
Figure 15. 3.3V Clock Waveform
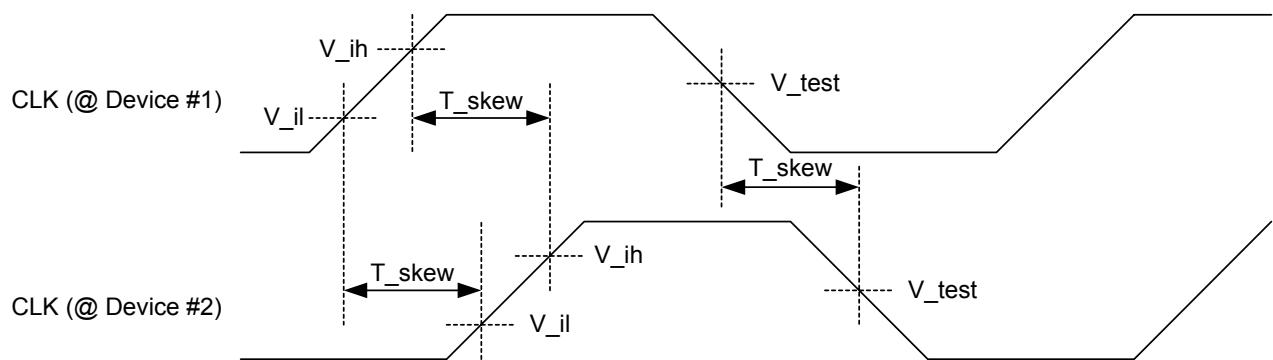
Figure 16. Clock Skew Diagram

Table 19.   Clock and Reset Specifications

		66MHz		33MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Symbol**	**Parameter**
Tcyc	CLK Cycle Time	15	30	30	∞	ns
Thigh	CLK High Time	6		11		ns
Tlow	CLK Low Time	6		11		ns
--	CLK Slew Rate	1.5	4	1	4	V/ns
--	RST# Slew Rate	50	-	50	-	mV/ns
Tskew	CLK Skew		1		2	ns

RTL8169SB(L)
Datasheet

7.7.3. PCI Transactions
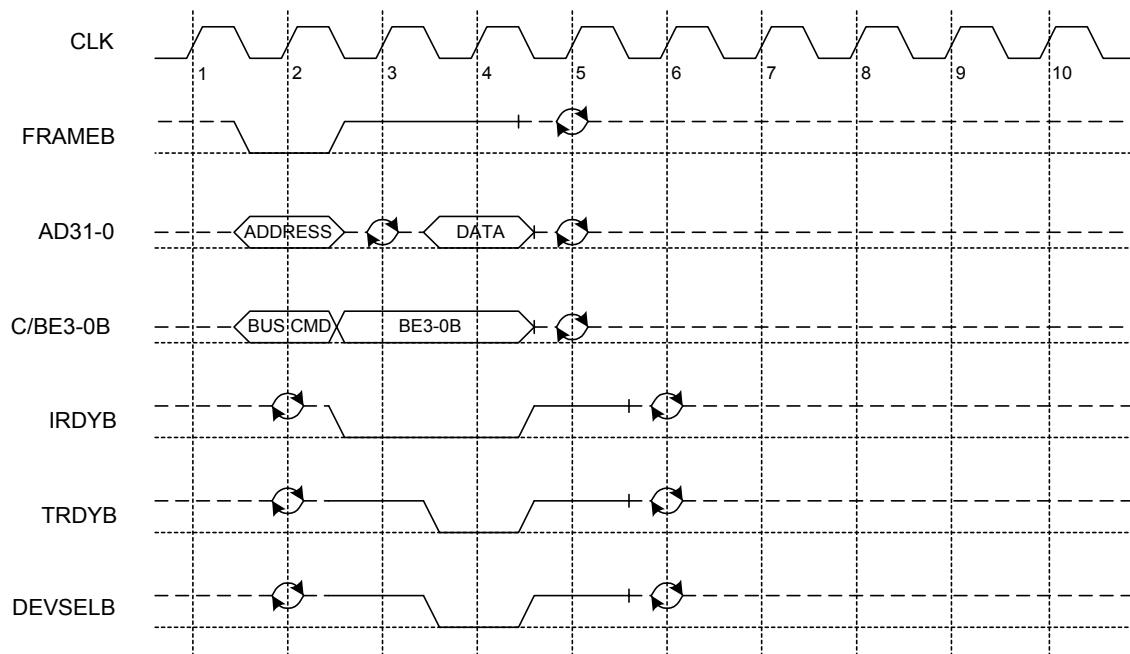
Figure 17.   I/O Read
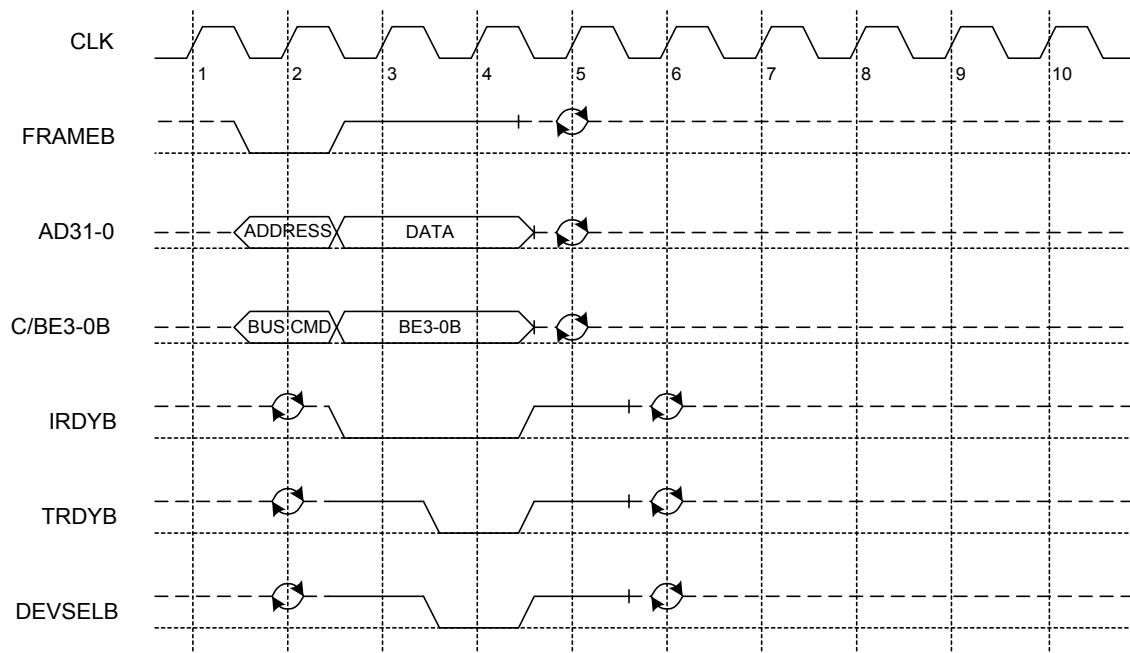
Figure 18.   I/O Write
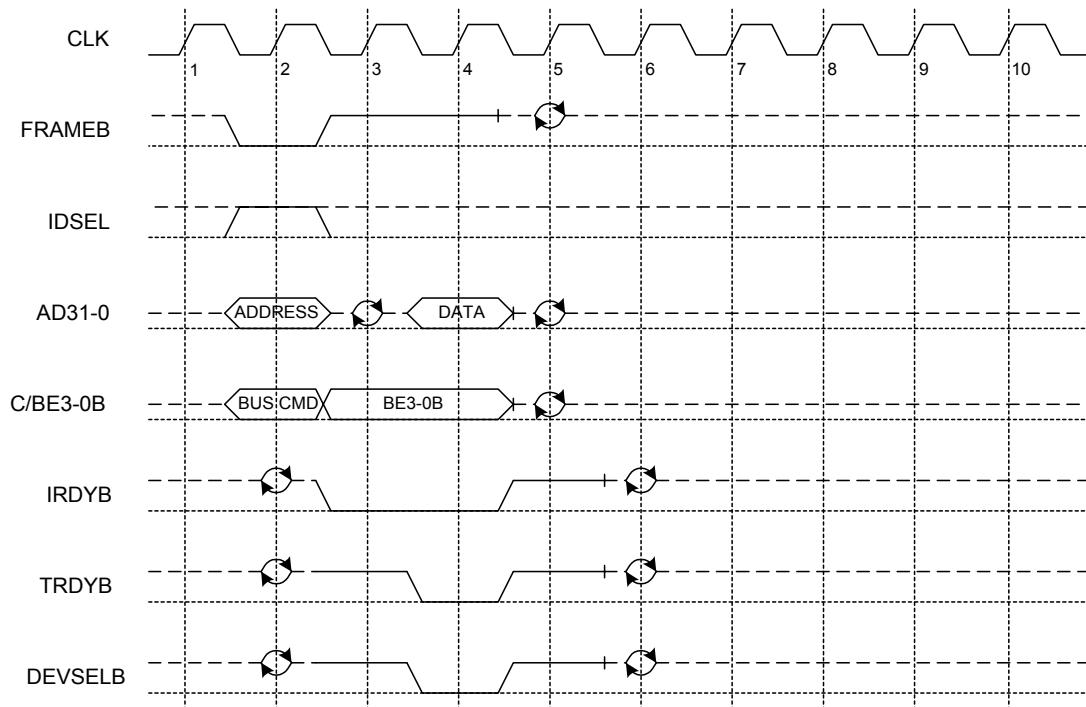
**Figure 19.   Configuration Read**
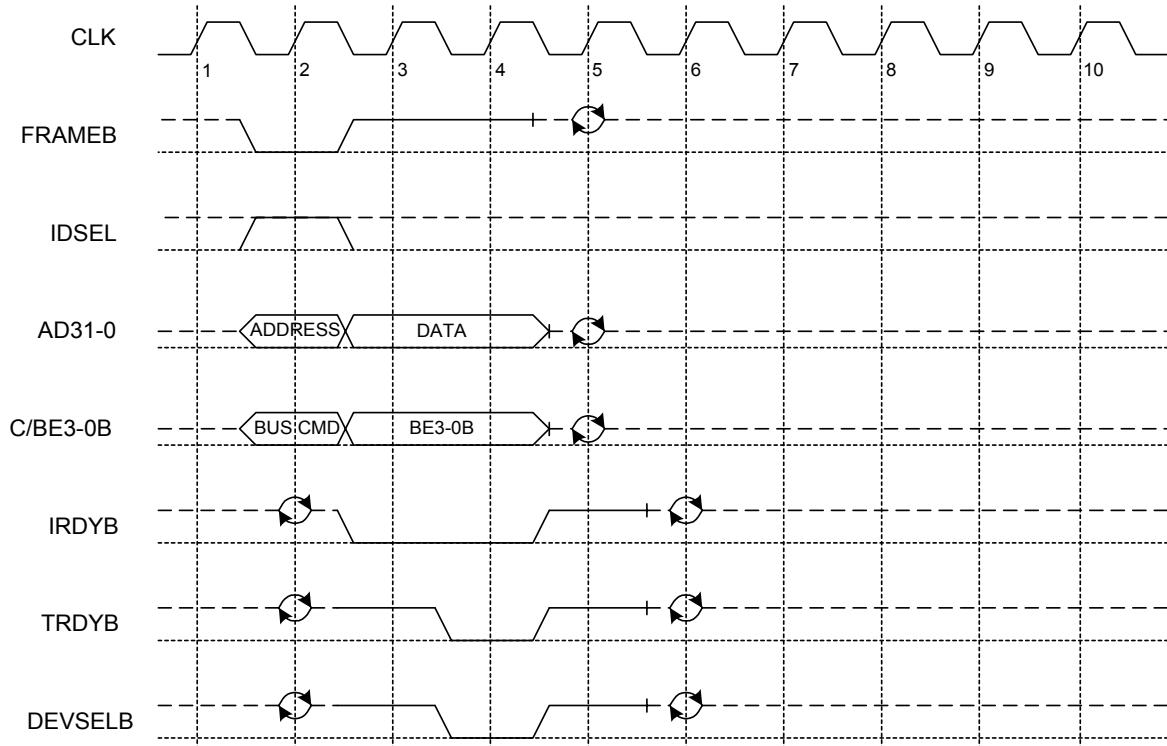
Figure 20.   Configuration Write
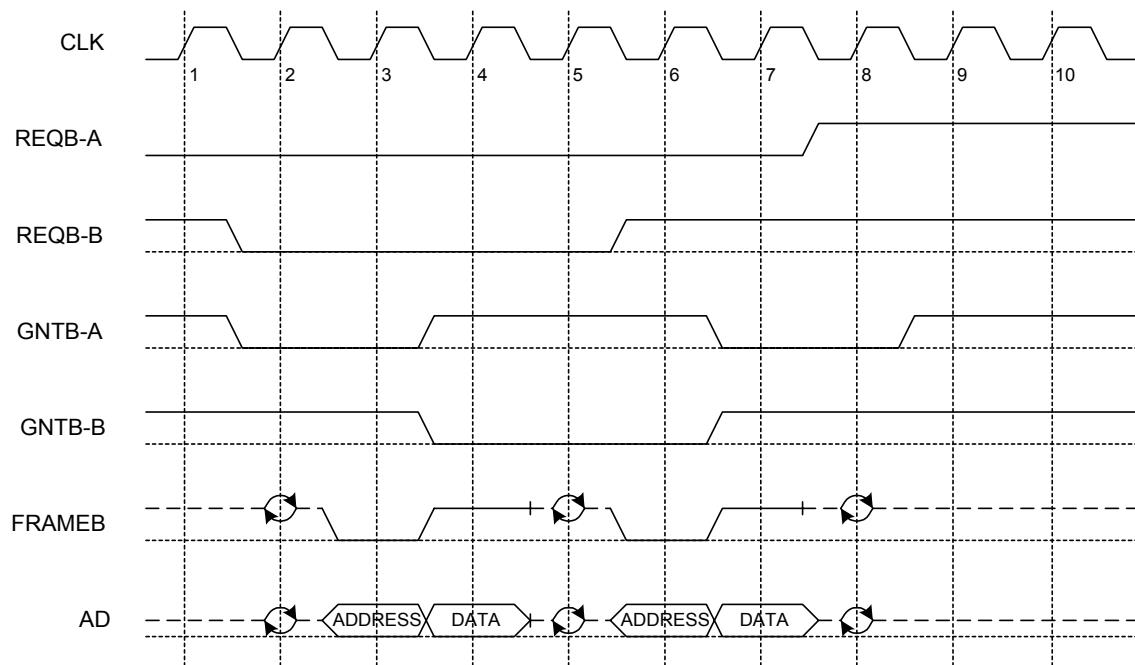
Figure 21.   Bus Arbitration
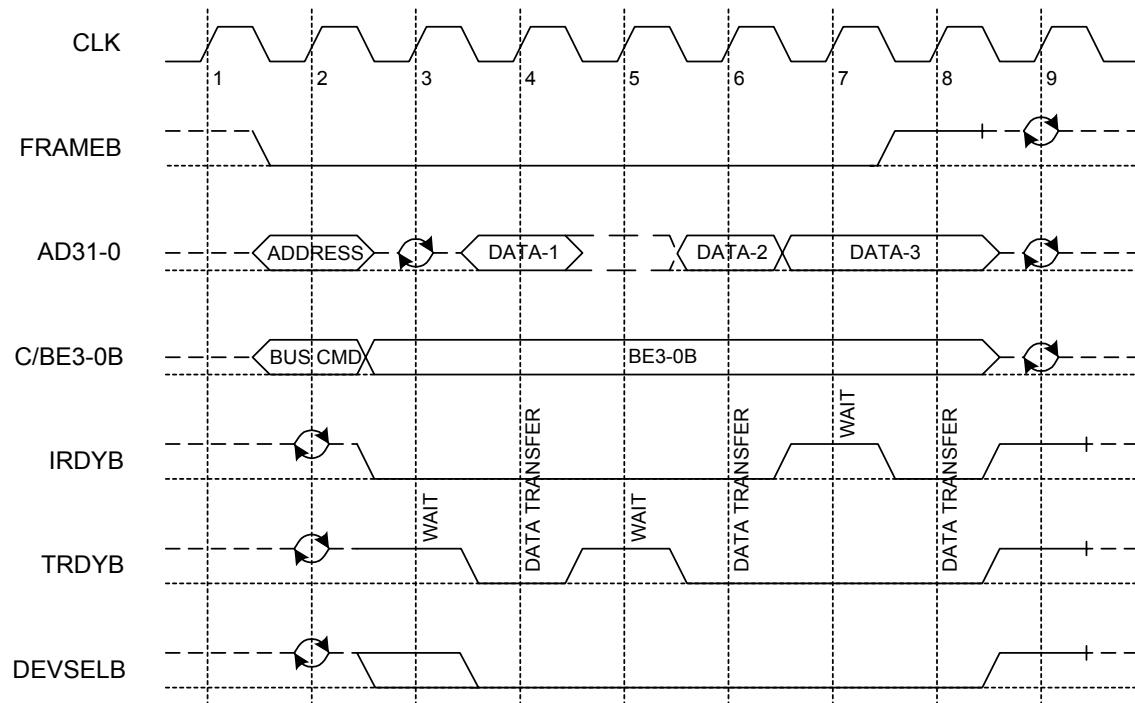

**Figure 22.   Memory Read Below 4GB**
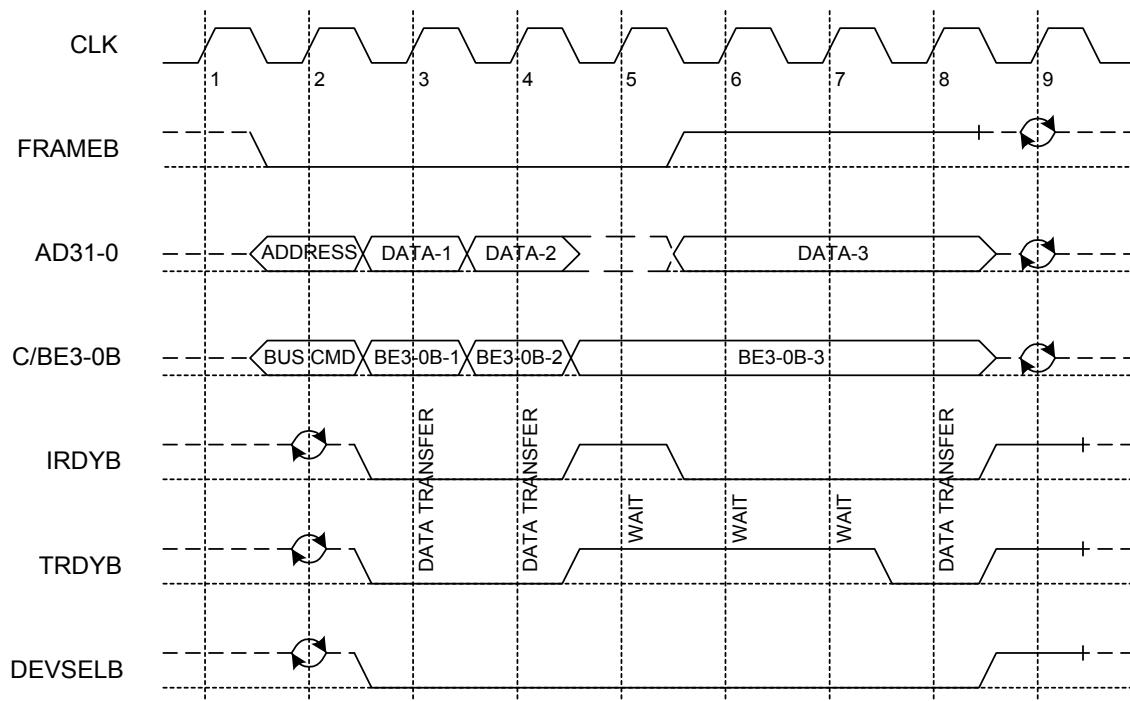
**Figure 23.   Memory Write Below 4GB**
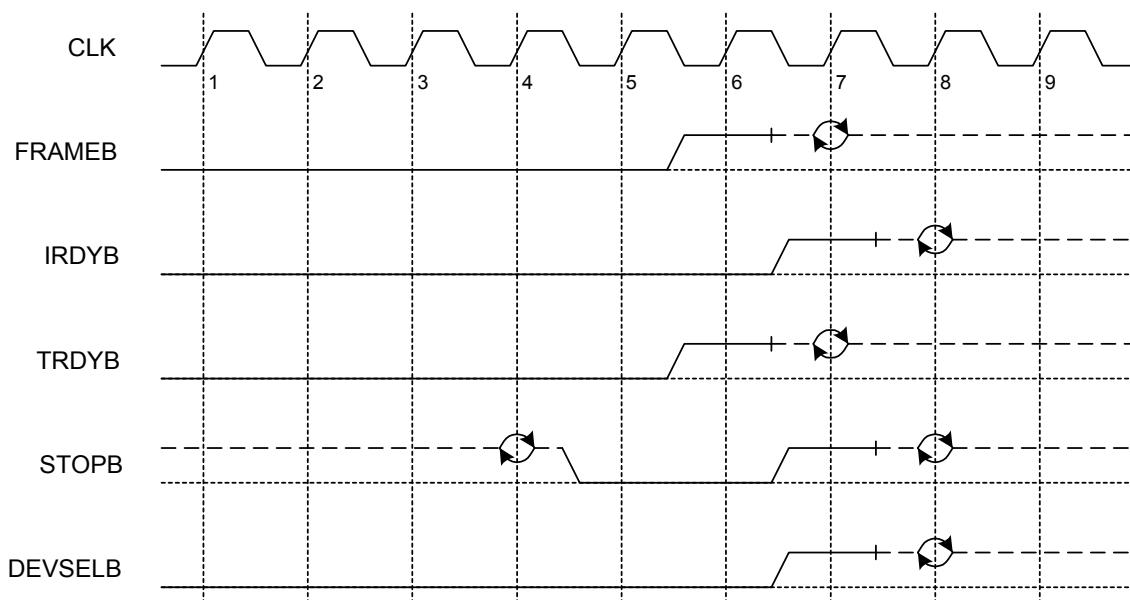
**Figure 24.   Target Initiated Termination - Disconnect**
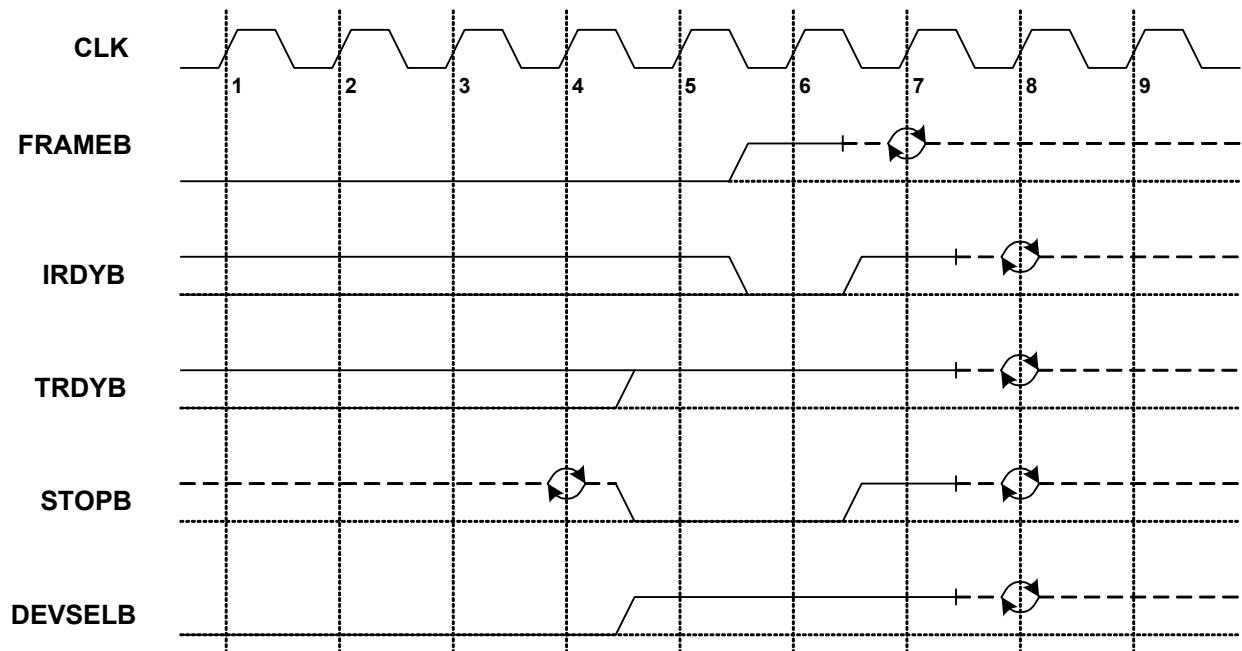
**Figure 25.   Target Initiated Termination - Abort**
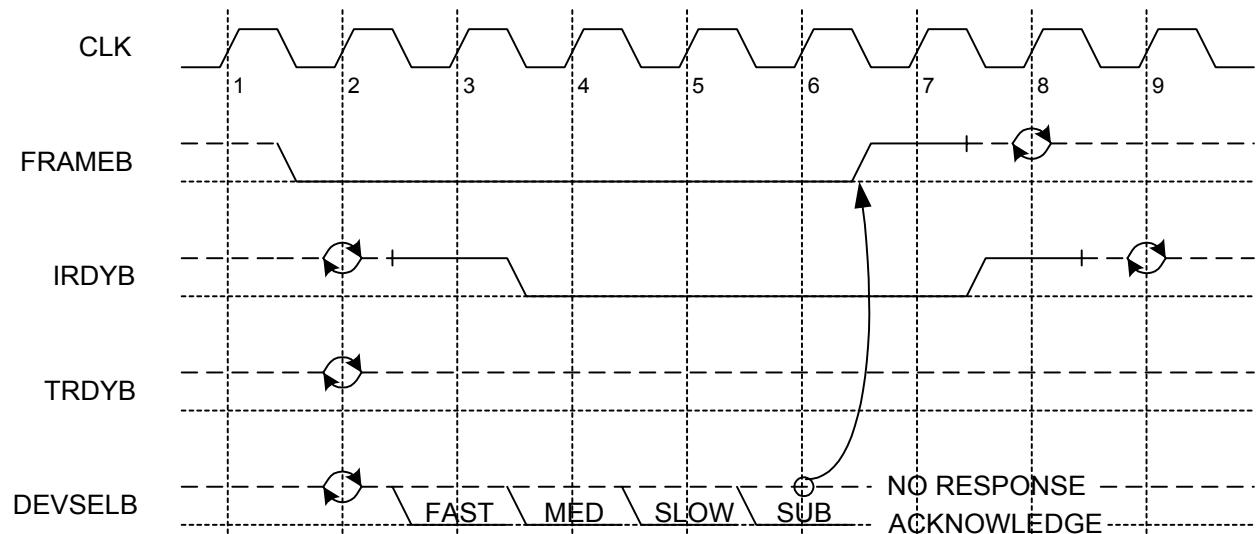
Figure 26.   Master Initiated Termination - Abort
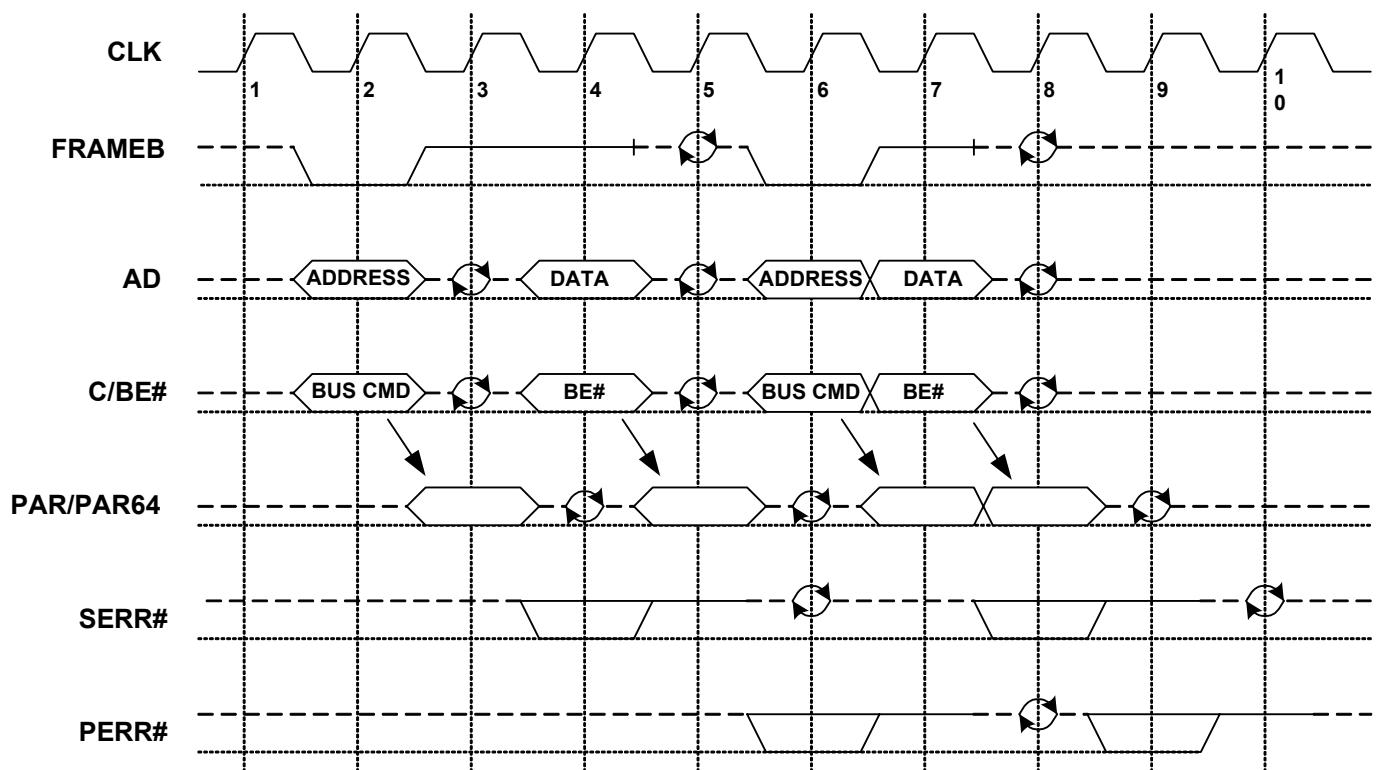
Figure 27.   Parity Operation – One Example
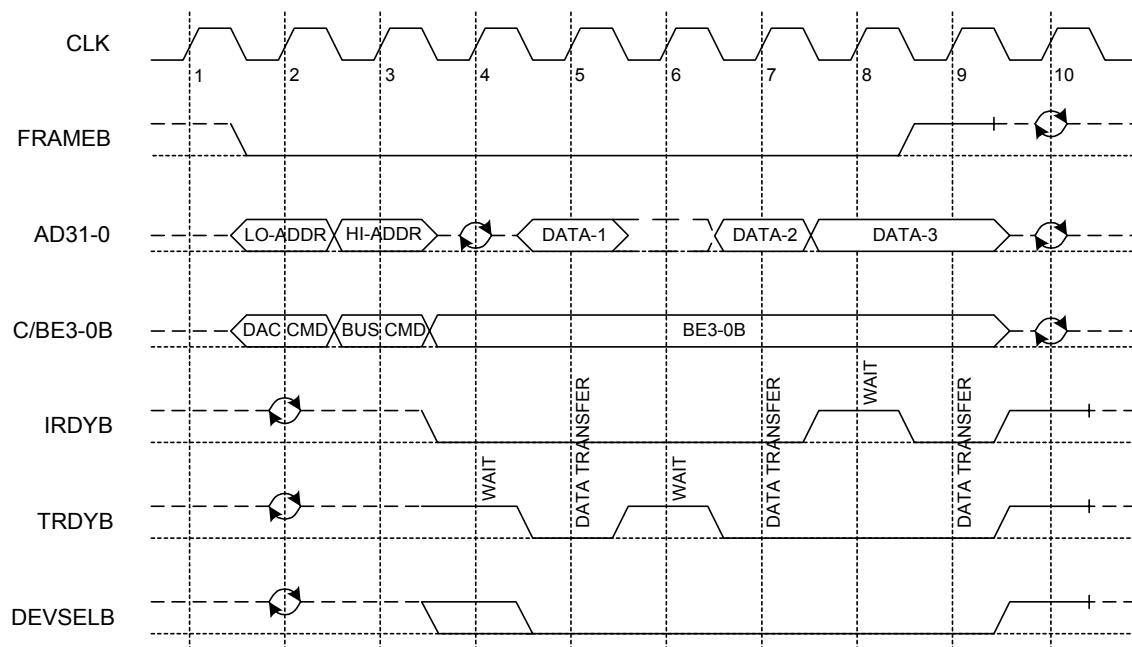
Figure 28.   Memory Read Above 4GB (DAC)
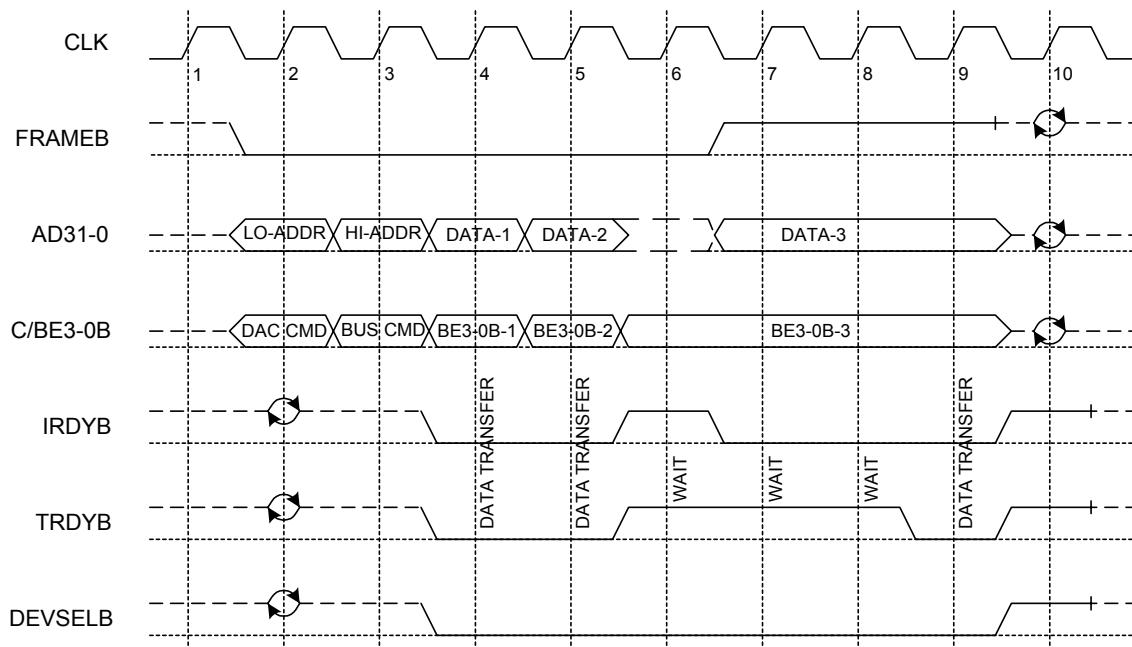
Figure 29.   Memory Write Above 4GB (DAC)

8. Mechanical Dimensions

8.1. 128-Pin QFP Mechanical Dimensions
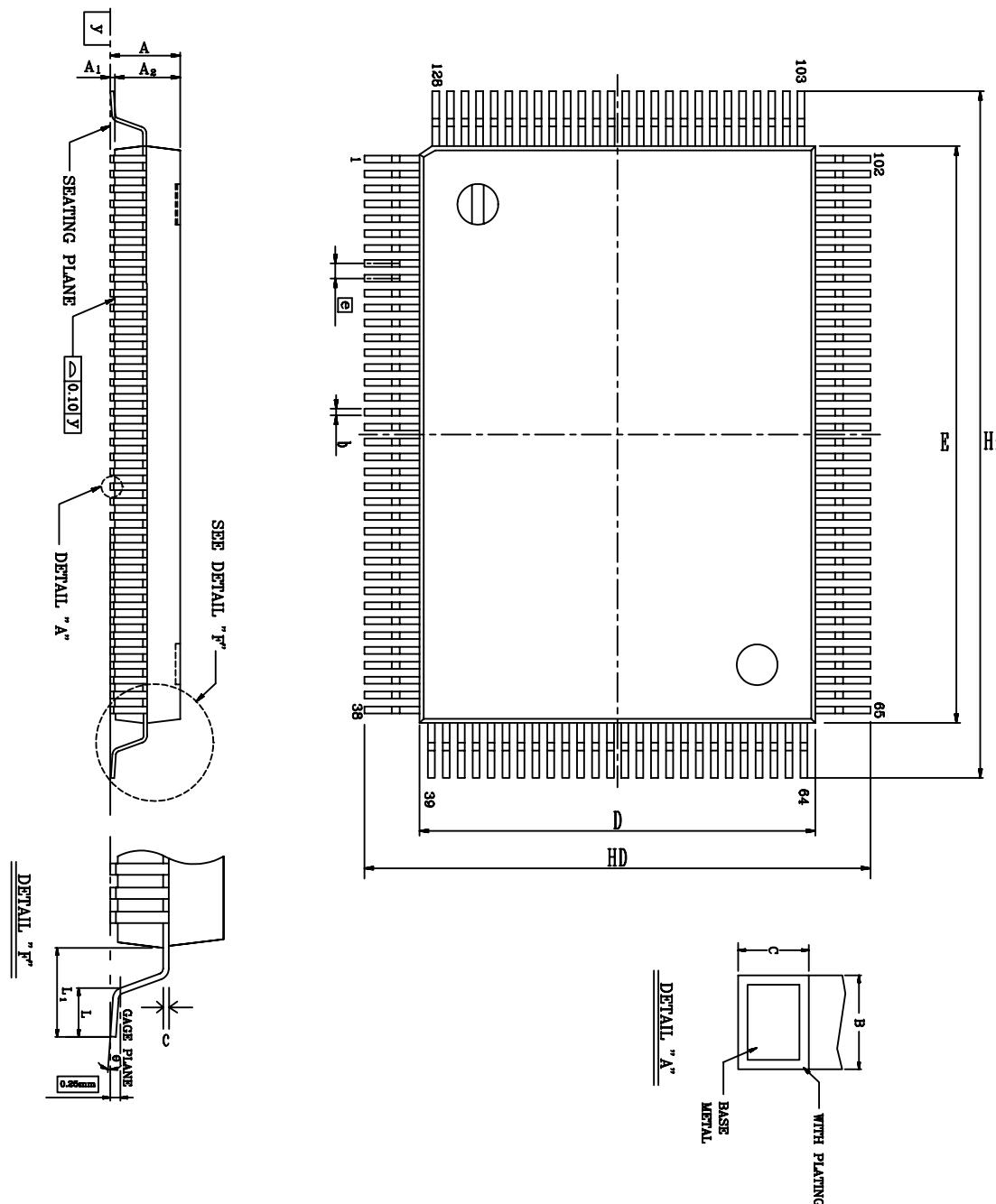
See the Mechanical Dimensions notes on the next page.

8.2. Notes for 128-Pin QFP Dimensions

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:

1. Dimensions D & E do not include interlead flash.

2. Dimension b does not include dambar protrusion/intrusion.

3. Controlling dimension: Millimeter

4. General appearance spec.   Should be based on final visual inspection.

TITLE: 128 QFP (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL			
APPROVE		DOC. NO.	
		VERSION	
		PAGE	
CHECK		DWG NO.	Q128 - 1
		DATE	
REALTEK SEMICONDUCTOR CORP.			

8.3. 128-Pin LQFP Mechanical Dimensions
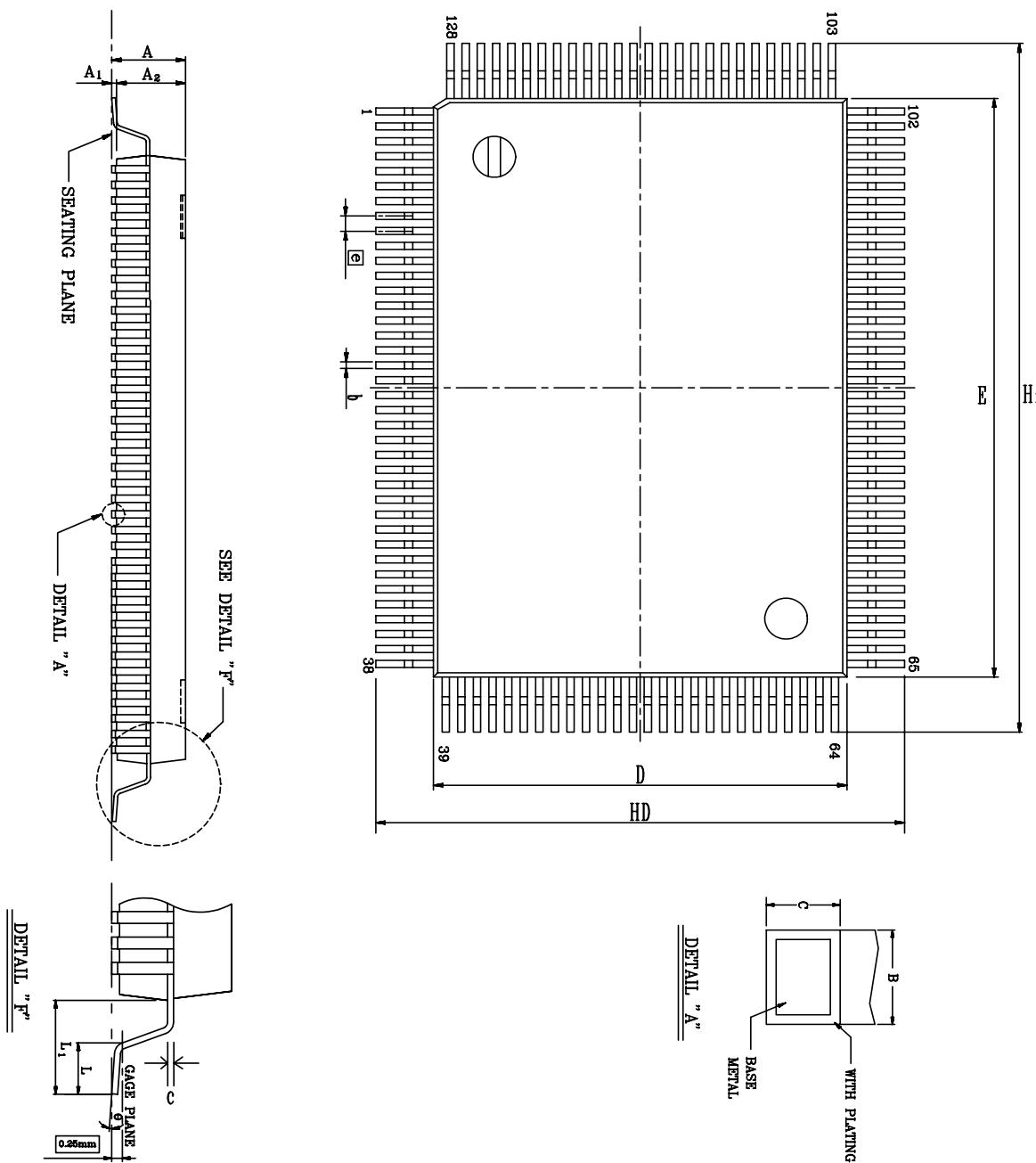
See the Mechanical Dimensions notes on the next page.

8.4. Notes for 128-Pin LQFP Dimensions

Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	-	0.25
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
b	0.006	0.009	0.011	0.15	**0.22**	0.29
c	0.004	-	0.006	0.09	-	0.20
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e		0.020	BSC		0.50	BSC
HD	0.620	0.630	0.640	15.90	**16.00**	16.30
HE	0.855	0.866	0.877	21.70	**22.00**	23.30
L	0.016	0.024	0.031	0.45	**0.60**	0.75
L1		0.039	REF		1.00	REF
θ	0°	3.5°	9°	0°	3.5°	9°

Notes:

1.Dimension b does not include dambar protrusion/intrusion.

2.Controlling dimension: Millimeter

3. General appearance spec.   Should be based on final

visual inspection.

TITLE: 128LD LQFP (14x20x1.4 mm*2) PACKAGE			
OUTLINE			
CU L/F, FOOTPRINT 2.0 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	
		PAGE	
CHECK		DWG NO.	LQ128 - 1
		DATE	
REALTEK SEMICONDUCTOR CORP.			

9. Ordering Information

Table 20.   Ordering Information

Part number	Package	Status
RTL8169SB	128-pin QFP	
RTL8169SBL	128-pin LQFP	
RTL8169SB-LF	128-pin QFP	
RTL8169SBL-LF	128-pin LQFP	