NCP1561

Push−Pull PWM Controller for 48 V Telecom Systems

The NCP1561 Push−Pull PWM controller contains all the features and flexibility needed to implement high efficiency dc−dc converters using voltage or current−mode control. This device can be configured in any dual ended topology such as push−pull or half−bridge. It can also be used for forward topologies requiring a 50% maximum duty cycle. This device is ideally suited for 48 V telecom, 42 V automotive systems and 12 V input applications.

The NCP1561 cost effectively reduce system part count by incorporating a high voltage startup regulator, line undervoltage detector, single resistor oscillator setting, dual mode overcurrent protection, soft−start and single resistor feedforward ramp generator. The oscillator frequency can be adjusted up to 250 kHz.

Features

- Internal High Voltage Startup Regulator
- Minimum Operating Voltage of 21.5 V
- Voltage or Current−Mode Control Capability
- Single Resistor Oscillator Frequency Setting
- Adjustable Frequency up to 250 kHz
- Fast Line Feedforward
- Line Undervoltage Lockout
- Dual Mode Overcurrent Protection
- Programmable Maximum Duty Cycle Control
- Maximum Duty Cycle Proportional to Line Voltage
- Programmable Soft−Start
- Precision 5.0 V Reference

Typical Applications

- 48 V Telecommunication Power Converters
- Industrial Power Converters
- 42 V Automotive Systems

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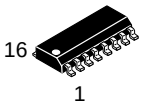
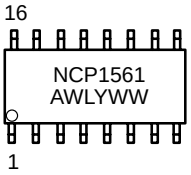
MARKING DIAGRAM

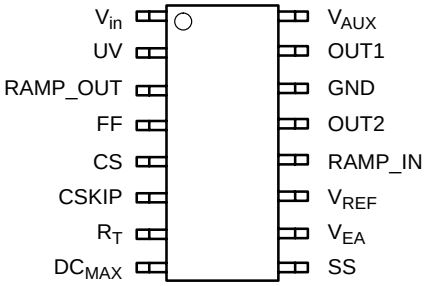


SO−16
D SUFFIX
CASE 751B



NCP1561 = Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1561DR2	SO−16	2500 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

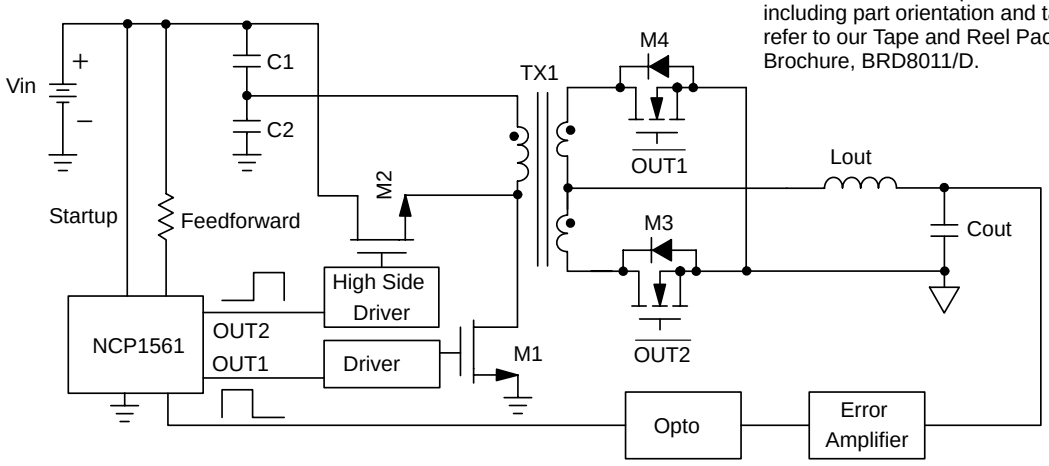


Figure 1. Half−Bridge Block Diagram

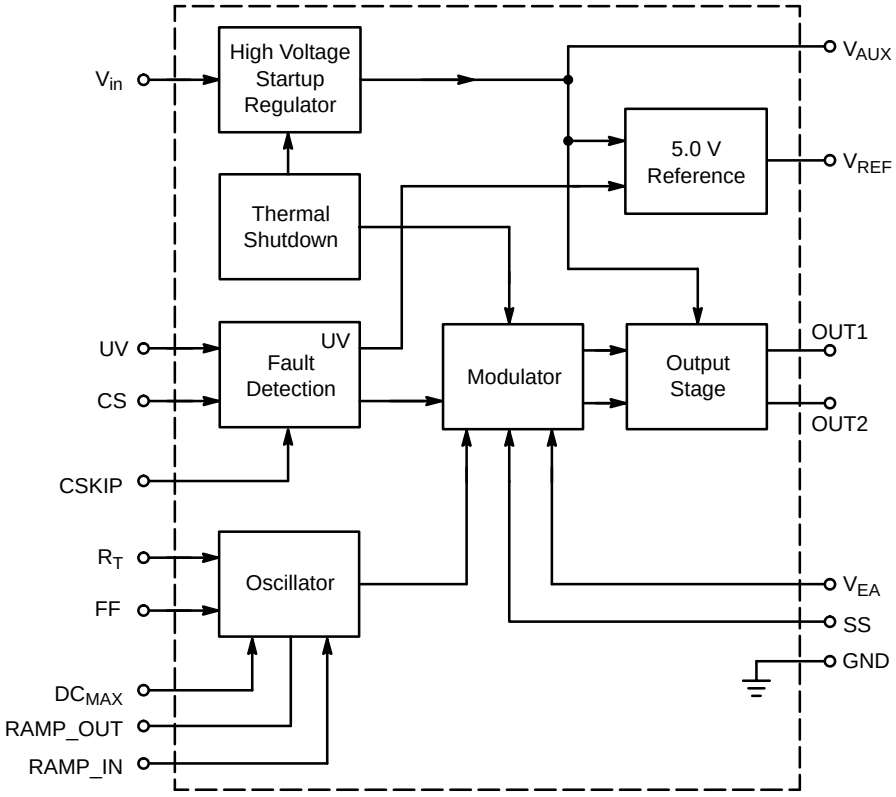


Figure 2. Simplified Block Diagram

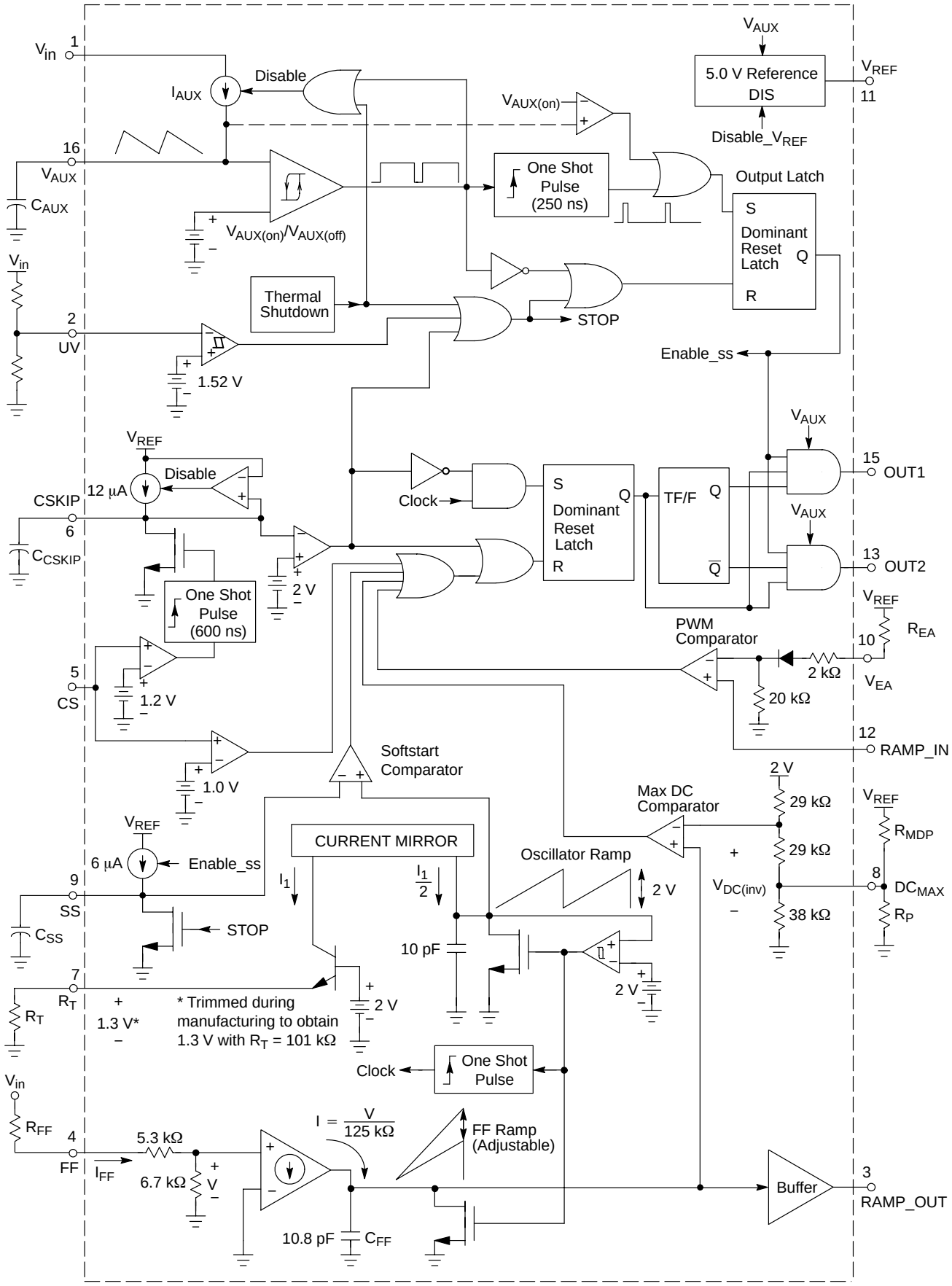


Figure 3. NCP1561 Block Diagram

PIN DESCRIPTION

Pin	Name	Application Information
1	V_{in}	This pin is connected to the bulk DC input voltage supply. A constant current source supplies current from this pin to the capacitor connected on the V_{AUX} pin. The charge current is typically 13.0 mA. Input voltage range is 21.5 V to 150 V.
2	UV	Input supply voltage is scaled down and sampled by means of a resistor divider. The supply voltage must be scaled such that the voltage on the UV pin is 1.54 V at the minimum input voltage.
3	RAMP_OUT	Internal Feedforward (FF) Ramp Output. This signal can be externally routed to the RAMP_IN pin for voltage−mode control operation.
4	FF	An external resistor between V_{in} and this pin adjusts the amplitude of the FF Ramp inversely proportional to V_{in}. By varying the Feedforward Ramp amplitude in proportion to the input voltage, changes in loop bandwidth resulting from V_{in} changes are eliminated.
5	CS	Overcurrent sense input. If the CS voltage exceeds 0.95 V or 1.15 V, the converter enters the Cycle by Cycle or Cycle Skip current limit mode, respectively.
6	CSKIP	The capacitor connected to this pin sets the Cycle Skip period. Once a cycle skip fault is detected, the capacitor connected to this pin is discharged. The capacitor is then charged with a constant current of 12 μA. The cycle skip period expires, once the voltage on this capacitor reaches 2.0 V. A soft−start sequence follows at the conclusion of the fault period.
7	R_T	A single external resistor between this pin and GND sets the fixed oscillator frequency.
8	DC_{MAX}	An external resistor between this pin and GND sets the voltage on the Max DC Comparator inverting input. The duty cycle is limited by comparing the voltage on the Max DC Comparator inverting input to the Feedforward Ramp.
9	SS	An internal 6.0 μA current source charges the external capacitor connected to this pin. The duty cycle is limited during startup by comparing the voltage on this pin to the Oscillator Ramp. The soft−start comparator limits the duty cycle while the SS voltage is below 2.0 V.
10	V_{EA}	The error signal from an external error amplifier is fed into this input and compared to the Feedforward Ramp. A series diode and resistor offset the voltage on this pin before it is applied to the PWM Comparator inverting input.
11	V_{REF}	Precision 5.0 V reference output. Maximum output current is 6.0 mA.
12	RAMP_IN	This pin configures the NCP1561 for voltage or current−mode control. The internal Feedforward Ramp (voltage−mode) or a signal proportional to the inductor current (current−mode) is fed into this input and compared to the signal in the V_{EA} pin.
13	OUT2	Output 2.
14	GND	Control circuit ground.
15	OUT1	Output 1.
16	V_{AUX}	Positive input supply voltage. This pin is connected to an external capacitor for energy storage. An internal current source supplies current from V_{in} to this pin. Once the voltage on V_{AUX} reaches approximately 10.3 V, the current source turns OFF. It turns ON again once V_{AUX} falls to 7 V. During normal operation, power is supplied to the IC via this pin, by means of an auxiliary winding. The startup circuit is disabled if the voltage on the V_{AUX} pin exceeds 10.3 V.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Input Line Voltage	V_{in}	−0.3 to 150	V
Auxiliary Supply Voltage	V_{AUX}	−0.3 to 16	V
Auxiliary Supply Input Current	I_{AUX}	35	mA
OUT1 and OUT2 Voltage	V_{OUT}	−0.3 to (V_{AUX} + 0.3 V)	V
OUT1 and OUT2 Output Current	I_{OUT}	10	mA
5.0 V Reference Voltage	V_{REF}	−0.3 to 6.0	V
5.0 V Reference Output Current	I_{REF}	6.0	mA
All Other Inputs/Outputs Voltage	V_{IO}	−0.3 to V_{REF}	V
All Other Inputs/Outputs Current	I_{IO}	10	mA
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Power Dissipation at T_A = 25°C	P_D	0.77	W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	130	°C/W

1. Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
   A. This device series contains ESD protection and exceeds the following tests:
      Pin 1: Pin 1 is the HV start−up of the device and is rated to the max rating of the part, or 150 V.
      Machine Model Method 150 V.
      Pins 2−16: Human Body Model 2000 V per MIL−STD−883, Method 3015.
      Machine Model Method 200 V.

ELECTRICAL CHARACTERISTICS (V_{in} = 48 V, V_{AUX} = 12 V, V_{EA} = 2 V, R_T = 101 kΩ, C_{CSKIP} = 6800 pF, R_D = 60.4 kΩ, R_{FF} = 432 kΩ, for typical values T_J = 25°C, for min/max values, T_J = −40°C to 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
START−UP CONTROL AND V_{AUX} REGULATOR					
V_{AUX} Regulation					V
Startup Threshold/V_{AUX} Regulation Peak (V_{AUX} increasing)	$V_{AUX(on)}$	9.7	10.3	10.8	
Minimum Operating V_{AUX} Valley Voltage After Turn−On	$V_{AUX(off)}$	6.6	7.0	7.4	
Hysteresis	V_H	−	3.3	−	
Minimum Startup Voltage (Pin 1) I_{START} = 1.0 mA, I_{REF} = 0 mA, V_{AUX} = $V_{AUX(on)}$ − 0.2 V	$V_{START(min)}$	−	18.3	21.5	V
Startup Circuit Output Current	I_{START}				mA
V_{AUX} = 0 V					
T_J = 25°C		13	17	21	
T_J = −40°C to 125°C		10	−	25	
V_{AUX} = $V_{AUX(on)}$ − 0.2 V					
T_J = 25°C		10	13	17	
T_J = −40°C to 125°C		8.0	−	19	
Startup Circuit Off−State Leakage Current (V_{in} = 150 V)	$I_{START(off)}$				μA
T_J = 25°C		−	23	50	
T_J = −40°C to 125°C		−	−	100	
Startup Circuit Breakdown Voltage (Note 2) $I_{START(off)}$ = 50 μA, T_J = 25°C	$V_{BR(DS)}$	150	−	−	V
Auxilliary Supply Current After V_{AUX} Turn−On					mA
Outputs Disabled					
V_{EA} = 0 V	I_{AUX1}	−	3.3	5.0	
V_{UV} = 0 V	I_{AUX2}	−	1.8	2.5	
Outputs Enabled	I_{AUX3}	−	4.1	6.5	
LINE UNDERVOLTAGE DETECTOR					
Undervoltage Threshold (V_{in} Increasing)	V_{UV}	1.40	1.54	1.64	V
Undervoltage Hysteresis	$V_{UV(H)}$	0.080	0.095	0.120	V
Undervoltage Propagation Delay to Output	t_{UV}	−	250	−	ns
CURRENT LIMIT AND THERMAL SHUTDOWN					
Cycle by Cycle Threshold Voltage	I_{LIM1}	0.89	0.95	1.03	V
Propagation Delay to Output (V_{EA} = 2.0 V) V_{CS} = I_{LIM1} to 2.0 V, measured when OUT1 reaches 10 V.	t_{ILIM}	−	86	150	ns
Cycle Skip Threshold Voltage	I_{LIM2}	1.05	1.15	1.24	V
Cycle Skip Charge Current (V_{CSKIP} = 0 V)	I_{CSKIP}	8.0	12.3	15	μA
Thermal Shutdown Threshold (Junction Temperature Increasing, Note 2)	T_{SHDN}	−	180	−	°C
Thermal Shutdown Hysteresis (Junction Temperature Decreasing, Note 2)	T_H	−	17	−	°C

2. Guaranteed by design only.

ELECTRICAL CHARACTERISTICS (V_{in} = 48 V, V_{AUX} = 12 V, V_{EA} = 2 V, R_T = 101 kΩ, C_{CSKIP} = 6800 pF, R_D = 60.4 kΩ, R_{FF} = 432 kΩ, for typical values T_J = 25°C, for min/max values, T_J = −40°C to 125°C, unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL OUTPUTS					
Frequency (R_T = 101 kΩ) T_J = 25°C T_J = −40°C to 125°C	f_{OSC1}	 143 137	 150 −	 157 163	kHz
Frequency (R_T = 59 kΩ) T_J = 25°C T_J = −40°C to 125°C	f_{OSC2}	 228 220	 240 −	 252 260	kHz
Output Voltage (I_{OUT} = 0 mA) Low State High State	 V_{OL} V_{OH}	 − −	 0.25 11.8	 − −	V
Drive Resistance (V_{in} = 15 V) Sink (V_{EA} = 0 V, V_{OUT} = 2 V) Source (V_{EA} = 3 V, V_{OUT} = 10 V)	 R_{SNK} R_{SRC}	 20 50	 36 88	 80 170	Ω
Rise Time (C_L = 100 pF, 10% to 90% of V_{OH})	t_{on}	−	32	−	ns
Fall Time (C_L = 100 pF, 90% to 10% of V_{OH})	t_{off}	−	19	−	ns
MAXIMUM DUTY CYCLE COMPARATOR					
Maximum Duty Cycle (V_{in} = 36 V) R_P = 0 Ω, R_{MDP} = open R_P = open, R_{MDP} = open (Note 3)	DC_{MAX}	 34 48	 38 −	 44 50	%
Open Circuit Voltage	V_{DCMAX}	0.49	0.74	0.90	V
SOFT−START					
Charge Current (V_{SS} = 1.0 V)	$I_{SS(C)}$	5.0	6.2	7.4	μA
Discharge Current (V_{SS} = 5.0 V, V_{UV} = 1.0 V)	$I_{SS(D)}$	20	50	−	mA
PWM COMPARATOR					
Input Resistance (V_1 = 1.25 V, V_2 = 1.50 V) $R_{IN(VEA)} = (V_2 - V_1) / (I_2 - I_1)$	$R_{IN(VEA)}$	8.0	22	60	kΩ
Lower Input Threshold	$V_{EA(L)}$	0.7	0.92	1.1	V
Delay to Output (from V_{OH} to 0.5 V_{OH})	t_{PWM}	−	200	−	ns
5.0 V REFERENCE					
Output Voltage (I_{REF} = 0 mA) T_J = 25°C T_J = −40°C to 125°C	V_{REF}	 4.9 4.8	 4.96 −	 5.1 5.1	V
Load Regulation (I_{REF} = 0 to 6 mA)	$V_{REF(Load)}$	−	10	50	mV
Line Regulation (V_{AUX} = 7.5 V to 16 V)	$V_{REF(Line)}$	−	50	100	mV

3. 50% Maximum Duty Cycle guaranteed by design.

TYPICAL CHARACTERISTICS

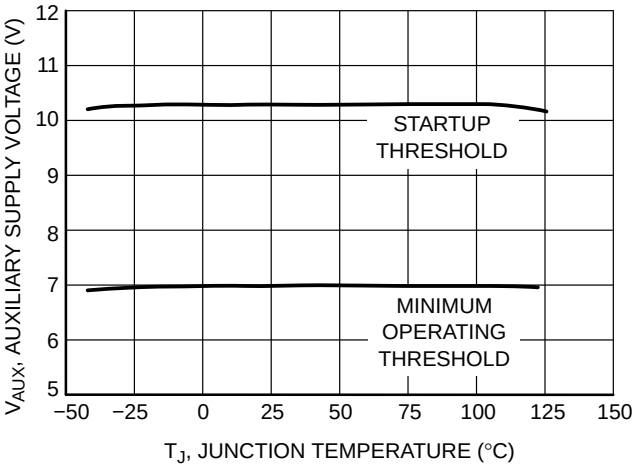


Figure 4. Auxiliary Supply Voltage Thresholds versus Junction Temperature

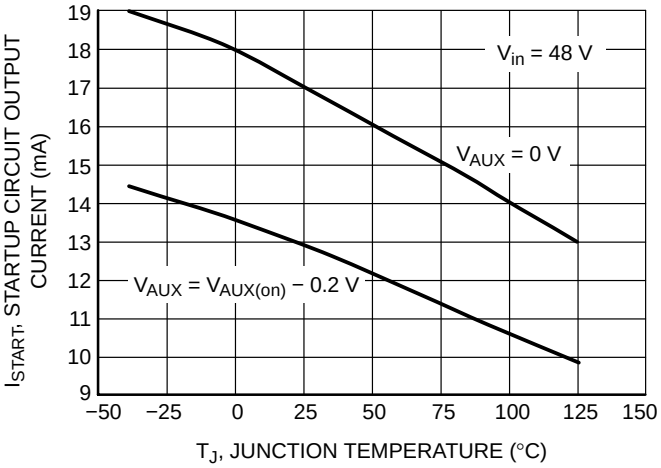


Figure 5. Startup Circuit Output Current versus Junction Temperature

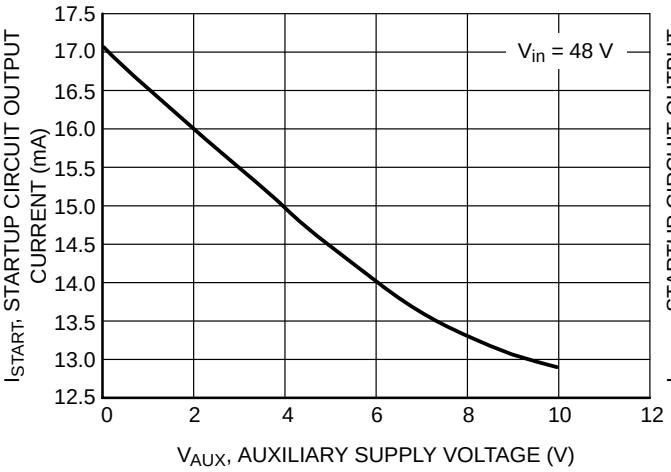


Figure 6. Startup Circuit Output Current versus Auxiliary Supply Voltage

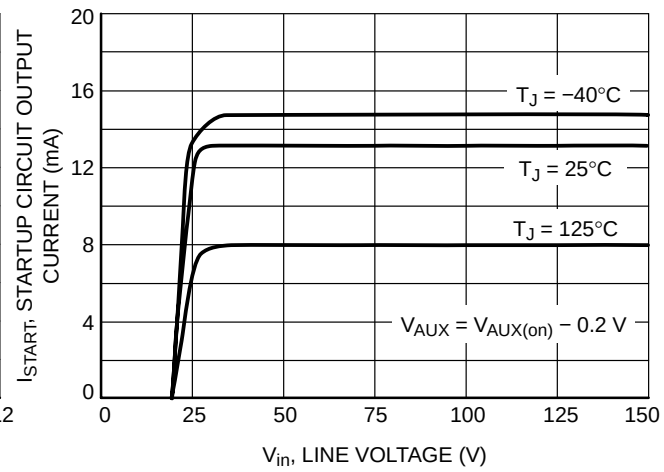


Figure 7. Startup Circuit Output Current versus Line Voltage

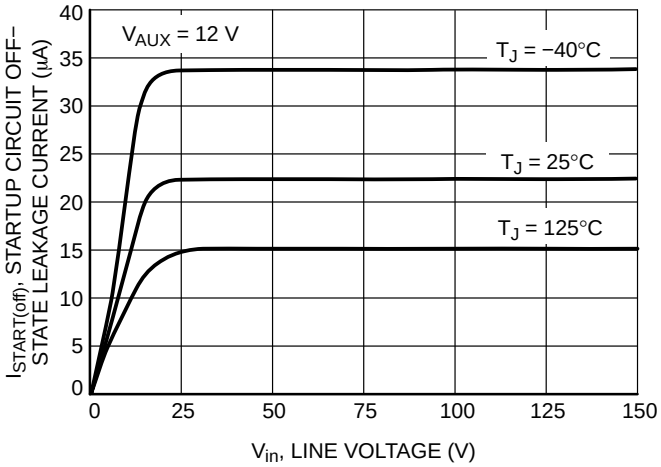


Figure 8. Startup Circuit Off−State Leakage Current versus Line Voltage

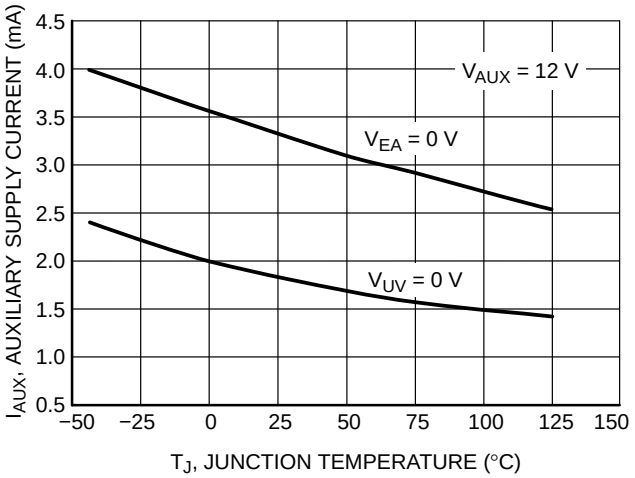


Figure 9. Auxiliary Supply Current versus Junction Temperature

TYPICAL CHARACTERISTICS

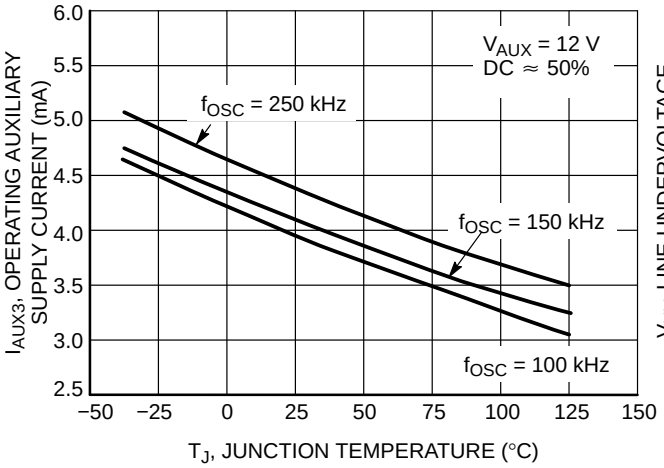


Figure 10. Operating Auxiliary Supply Current versus Junction Temperature

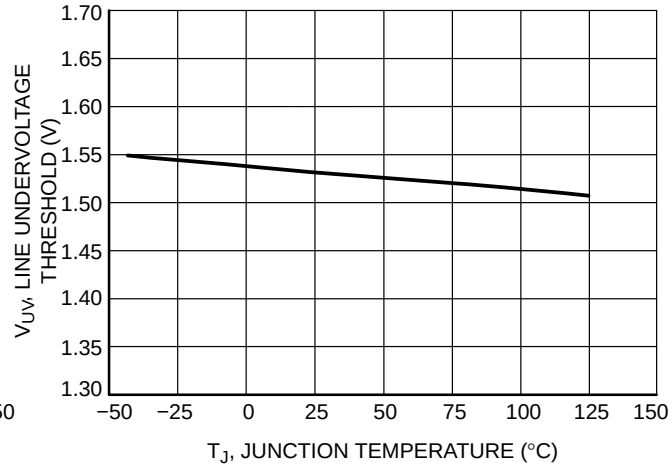


Figure 11. Line Undervoltage Threshold versus Junction Temperature

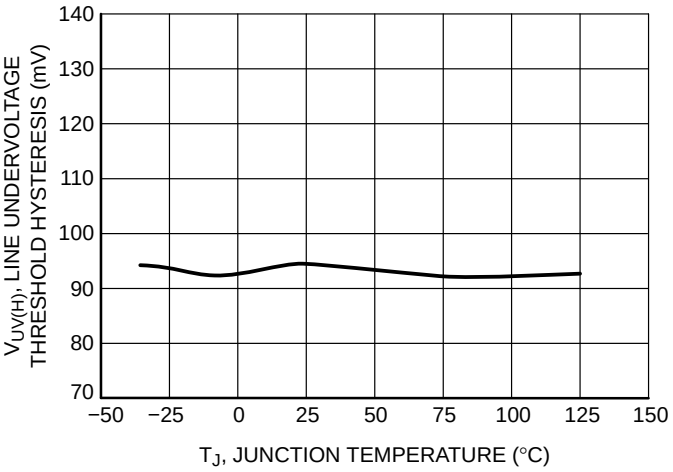


Figure 12. Line Undervoltage Hysteresis versus Junction Temperature

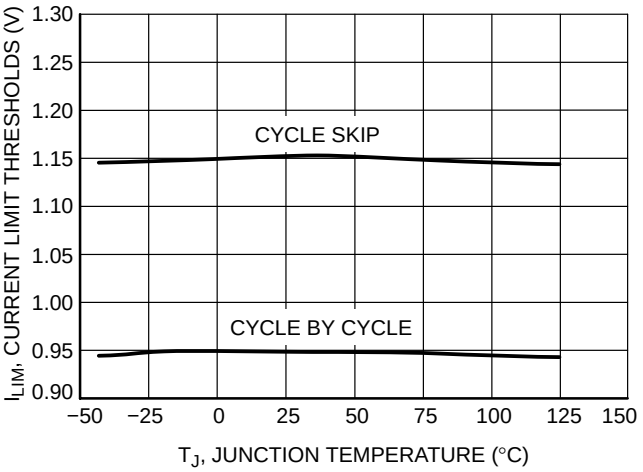


Figure 13. Current Limit Thresholds versus Junction Temperature

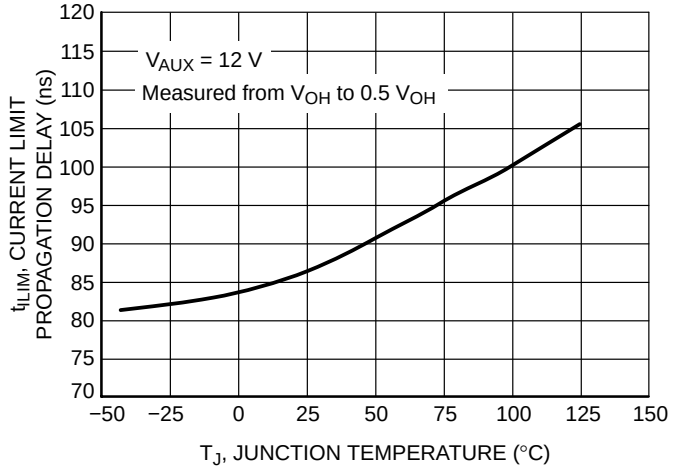


Figure 14. Current Limit Propagation Delay versus Junction Temperature

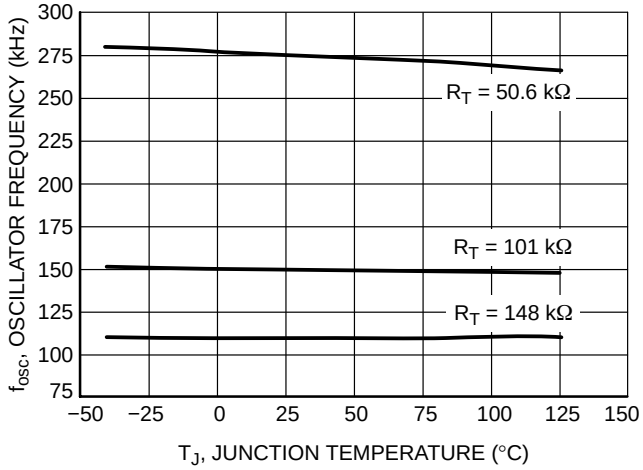


Figure 15. Oscillator Frequency versus Junction Temperature

TYPICAL CHARACTERISTICS

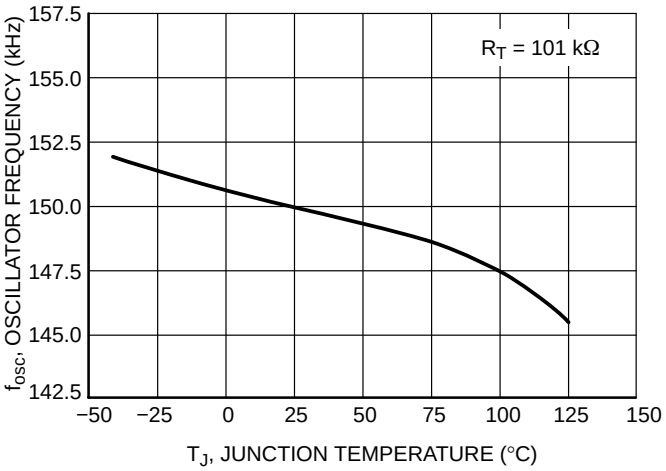


Figure 16. Oscillator Frequency versus Junction Temperature

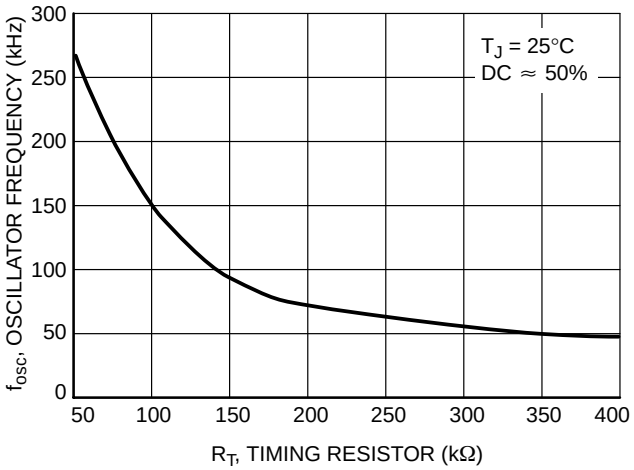


Figure 17. Oscillator Frequency versus Timing Resistor

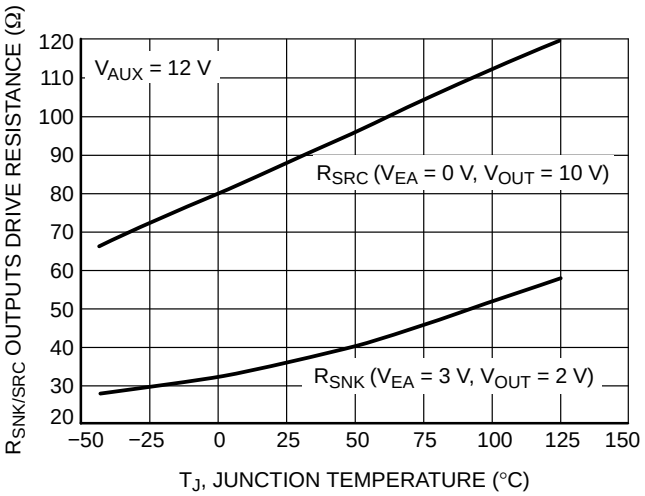


Figure 18. Outputs Drive Resistance versus Junction Temperature

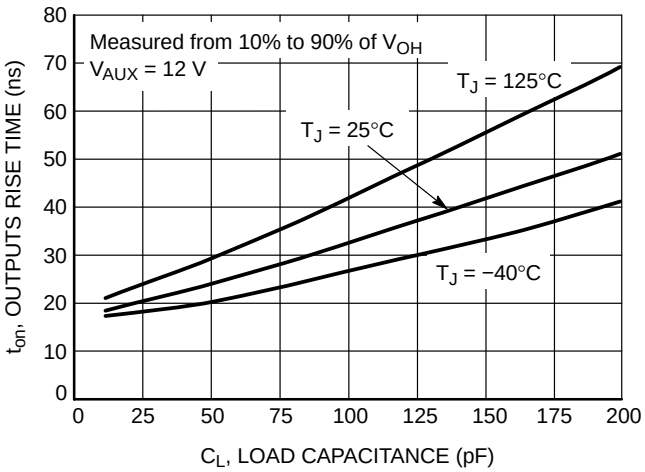


Figure 19. Outputs Rise Time versus Load Capacitance

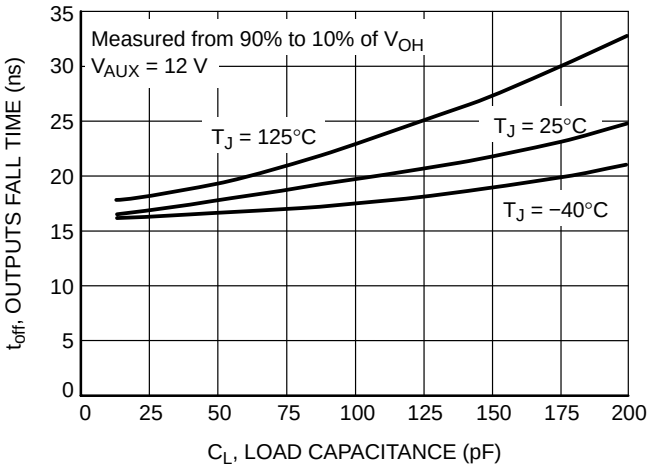


Figure 20. Outputs Fall Time versus Load Capacitance

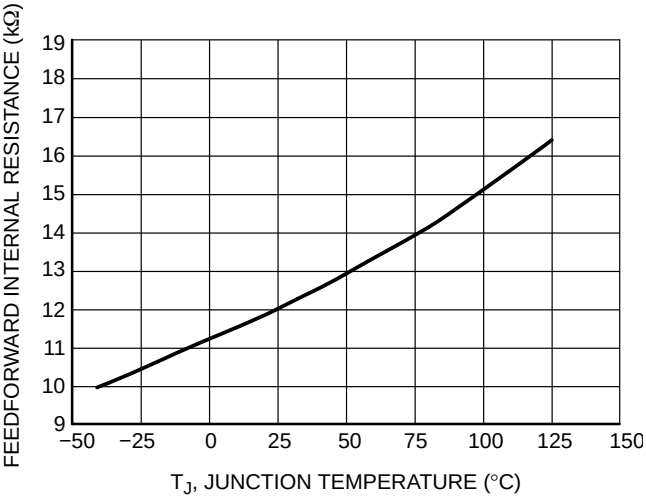


Figure 21. Feedforward Internal Resistance versus Junction Temperature

TYPICAL CHARACTERISTICS

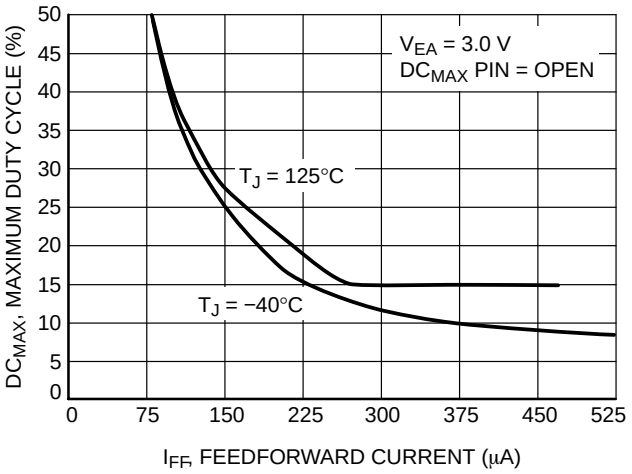


Figure 22. Maximum Duty Cycle versus Feedforward Current

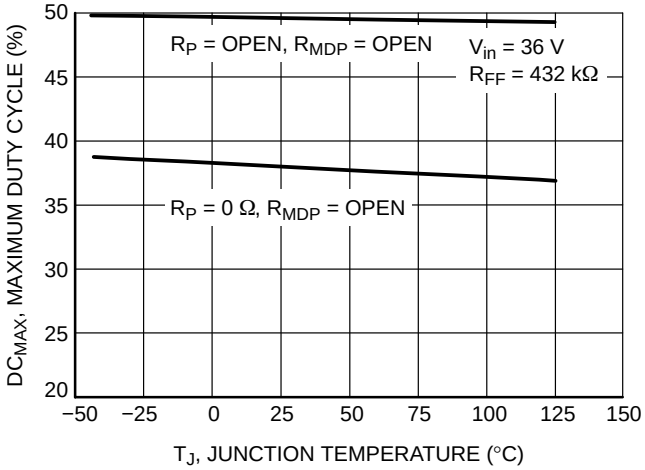


Figure 23. Maximum Duty Cycle versus Junction Temperature

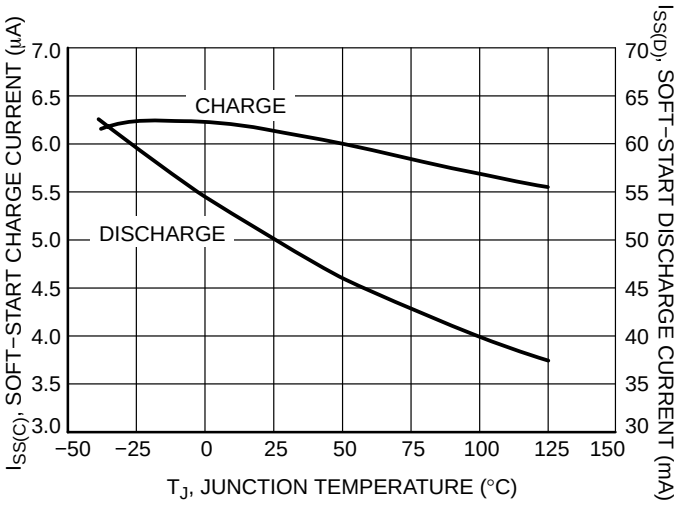


Figure 24. Soft−Start Charge/Discharge Currents versus Junction Temperature

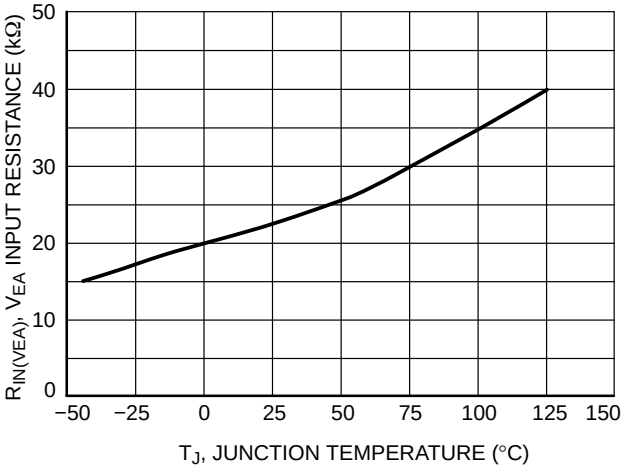


Figure 25. V_{EA} Input Resistance versus Junction Temperature

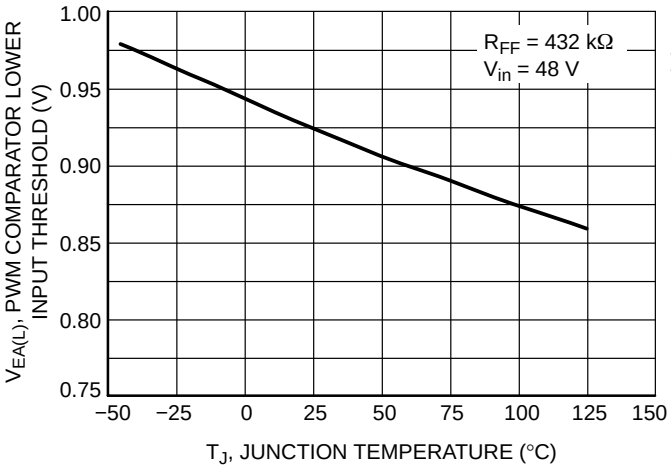


Figure 26. PWM Comparator Lower Input Threshold versus Junction Temperature

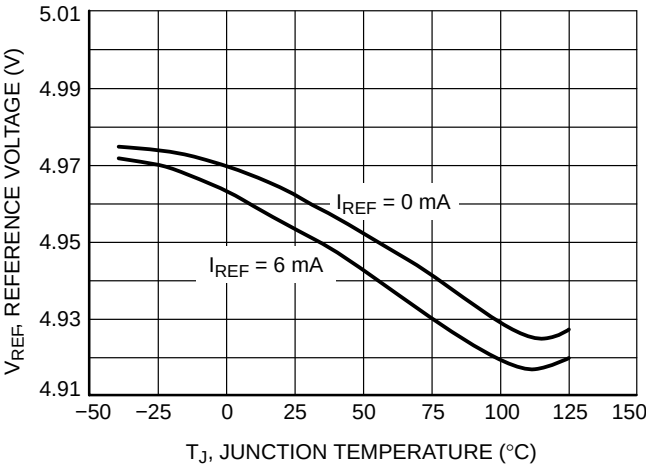


Figure 27. Reference Voltage versus Junction Temperature

DETAILED OPERATING DESCRIPTION

The NCP1561 is a push−pull PWM controller for use in 48 V telecom power converters or 42 V automotive systems. This controller contains all the features and flexibility required in high density isolated dc−dc modules and on−board designs for telecom and automotive systems. It can be configured for operation in voltage−mode with feedforward or current−mode control. The extensive set of features included in the NCP1561 facilitates system design and reduces overall system cost and component count by incorporating supervisory functions and components traditionally found outside the controller. Features of the NCP1561 include a high voltage startup regulator, fast line feedforward, a line undervoltage lockout, dual mode overcurrent protection, programmable maximum duty cycle limit, programmable soft start and external voltage reference.

Voltage−mode operation with line feedforward provides better line regulation without some of the traditional problems associated with current−mode control. The controller is configured for voltage−mode operation by routing the internal Feedforward Ramp output (RAMP_OUT) to the PWM Comparator non−inverting input (RAMP_IN). The amplitude of the Feedforward Ramp varies inversely proportional to the input voltage. Operation in current−mode control is obtained by routing a signal proportional to the inductor current into the PWM Comparator non−inverting input (V_{EA} pin). In either mode, the maximum duty cycle is inversely proportional to the line voltage, as configured by the DC_{MAX} pin and FF pins.

High Voltage Start−up Regulator

The NCP1561 contains an internal high voltage start−up regulator that eliminates the need for external start−up components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding. The startup regulator consists of a constant current source that supplies current from the input line voltage (V_{in}) to the capacitor on the V_{AUX} pin (C_{AUX}). The startup current is typically 13.0 mA. Once V_{AUX} reaches approximately 10.3 V, the start−up regulator turns OFF and the outputs are enabled. When V_{AUX} reaches 7 V, the outputs are disabled and the startup regulator turns ON. This mode of operation is known as Dynamic Self Supply (DSS).

The startup circuit sources current out of the V_{AUX} pin. It is recommended to place a diode between C_{AUX} and the auxiliary supply as shown in Figure 28. This will allow the NCP1561 to charge C_{AUX} while preventing the startup regulator from sourcing current into the auxiliary supply.

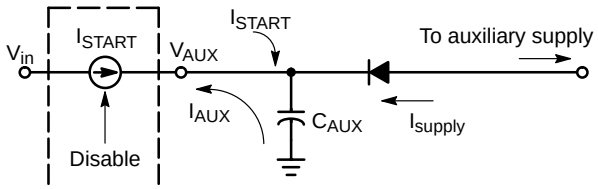


Figure 28. Recommended V_{AUX} Configuration

Power to the controller while operating in the self−bias or DSS mode is provided by C_{AUX}. Therefore, C_{AUX} must be sized such that a V_{AUX} voltage greater than 7 V is maintained while the outputs are enabled and the converter reaches regulation. Also, the V_{AUX} discharge time (from 10.3 V to 7 V) must be greater than the soft−start charge period to assure the converter turns ON. The startup circuit is rated at a maximum voltage of 150 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller.

The startup regulator is disabled by biasing V_{AUX} above 7 V once the outputs are enabled. It can also be disabled by biasing V_{AUX} above $V_{AUX(on)}$ (typically 10.3 V). This feature allows the NCP1561 to operate from an independent 12 V (±10%) supply. The independent supply should keep V_{AUX} above $V_{AUX(on)}$. Otherwise the Output Latch will not be SET and the outputs will remain OFF after a fault condition is cleared. If operating from an independent supply, the V_{in} and V_{AUX} pins should be connected together.

Line Undervoltage Shutdown

The NCP1561 incorporates a line undervoltage shutdown (UV) circuit. The undervoltage threshold is approximately 1.54 V.

The UV circuit can be biased using an external resistor divider from the input line. The resistor divider must be sized to enable the controller once V_{in} is within the required operating range.

Once the UV condition is removed and V_{AUX} reaches $V_{AUX(on)}$, the controller initiates a soft−start cycle, as shown in Figure 29.

The UV pin can also be used to implement a remote enable/disable function. Biasing the UV pin below its UV threshold disables the converter.

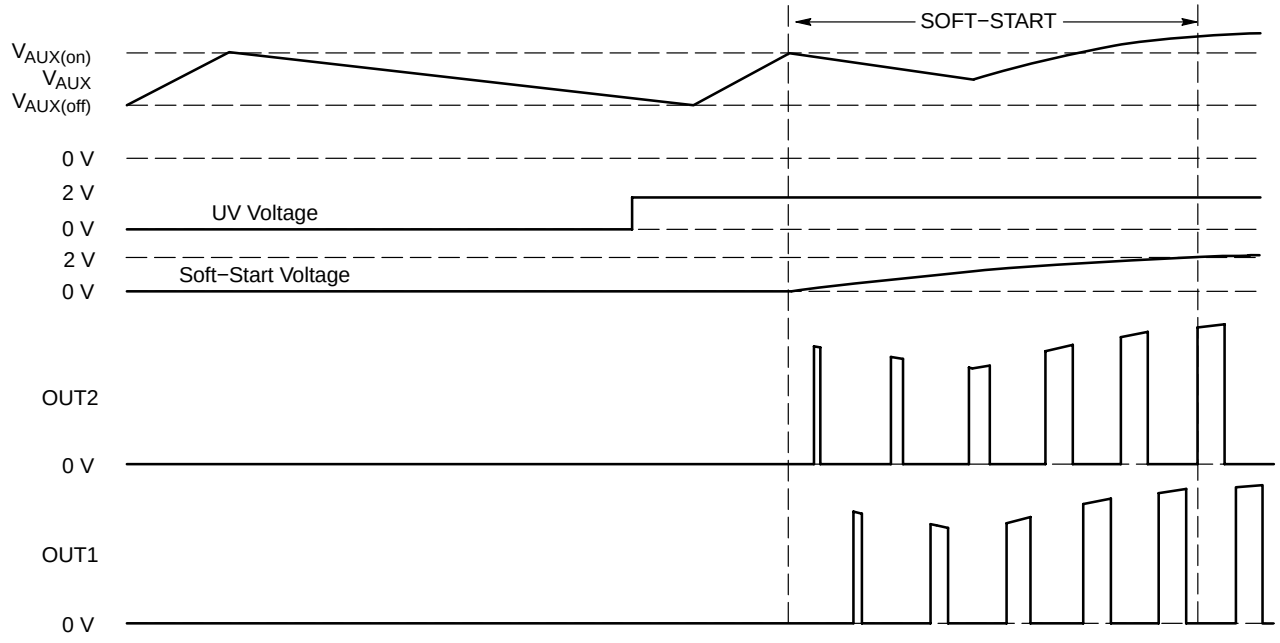


Figure 29. Soft−Start Timing Diagram (Using Auxiliary Winding)

If the UV threshold is reached, once in normal operation, the soft−start capacitor is discharged, and the outputs are immediately disabled as shown in Figure 30. Also, if an UV condition is detected, the 5.0 V Reference Supply is disabled.

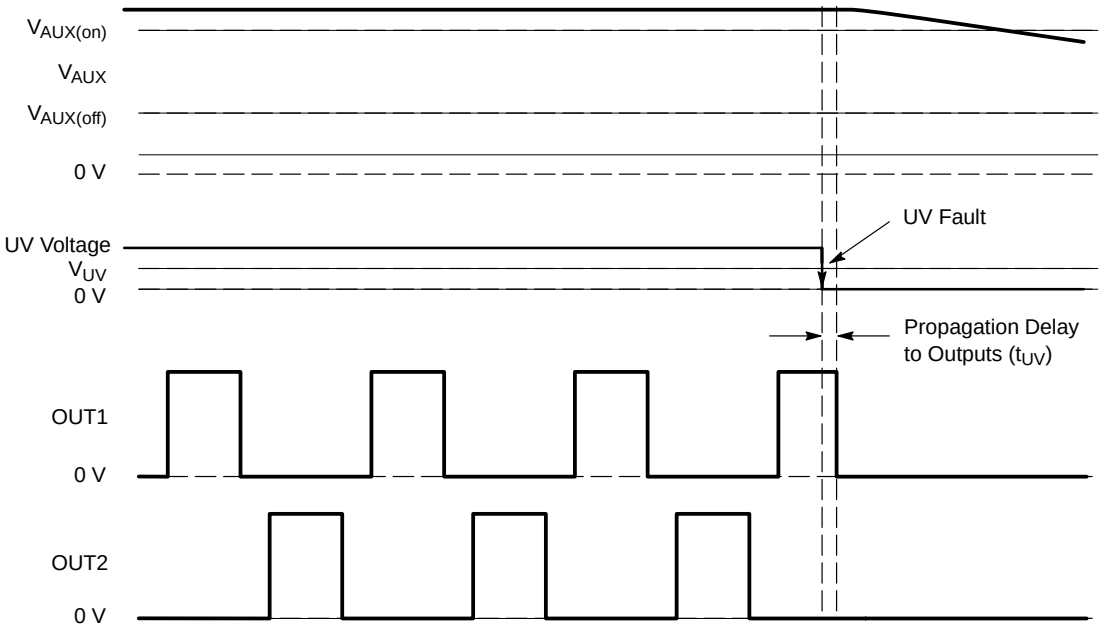


Figure 30. UV Fault Timing Diagram

Feedforward Ramp Generator

The NCP1561 incorporates line feedforward (FF) to compensate for changes in line voltage. A FF Ramp proportional to V_{in} is generated and compared to the error signal. If the line voltage changes, the FF Ramp slope changes accordingly. The duty cycle will be adjusted immediately instead of waiting for the line voltage change to propagate around the system and be reflected back on V_{EA}.

A resistor between V_{in} and the FF pin (R_{FF}) sets the feedforward current (I_{FF}). The FF Ramp is generated by charging an internal 10.8 pF capacitor (C_{FF}) with a constant current proportional to I_{FF}. The FF Ramp is finished (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. Please refer to Figure 3 for a functional drawing of the Feedforward Ramp generator.

I_{FF} is usually a few hundred microamps, depending on the operating frequency and the required duty cycle. If the operating frequency and maximum duty cycle are known, I_{FF} is calculated using the equation below:

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 125\ k\Omega}{6.7\ k\Omega \times t_{on(max)}}$$

where $V_{DC(inv)}$ is the voltage on the inverting input of the Max DC Comparator and $t_{on(max)}$ is the maximum ON time. Figure 22 shows the relationship between I_{FF} and DC_{MAX}. For example, if a system is designed to operate at an oscillator frequency of 150 kHz, with a 45% maximum duty cycle at 36 V, the DC_{MAX} pin can be grounded and I_{FF} is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{150\ kHz} = 6.66\ \mu s$$

$$t_{on(max)} = DC_{MAX} \times T = 0.45 \times 6.66\ \mu s = 3.0\ \mu s$$

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 125\ k\Omega}{6.7\ k\Omega \times t_{on(max)}}$$

$$= \frac{10.8\ pF \times 1.0\ V \times 125\ k\Omega}{6.7\ k\Omega \times 3.0\ \mu s} = 67.2\ \mu A$$

As the minimum line voltage is 36 V, the required feedforward resistor is calculated using the equation below:

$$R_{FF} = \frac{V_{in}}{I_{FF}} - 12.0\ k\Omega = \frac{36\ V}{67.2\ \mu A} - 12.0\ k\Omega \approx 523\ k\Omega$$

From the above calculations it can be observed that I_{FF} is controlled predominantly by the value of R_{FF}, as the resistance seen into the FF pin is only 12 kΩ. If a tight maximum duty cycle control over temperature is required, R_{FF} should have a low thermal coefficient. If current−mode control is used and the FF Ramp generator is not used for maximum duty cycle control, the FF Ramp generator can be disabled grounding the FF pin.

Current Limit

The NCP1561 has two overcurrent protection modes, cycle by cycle and cycle skip. It allows the NCP1561 to handle momentary and hard shorts differently for the best tradeoff in system performance and safety. The outputs are disabled typically 86 ns after a current limit fault is detected.

The cycle by cycle mode terminates the conduction cycle (reducing the duty cycle) if the voltage on the CS pin exceeds 0.95 V. The cycle skip mode is enabled if the voltage on the CS pin reaches 1.15 V. Once a cycle skip fault is detected, the outputs are disabled, the soft−start and cycle skip capacitors are discharged, and the cycle skip period (T_{CSKIP}) commences.

The cycle skip period is set by an external capacitor (C_{CSKIP}). Once a cycle skip fault is detected, the cycle skip capacitor is discharged followed by a charge cycle. The charge current is 12.3 μA. The cycle skip period ends when the voltage on the cycle skip capacitor reaches 2.0 V. If the cycle skip period is known, the cycle skip capacitor is calculated using the equation below:

$$C_{CSKIP} \approx \frac{T_{CSKIP} \times 12.3\ \mu A}{2\ V}$$

Using the above equation, a cycle skip period of 11.0 μs requires a cycle skip capacitor of 68 pF. The differences between the cycle by cycle and cycle skip modes are shown in Figure 31.

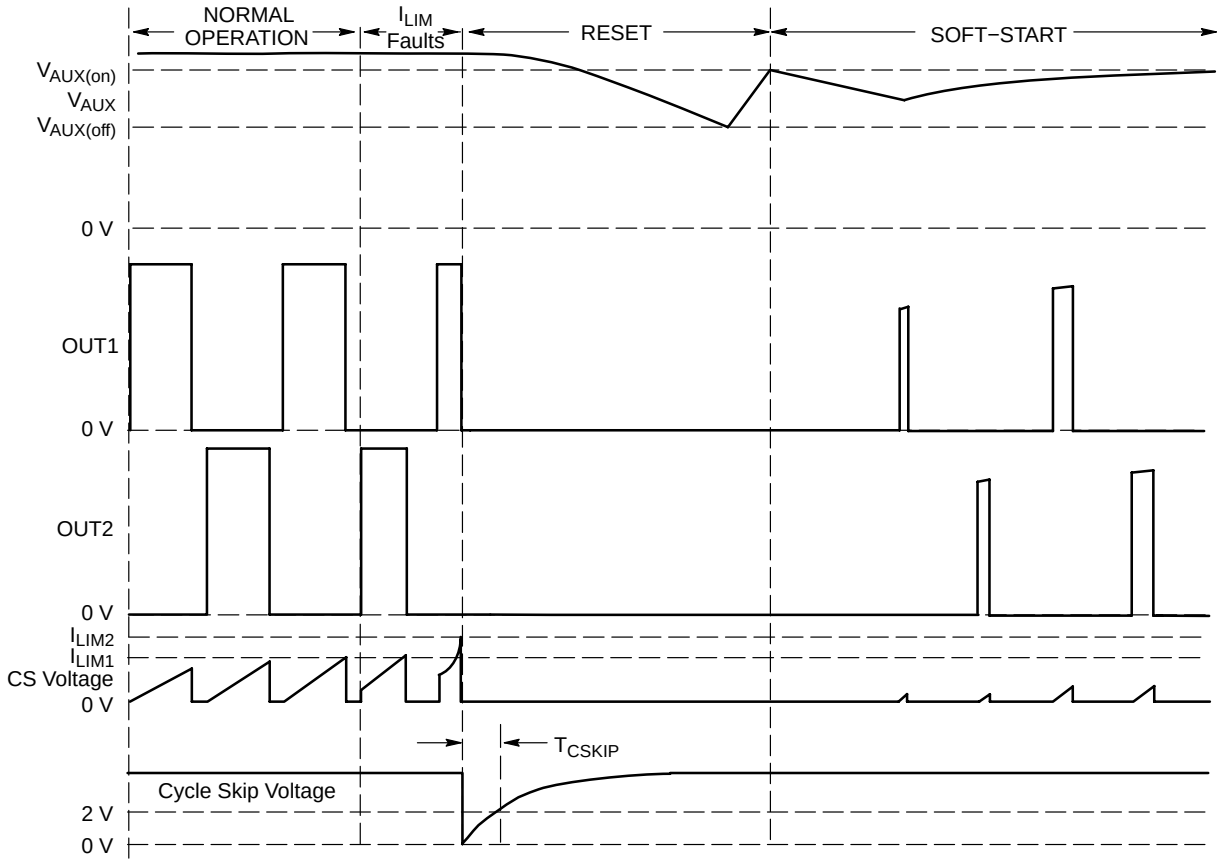


Figure 31. Overcurrent Faults Timing Diagram

Once the cycle skip period is complete and V_{AUX} reaches $V_{AUX(on)}$, a soft−start sequence commences. The possible minimum OFF time is set by C_{CSKIP}. The actual OFF time is generally greater than the cycle skip period if operating in DSS because it is the cycle skip period added to the time it takes V_{AUX} to cycle between $V_{AUX(off)}$ and $V_{AUX(on)}$. If operating from an independent supply, the OFF time is the cycle skip period.

Oscillator

The NCP1561 oscillator frequency is set by a single external resistor connected between the R_T pin and GND. The oscillator is designed to operate up to 250 kHz.

The voltage on the R_T pin is laser trim adjusted during manufacturing to 1.3 V for an R_T of 101 kΩ. A current set by R_T generates an Oscillator Ramp by charging an internal 10 pF capacitor as shown in Figure 3. The period ends (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. If R_T increases, the current and the Oscillator Ramp slope decrease, thus reducing the frequency. If R_T decreases, the opposite effect is obtained. Figure 17 shows the relationship between R_T and the oscillator frequency.

Maximum Duty Cycle

A dedicated internal comparator limits the maximum ON time by comparing the FF Ramp to $V_{DC(inv)}$ as shown in Figure 3. If the FF Ramp voltage exceeds $V_{DC(inv)}$, the output of the Max DC Comparator goes high. This will reset the Output Latch, thus turning OFF the outputs and limiting the duty cycle.

Duty cycle is defined as:

$$DC = \frac{t_{on}}{T} = t_{on} \times f$$

Therefore, the maximum ON time can be set to yield the desired DC if the operating frequency is known. The maximum ON time is set by adjusting the FF Ramp to reach $V_{DC(inv)}$ in a time equal to $t_{on(max)}$ as shown in Figure 32. The maximum ON time should be set for the minimum line voltage. As line voltage increases, the slope of the FF Ramp increases. This reduces the duty cycle below DC_{MAX}, which is a desirable feature as the duty cycle is inversely proportional to line voltage.

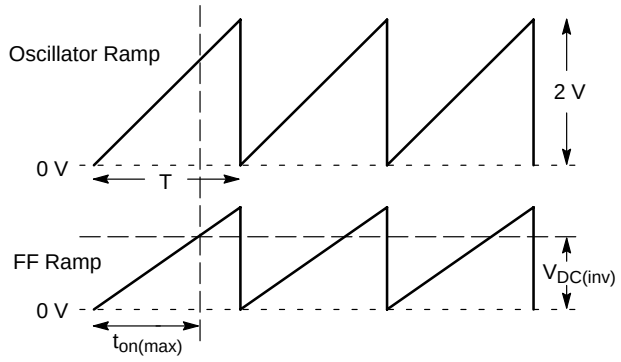


Figure 32. Maximum ON Time Limit Waveforms

An internal resistor divider from a 2.0 V reference is used to set $V_{DC(inv)}$. If the DC_{MAX} pin is grounded, $V_{DC(inv)}$ is 1.0 V. If the pin is floating, $V_{DC(inv)}$ is 1.4 V. This is equivalent to 71% (36% DC) or 100% (50% DC) of a FF Ramp, with a peak voltage of 1.4 V. $V_{DC(inv)}$ can be adjusted to other values by placing an external resistor network on the DC_{MAX} pin. For example, if the minimum line voltage is 36 V, R_{FF} is 432 kΩ, oscillator frequency is 150 kHz and a maximum duty cycle of 45% is required, $V_{DC(inv)}$ is calculated as follows:

$$V_{DC(inv)} = \frac{I_{FF} \times 6.7\ k\Omega \times t_{on(max)}}{C_{FF} \times 125\ k\Omega}$$

$$V_{DC(inv)} = \frac{81.0\ \mu A \times 6.7\ k\Omega \times 3.0\ \mu s}{10.8\ pF \times 125\ k\Omega} = 1.2\ V$$

This can be achieved by connecting a 23.44 kΩ resistor from the DC_{MAX} pin to GND. The maximum duty cycle limit can be disabled connecting a 100 kΩ resistor between the DC_{MAX} and V_{REF} pins.

5.0 V Reference

The NCP1561 includes a precision 5.0 V reference output. The reference output is biased directly from V_{AUX} and it can supply up to 6 mA. Load regulation is 50 mV and line regulation is 100 mV within the specified operating range.

It is recommended to bypass the reference output with a 0.1 μF ceramic capacitor. The reference output is disabled when an UV fault is present.

PWM Comparator

In steady state operation, the PWM Comparator adjusts the duty cycle by comparing the error signal to the FF Ramp (voltage−mode) or a ramp proportional to the inductor current (current−mode). The error signal is fed into the V_{EA} input. The FF Ramp or the inductor ramp is fed into the RAMP_IN pin. If operating in voltage−mode, the connection between the RAMP_OUT and RAMP_IN pins should be as close as possible to minimize parasitic inductance. It can be easily routed underneath the package.

The V_{EA} input can be driven directly with an optocoupler and a pull up resistor (R_{EA}) from V_{REF} as shown in Figure 33. The drive of the control pin is simplified by internally incorporating a series diode and resistor. The series diode provides a 0.7 V offset between the V_{EA} input and the PWM Comparator inverting input. The outputs are enabled if the V_{EA} voltage is approximately 0.7 V above the valley voltage of the ramp (V_{valley}) in the RAMP_IN pin.

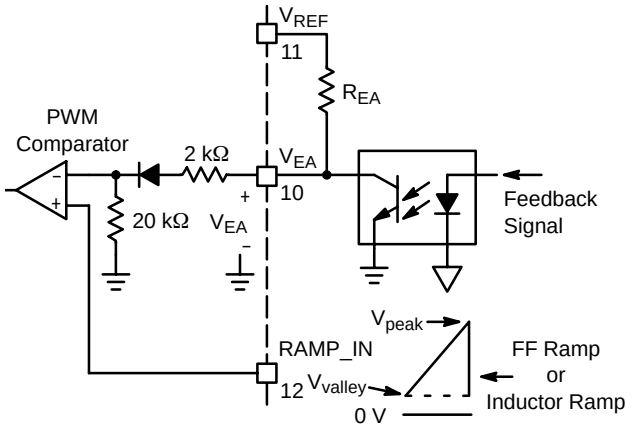


Figure 33. Optocoupler driving V_{EA} input

The pull−up resistor is selected such that in the absence of the error signal, the voltage on the V_{EA} pin exceeds the peak amplitude of the ramp in the RAMP_IN pin. Otherwise, the converter may not be able to reach maximum duty cycle. If operating in voltage−mode, R_{EA} is calculated using the equation below:

$$R_{EA} < 22\ k\Omega \left(\frac{V_{REF} - 0.7\ V}{V_{valley} + \frac{0.0515 \times I_{FF}}{C_{FF} \times f}} - 1 \right)$$

where, C_{FF} is the internal FF capacitor, typically 10.8 pF.

Soft−Start

Soft−start (SS) allows the converter to gradually reach steady state operation, thus reducing startup stress and surges on the system. The duty cycle is limited during a soft−start sequence by comparing the Oscillator Ramp to the SS voltage (V_{SS}) by means of the Soft−Start Comparator.

Once faults are removed and V_{AUX} reaches $V_{AUX(on)}$, a 6.2 μA current source starts to charge the capacitor on the SS pin. The Soft−Start Comparator controls the duty cycle while the SS voltage is below 2.0 V. Once V_{SS} reaches 2.0 V, it exceeds the Oscillator Ramp voltage and the Soft−Start Comparator does not limit the duty cycle. Figure 34 shows the relationship between the outputs duty cycle and the soft−start voltage.

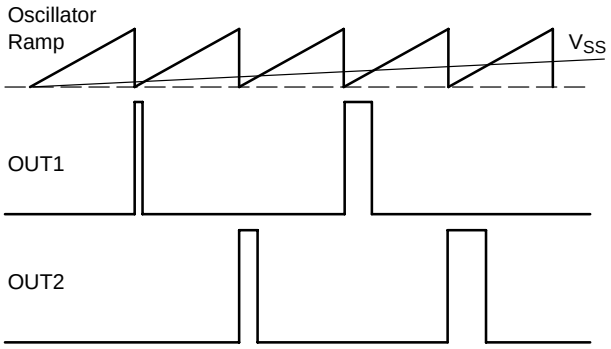


Figure 34. Soft Start Timing Diagram

If the soft start period is too long, V_{AUX} may discharge to 7 V before the converter output is completely in regulation causing the outputs to be disabled. If the converter output is not completely discharged when the outputs are re−enabled, the converter will eventually reach regulation exhibiting a non−monotonic startup behavior. But, if the converter output is completely discharged when the outputs are re−enabled, the cycle may repeat and the converter will not start.

In the event of an UV or cycle skip fault, the soft−start capacitor is discharged. Once the fault is removed, a soft−start cycle commences. The soft−start steady state voltage is approximately 4.1 V.

Control Outputs

The NCP1561 has two off−phase control outputs, OUT1 and OUT2. Figure 35 shows the relationship between OUT1 and OUT2.

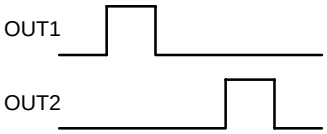


Figure 35. Control Outputs Timing Diagram

Once V_{AUX} reaches $V_{AUX(on)}$, the internal startup circuit is disabled and the One Shot Pulse Generator is enabled. If no faults are present, the outputs turn ON. Otherwise, the outputs remain OFF until the fault is removed and V_{AUX} reaches $V_{AUX(on)}$ again.

The control outputs are biased from V_{AUX}. The outputs can supply up to 10 mA each and their high state voltage is usually 0.2 V below V_{AUX}. Therefore, the auxiliary supply voltage should not exceed the maximum input voltage of the driver stage.

If the control outputs need to drive a large capacitive load, a driver should be used between the NCP1561 and the load. Figures 19 and 20 show the relationship between the output's rise and fall times vs capacitive load.

Thermal Protection

Internal Thermal Shutdown Circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 180°C, the controller is forced into a low power reset state, discharging the soft−start capacitor and disabling the output drivers and the bias regulator. Once the junction temperature falls below 163°C, the NCP1561 enters a soft−start mode and it is allowed to resume normal operation. This feature is provided to prevent catastrophic failures from accidental device overheating.

Application Information

A dc−dc converter for a 48 V telecom system is designed and implemented using the NCP1561. The converter delivers 125 W at 2.5 V and achieves a full load efficiency of 85%. The system is built using a 4 layer FR4, single sided board. The converter footprint is 3.25 in x 3.75 in. The components location within the board is shown in Figure 36 and the complete circuit schematic is shown in Figure 37. The Bill of Material is listed in Table 1. The layout files are available. Please contact your sales representative for more information.

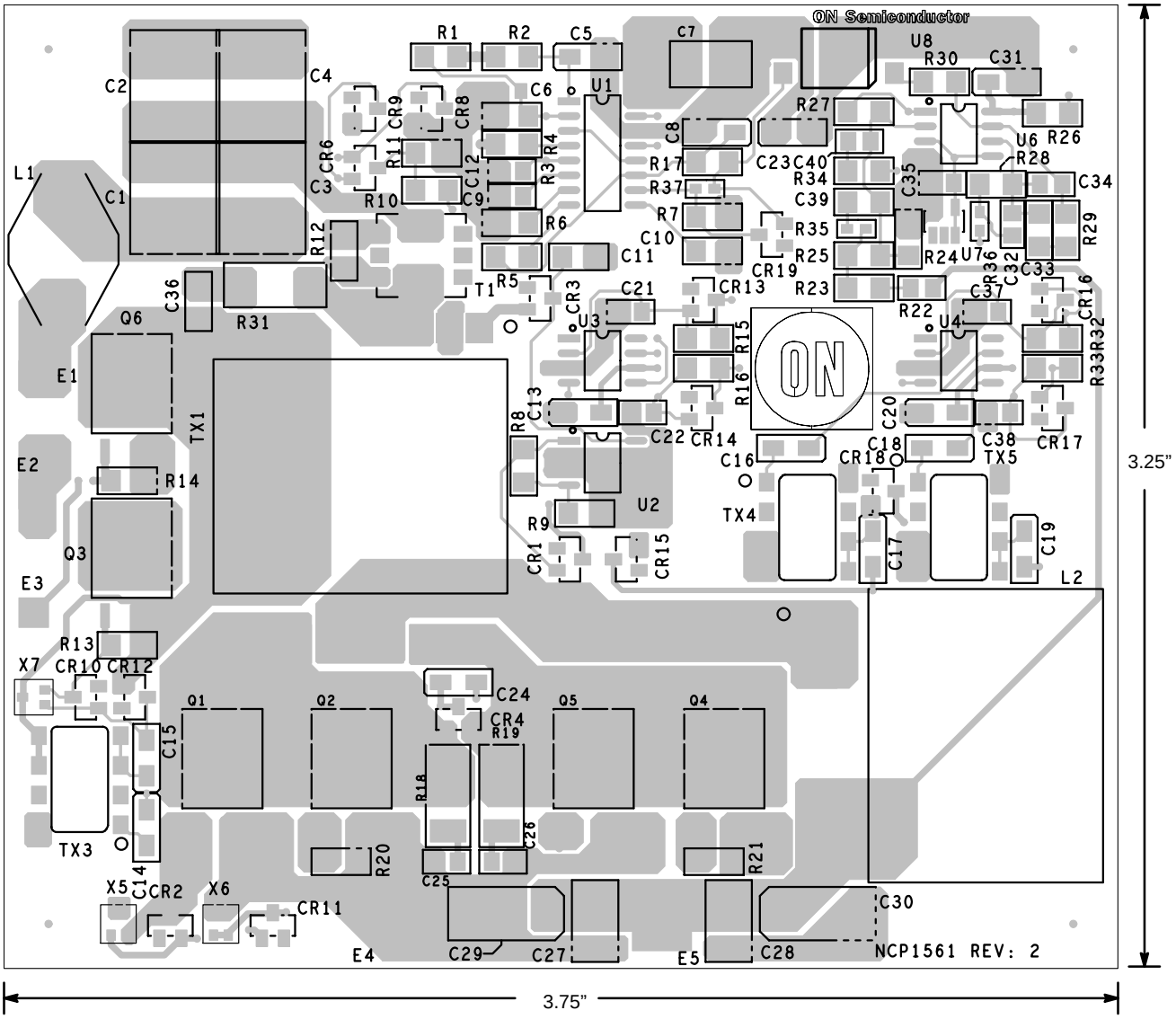


Figure 36. Demo Board Top View

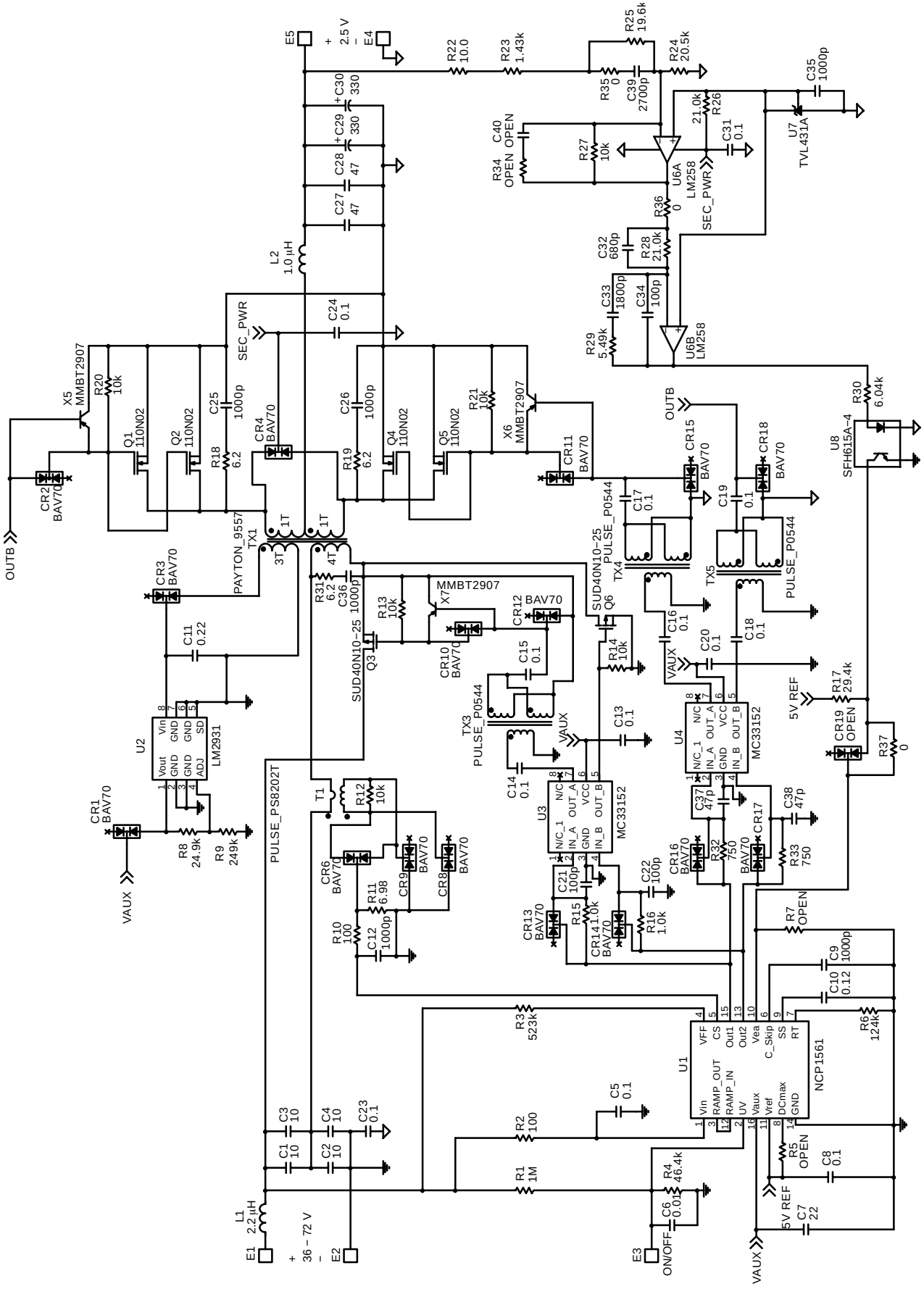


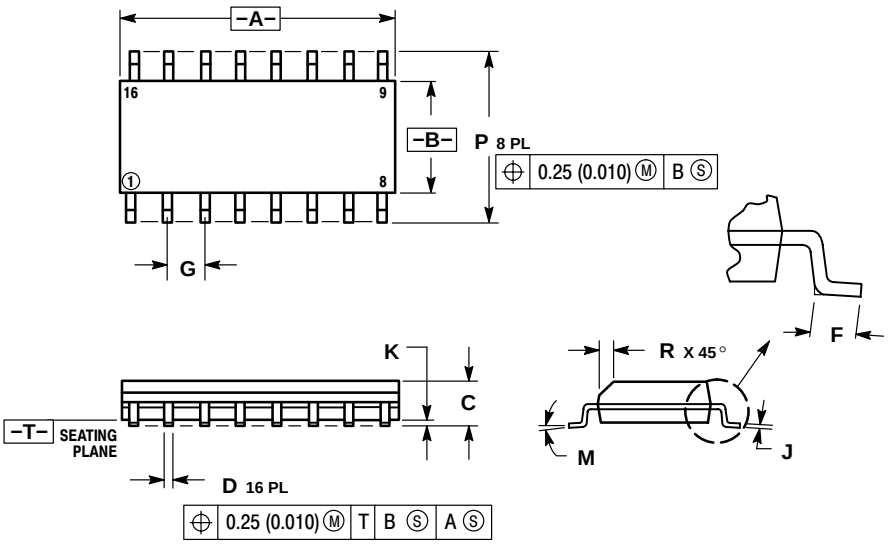
Figure 37. NCP1561 Demo Board Circuit Schematic

Table 1. NCP1561 Demo Board Bill of Material

Quantity	Part Reference	Part	Value	Vendor	Comments
4	C1−C4	C5750X7R1H106M	10 μF	TDK	50 V
13	C5, C8, C13−C20, C23, C24, C31	C3216X7R2A104K	0.1 μF	TDK	100 V
1	C6	C2012X7R1H103K	0.01 μF	TDK	50 V
1	C7	C4532X7R1C226MT	22 μF	TDK	16 V
5	C9, C12, C25, C26, C35	VJ0805A102KXBAT	1000 pF	Vishay (VITRAMON)	100 V
1	C10	VJ1206Y124KXXAT	0.12 μF	Vishay (VITRAMON)	25 V
1	C11	C3216X7R1H224KT	0.22 μF	TDK	25 V
3	C21, C22, C34	VJ0805A101KXBAT	100 pF	Vishay (VITRAMON)	100 V
2	C27, C28	C4532X5R0J476M	47 μF	TDK	6.3 V
2	C29, C30	T495X337K006AS	330 μF	KEMET	6 V
1	C32	VJ0805A681KXBAT	680 pF	Vishay (VITRAMON)	100 V
1	C33	VJ1206A182KXBAT	1800 pF	Vishay (VITRAMON)	100 V
1	C36	VJ1206A102KXBAT	1000 pF	Vishay (VITRAMON)	100 V
2	C37, C38	VJ0805A470KXBAT	47 pF	Vishay (VITRAMON)	100 V
1	C39	VJ1206A272KXBAT	2700 pF	Vishay (VITRAMON)	100 V
1	C40	−	OPEN	−	OPEN
16	CR1−CR4, CR6, CR8−CR18	BAV70LT1	−	ON Semiconductor	Dual Diode
1	CR19	−	OPEN	−	OPEN
1	L1	DO3316P−222	2.2 μH	COILCRAFT	
1	L2	9558	1.0 μH	PAYTON	
4	Q1, Q2, Q4, Q5	NTD110N02R	−	ON Semiconductor	24 V, N−MOSFET
2	Q3, Q6	SUD40N10−25	−	VISHAY	100 V, N−MOSFET
1	R1	CRCW12061004FRE4	1M	Vishay (DALE)	1%
2	R2, R10	CRCW1206101JRT1	100	Vishay (DALE)	5%
1	R3	CRCW12065233FRT1	523k	Vishay (DALE)	1%
1	R4	CRCW12064642FRT1	46.4k	Vishay (DALE)	1%
3	R5, R7, R34	−	OPEN	−	OPEN
1	R6	CRCW12061243FRT1	124k	Vishay (DALE)	1%
1	R9	CRCW12062493FRT1	249k	Vishay (DALE)	1%
5	R12, R13, R14, R20, R21	CRCW1206103JRT1	10k	Vishay (DALE)	5%
1	R8	CRCW12062492FRT1	24.9k	Vishay (DALE)	1%
1	R11	CRCW12066R98FRT1	6.98	Vishay (DALE)	1%
2	R15, R16	CRCW12061001FRT1	1.0k	Vishay (DALE)	1%
1	R17	CRCW12062942FRT1	29.4k	Vishay (DALE)	1%
3	R18, R19, R31	CRCW25126R19FRT1	6.2	Vishay (DALE)	5%
1	R22	CRCW080510R0FRT1	10	Vishay (DALE)	1%
1	R23	CRCW12061431FRT1	1.43k	Vishay (DALE)	1%
1	R24	CRCW12062052FRT1	20.5k	Vishay (DALE)	1%
1	R25	CRCW12061962FRT1	19.6k	Vishay (DALE)	1%
2	R26, R28	CRCW12062102FRT1	21.0k	Vishay (DALE)	1%
1	R27	CRCW1206103JRT1	10k	Vishay (DALE)	5%
1	R29	CRCW12065491FRT1	5.49k	Vishay (DALE)	1%
1	R30	CRCW12066041FRT1	6.04k	Vishay (DALE)	1%
	R32, R33	CRCW12067500FRT1	750	Vishay (DALE)	1%
3	R35−R37	CRCW0603000ZT	0	Vishay (DALE)	5%
1	T1	PS8202T	−	PULSE	Current Sense Transformer
1	TX1	9557	−	PAYTON	Power Transformer
3	TX3−TX5	P0544	−	PULSE	Gate Drive Transformer
1	U1	NCP1561DR2	−	ON Semiconductor	Controller
1	U2	LM2931CD	−	ON Semiconductor	Voltage Regulator
2	U3, U4	MC33152D	−	ON Semiconductor	MOSFET Driver
1	U6	LM258D	−	ON Semiconductor	Dual OpAmp
1	U7	TVL431ASNT1	−	ON Semiconductor	Regulator
1	U8	SFH6156−4	−	VISHAY	Poptocoupler
3	X5−X7	MMBT2907AWT1	−	ON Semiconductor	PNP transistor

PACKAGE DIMENSIONS

SO−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

The product described herein (NCP1561) may be covered by one or more U.S. patents. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Japan: ON Semiconductor, Japan Customer Focus Center
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For additional information, please contact your local Sales Representative.

NCP1561/D