PHOTO IC COUPLER

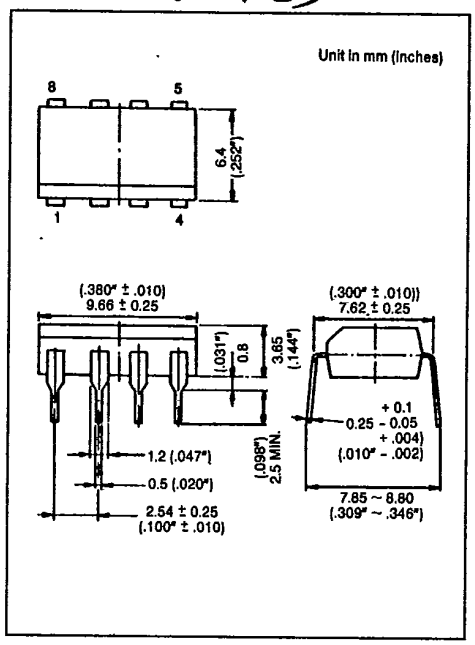
T-41-83

MT25300, MT25310

APPLICATIONS

- DIGITAL LOGIC ISOLATION
- LINE RECEIVER
- POWER SUPPLY CONTROL
- SWITCHING POWER SUPPLY
- TRANSISTOR INVERTER

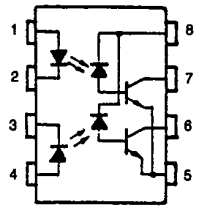
The MARKTECH MT25300 and MT25310 dual photocouplers consist of a pair of GaAlAs light emitting diodes and integrated photodetector. This unit is 8-lead DIP package. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.



FEATURES

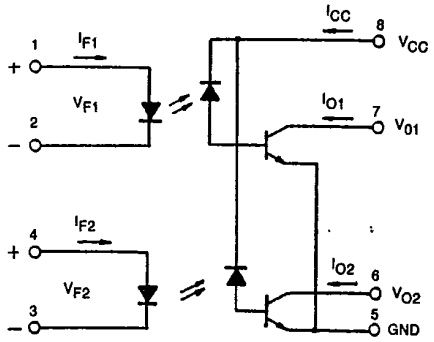
- TTL Compatible
- Switching Speed : t_{pHL}, t_{pLH}=0.3μs (Typ.) (@R_L=1.9kΩ)
- Guaranteed Performance Over Temp. : 0 ~ 70°C
- Isolation Voltage : 2500 V_{rms} Min.

PIN CONFIGURATION (TOP VIEW)



1: ANODE .1
2: CATHODE .1
3: CATHODE .2
4: ANODE .2
5: GND
6: V_{O2} (OUTPUT 2)
7: V_{O1} (OUTPUT 1)
8: V_{CC}

SCHEMATIC



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RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	0	—	12	V
Forward Current, Each Channel	I_F	—	16	25	mA
Operating Temperature	T_{opr}	-25	—	85	°C

ABSOLUTE MAXIMUM RATINGS

	CHARACTERISTIC	SYMBOL	RATING	UNIT
LED	Forward Current (Each channel, Note 1)	I_F	25	mA
	Pulse Forward Current (Each channel, Note 2)	I_{FP}	50	mA
	Total Pulse Forward Current (Each channel, Note 3)	I_{FPT}	1	A
	Reverse Voltage (Each channel)	V_R	5	V
	Diode Power Dissipation (Each channel, Note 4)	P_D	45	mW
DETECTOR	Output Current (Each channel)	I_O	8	mA
	Peak Output Current (Each channel)	I_{OP}	16	mA
	Supply Voltage	V_{CC}	-0.5 ~ 15	V
	Output Voltage (Each channel)	V_O	-0.5 ~ 15	V
	Output Power Dissipation (Each channel, Note 5)	P_o	35	mW
Operating Temperature Range		T_{opr}	-55 ~ 100	°C
Storage Temperature Range		T_{stg}	-55 ~ 125	°C
Lead Solder Temperature (10 sec.) **		T_{sold}	260	°C
Isolation Voltage (AC, 1 min., R.H. ≤ 60%, Note 7)		BV_S	2500	V_{rms}

Note 1: Derate 0.8mA above 70°C.

Note 2: 50% duty cycle, 1ms pulse width. Derate 1.6mA/°C above 70°C.

Note 3: Pulse width 1μs, 300pps.

Note 4: Derate 0.9mW/°C above 70°C.

Note 5: Derate 1mW/°C above 70°C.

** 1.6mm below seating plane.

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ELECTRICAL CHARACTERISTICS
Over Recommended Temperature (Ta=0°C ~ 70°C, Unless otherwise noted).

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.**	MAX.	UNIT
Current Transfer Ratio (Each channel)	MT25300	CTR	I_F=16mA, V_O=0.4V	7	30	—	%
	MT25310		V_{CC}=4.5V, Ta=25°C (Note 6)	19	30	—	
	MT25300	CTR	I_F=16mA, V_O=0.5V	5	—	—	%
	MT25310		V_{CC}=4.5V (Note 6)	15	—	—	
Logic Low Output Voltage (Each channel)	MT25300	V_{OL}	I_F=16mA, I_O=1.1mA	—	0.1	0.4	V
			V_{CC}=4.5V				
	MT25310		I_F=16mA, I_O=2.4mA	—	0.1	0.4	V
			V_{CC}=4.5V				
Logic High Output Current (Each channel)		I_{OH}	I_F=0mA, V_O=V_{CC}=5.5V	—	3	500	nA
			Ta=25°C				
			I_F=0mA, V_O=V_{CC}=15V	—	—	50	μA
Logic Low Supply Current		I_{CCL}	I_{F1}=I_{F2}=16mA	—	160	—	μA
			V_{O1}=V_{O2}=Open, V_{CC}=15V				
Logic High Supply Current		I_{CCH}	I_{F1}=I_{F2}=0mA,	—	0.05	4	μA
			V_{O1}=V_{O2}=Open, V_{CC}=15V				
Input Forward Voltage (Each channel)		V_F	I_F=16mA, Ta=25°C	—	1.65	1.7	V
Temperature Coefficent of Forward Voltage (Each channel)		$\frac{\Delta V_F}{\Delta Ta}$	I_F=16mA	—	-2	—	mV/°C
Input Reverse Breakdown Voltage (Each channel)		BV_R	I_R=10μA, Ta=25°C	5	—	—	V
Input Capacitance (Each channel)		C_{IN}	f=1MHz, V_F=0	—	60	—	pF
Input-Output Insulation Leakage Current		I_{I-O}	Relative Humidity=45%	—	—	1.0	μA
			t=5s, V_{I-O}=3000V_{dc},				
			Ta=25°C (Note 7)				
Resistance (Input-Output)		R_{I-O}	V_{I-O}=500V_{dc}, (Note 7)	—	10^{12}	—	Ω
Capacitance (Input-Output)		C_{I-O}	f=1MHZ (Note 7)	—	0.6	—	pF
Input-Input Leakage Current		I_{I-I}	Relative Humidity=45%	—	0.005	—	μA
			t=5s, V_{I-I}=500V (note 8)				
Resistance (Input-Input)		R_{I-I}	V_{I-I}=500V_{dc}, (Note 8)	—	10^{11}	—	Ω
Capacitance (Input-Input)		C_{I-I}	f=1MHZ (Note 8)	—	0.25	—	pF

**All typicals Ta=25°C.

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SWITCHING SPECIFICATIONS
(Unless otherwise specified, Ta=25°C, V_{CC}=5V, I_F=16mA)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to Logic Low at Output (Each channel)	MT25300	t_{pHL}	1	R_L=4.1kΩ	—	0.3	1.5	μs
	MT25310			R_L=1.9kΩ	—	0.2	0.8	
Propagation Delay Time to Logic High at Output (Each channel)	MT25300	t_{pLH}	1	R_L=4.1kΩ	—	0.5	1.5	μs
	MT25310			R_L=1.9kΩ	—	0.3	0.8	
Common Mode Transient Immunity at Logic High Level Output (Each channel, Note 9)	MT25300	C_{MH}	2	I_F=0mA, V_{CM}=400Vp-p R_L=4.1kΩ	—	1000	—	V/μs
	MT25310			I_F=0mA, V_{CM}=400Vp-p R_L=1.9kΩ	—	1000	—	
Common Mode Transient Immunity at Logic Low Level Output (Each Channel, Note 9)	MT25300	C_{ML}	2	V_{CM}=400Vp-p R_L=4.1kΩ, I_F=16mA	—	-1000	—	V/μs
	MT25310			V_{CM}=400Vp-p R_L=1.9kΩ, I_F=16mA	—	-1000	—	
Bandwidth (Each channel, Note 10)		BW	3	R_L=100Ω	—	2	—	MHz

Note 6: DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

Note 7: Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.

Note 8: Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Note 9: Common mode transient immunity in Logic High level is the maximum tolerable (Positive) dVcm/dt on the leading edge of the common mode pulse, Vcm, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V).
Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dVcm/dt on the trailing edge of the common mode pulse signal, Vcm, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).

Note 10: The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

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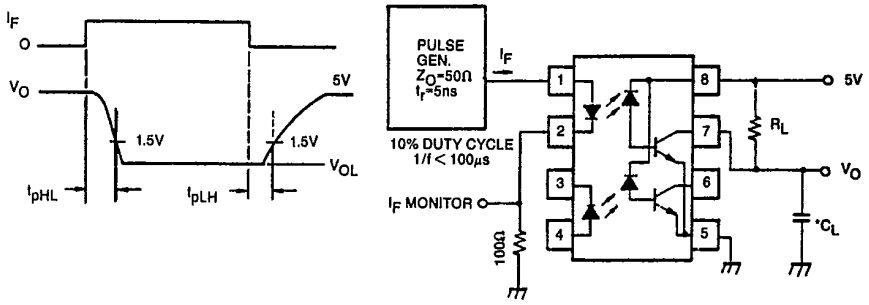
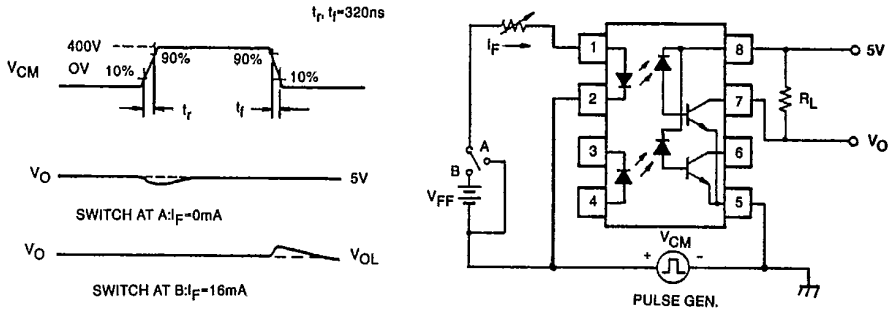
TEST CIRCUIT 1: SWITCHING TIME, t_{pHL}, t_{pLH}

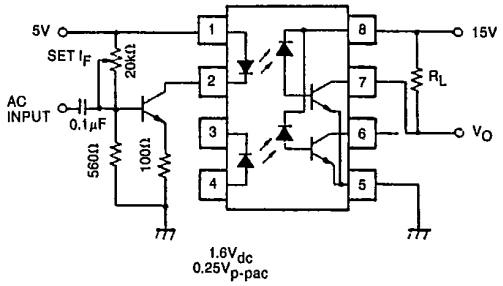


*C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2: TRANSIENT IMMUNITY AND TYPICAL WAVEFORM



TEST CIRCUIT 3: FREQUENCY RESPONCE



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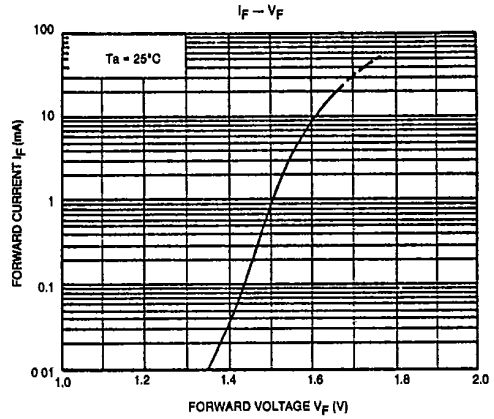
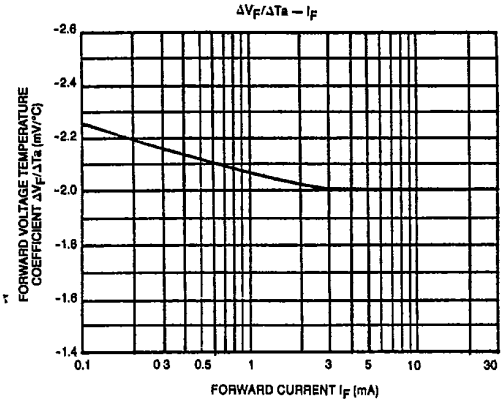
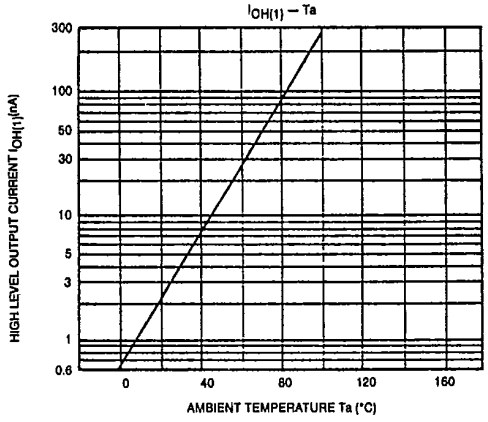
$I_F - V_F$



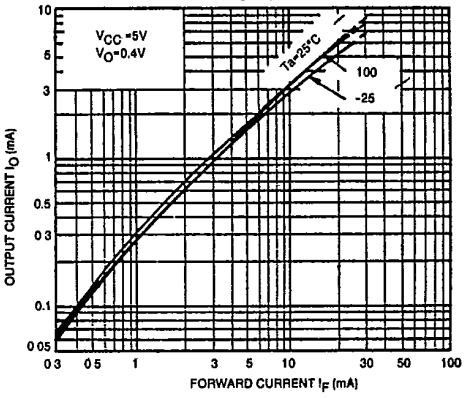
$\Delta V_F/\Delta Ta - I_F$



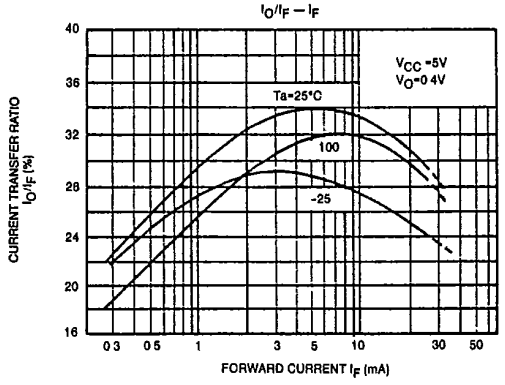
$I_{OH(1)} - Ta$



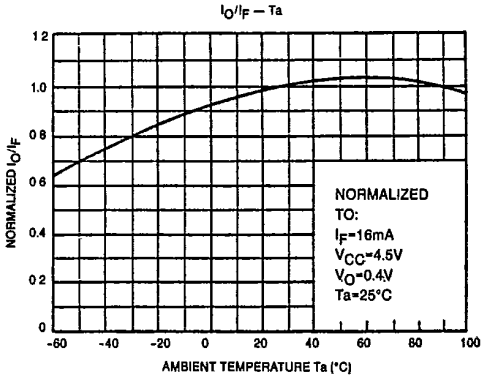
$I_O - I_F$



$I_O/I_F - I_F$



$I_O/I_F - Ta$



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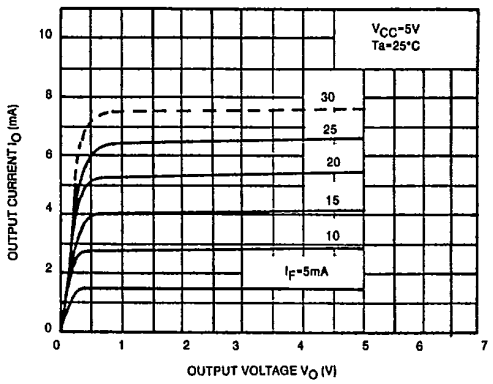
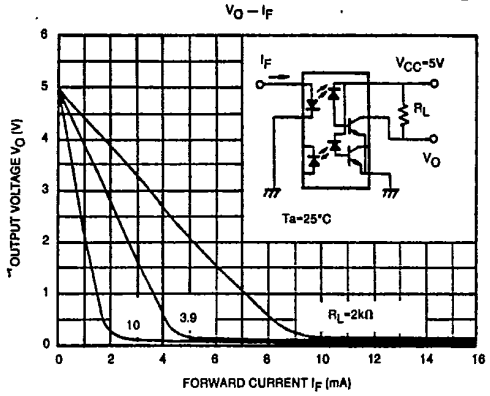
$I_O - V_O$



$V_O - I_F$



$t_{pHL}, t_{pLH} - R_L$