Document Title

256Kx18-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial draft	May. 15. 1997	Preliminary
0.1	Modify power down cycle timing & Interleaved read timing, Insert Note 4 at AC timing characteristics. Change I_{SB1} value from 10mA to 30mA. Change I_{SB2} value from 10mA to 20mA.	February. 11. 1998	Preliminary
0.2	Change Undershoot spec from -3.0V(pulse width≤20ns) to -2.0V(pulse width≤t_{CYC}/2) Add Overshoot spec 4.6V((pulse width≤t_{CYC}/2) Change V_{IH} max from 5.5V to V_{DD}+0.5V	April. 14. 1998	Preliminary
0.3	Change I_{SB2} value from 20mA to 30mA. Change V_{DD} condition from V_{DD}=3.3V+10%/-5% to V_{DD}=3.3V+0.3V/-0.165V.	May 13. 1998	Preliminary
1.0	Final spec Release	May 15. 1998	Final
2.0	Add V_{DDQ} Supply voltage(2.5V)	Dec. 02. 1998	Final

256Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V+0.3V/-0.165V Power Supply.
- V_{DDQ} Supply Voltage 3.3V+0.3V/-0.165V for 3.3V I/O
  or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a
  linear burst.
- Three Chip Enables for simple depth expansion with No Data
  Contention.
- TTL-Level Three-State Output.
- 100-TQFP-1420A

FAST ACCESS TIMES

PARAMETER	Symbol	-7	-8	-9	Unit
Cycle Time	t_{CYC}	8.5	10	12	ns
Clock Access Time	t_{CD}	7.5	8	9	ns
Output Enable Access Time	t_{OE}	3.5	3.5	3.5	ns

GENERAL DESCRIPTION

The KM718V887 is a 4,718,592 bit Synchronous Static Random Access Memory designed for support zero wait state performance for advanced Pentium/Power PC address pipelining. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signal.

It is organized as 256K words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementation of high performance cache RAM applications.
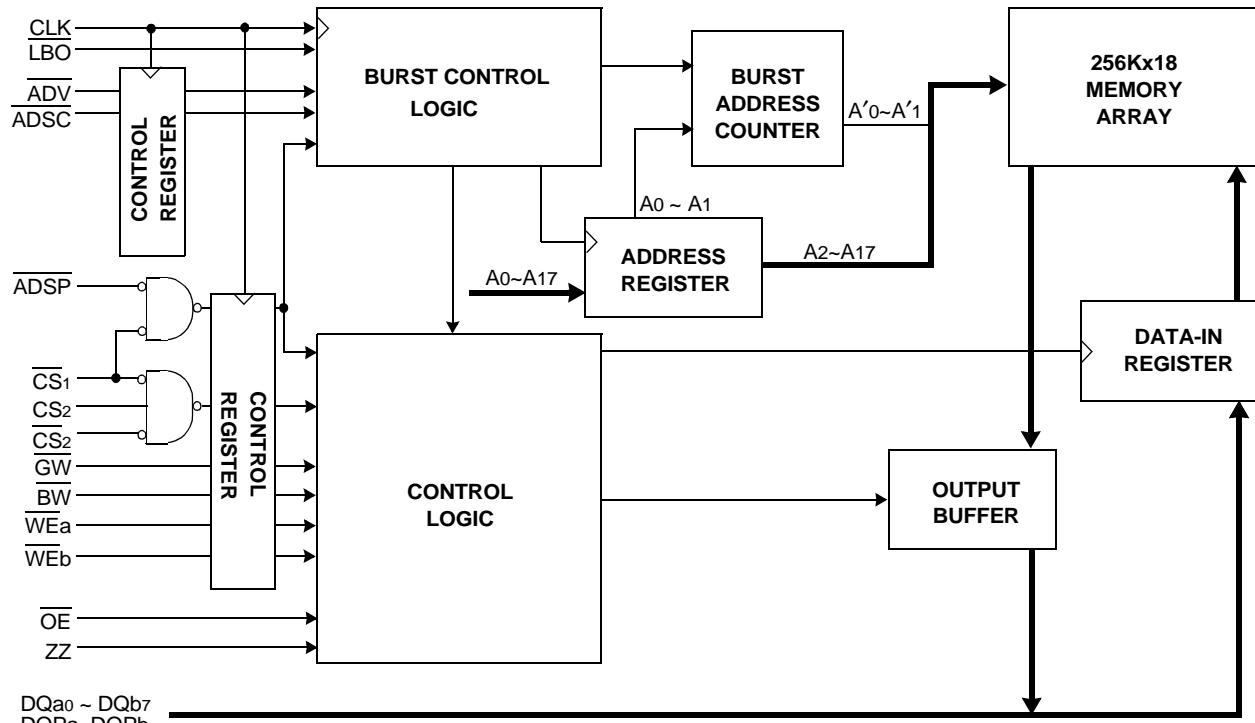
Write cycles are internally self-timed and synchronous.
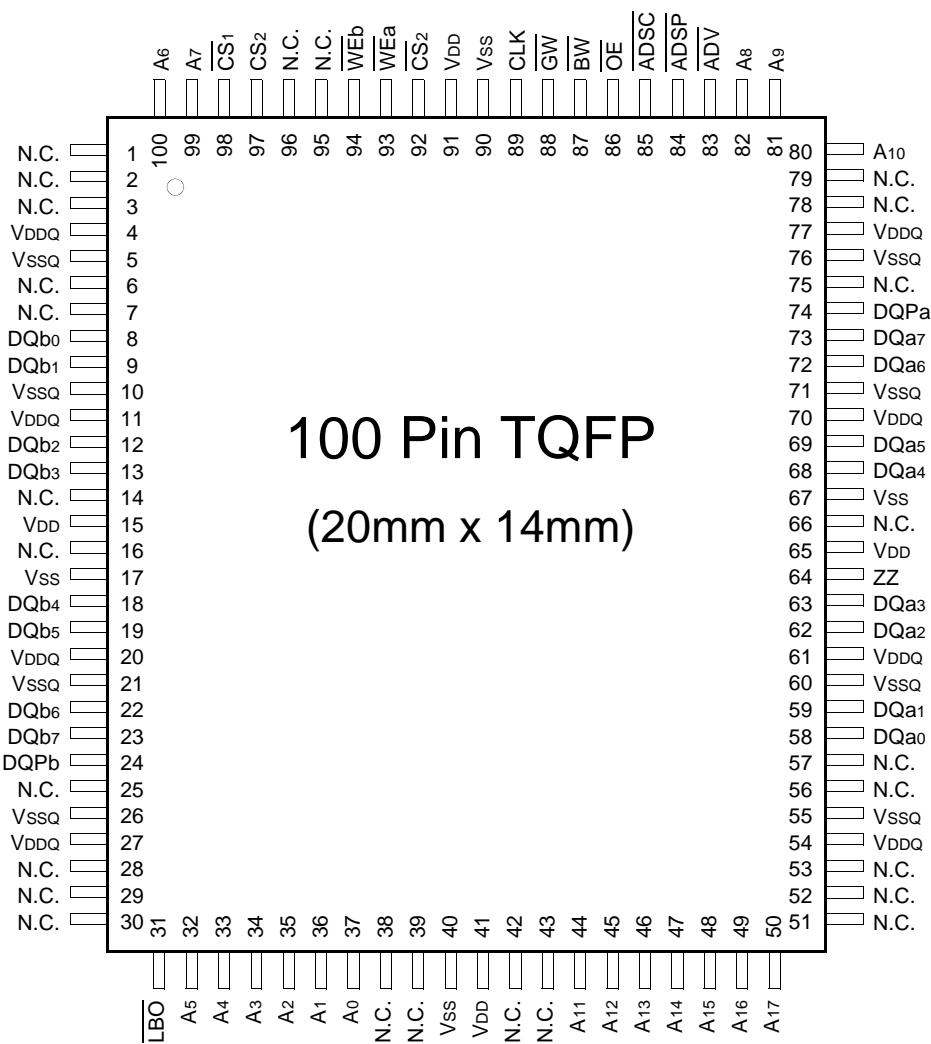
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input. ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM718V887 is implemented in SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM

December 1998
Rev. 2.0

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PIN CONFIGURATION(TOP VIEW)

100 Pin TQFP

(20mm x 14mm)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{17}	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 50,80,81,82,99,100	V_{DD} V_{SS} N.C.	Power Supply(+3.3V) Ground No Connect	15,41,65,91 17,40,67,90 1,2,3,6,7,14,16,25,28,
$\overline{ADV}$	Burst Address Advance	83			29,30,38,39,42,43,51
$\overline{ADSP}$	Address Status Processor	84			52,53,56,57,66,75
ADSC	Address Status Controller	85			78,79,95,96
CLK	Clock	89	DQa_0~a_7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_1}$	Chip Select	98	DQb_0~b_7		8,9,12,13,18,19,22,23
CS_2	Chip Select	97	DQPa, Pb		74,24
$\overline{CS_2}$	Chip Select	92	V_{DDQ}	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94		(2.5V or 3.3V)	
$\overline{OE}$	Output Enable	86	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

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FUNCTION DESCRIPTION

The KM718V887 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSP, ADSC, ADV and Chip Select pins.

When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP(or ADSC) using the new external address clocked into the on-chip address register when both GW and BW are high or when BW is low and both WEa and WEb are high, When ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE, the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with ADSP(or ADSC)and are differentiated into two kinds of operations; All byte write operation and individual byte write operation. All byte write occurs by enabling GW(in dependent of BW and WEx.), and individual byte write is performed only when GW is High and BW is Low. WEa controls DQa0 ~ DQa7 and DQPa, WEb controls DQb0 ~ DQb7 and DQPb.

CS1 is used to enable the device and conditions internal use of ADSP and is sampled only when a new external address is loaded.

ADV is ignored at the clock edge when ADSP is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when ADV is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	ZZ	OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

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SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	ADSP	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	None	Not Selected
L	L	X	L	X	X	X	↑	None	Not Selected
L	X	H	L	X	X	X	↑	None	Not Selected
L	L	X	X	L	X	X	↑	None	Not Selected
L	X	H	X	L	X	X	↑	None	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.

   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ}+0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C≤ T_A≤70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	3.135	3.3	3.6	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDI-	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(T$_A$=0 to 70°C, V$_{DD}$=3.3V+0.3V/-0.165V)
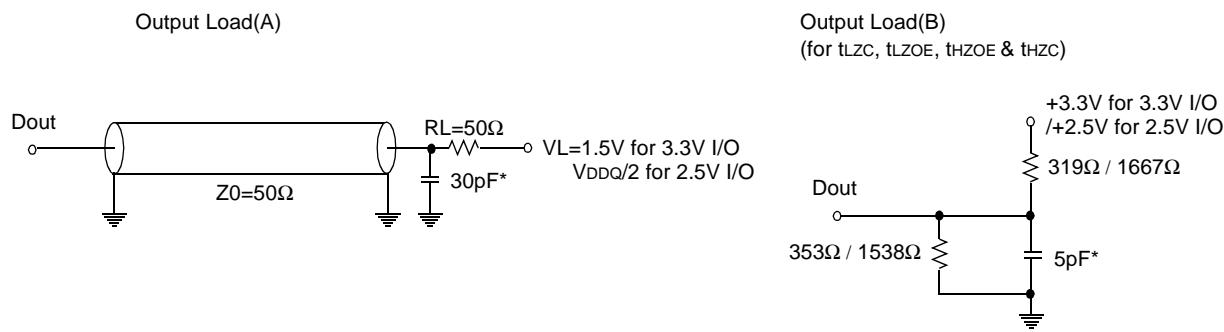
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Input Leakage Current(except ZZ)	I$_{IL}$	V$_{DD}$=Max ; V$_{IN}$=V$_{SS}$ to V$_{DD}$		-2	2	μA
Output Leakage Current	I$_{OL}$	Output Disabled, V$_{OUT}$=V$_{SS}$ to V$_{DDQ}$		-2	2	μA
Operating Current	I$_{CC}$	Device Selected, I$_{OUT}$=0mA, ZZ≤V$_{IL}$, All Inputs=V$_{IL}$ or V$_{IH}$ Cycle Time ≥ tcYC Min	-7	-	350	mA
			-8	-	325	
			-9	-	300	
Standby Current	I$_{SB}$	Device deselected, I$_{OUT}$=0mA, ZZ≤V$_{IL}$, f=Max, All Inputs≤0.2V or ≥ V$_{DD}$-0.2V	-7	-	100	mA
			-8	-	90	
			-9	-	80	
	I$_{SB1}$	Device deselected, I$_{OUT}$=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V$_{DD}$-0.2V or 0.2V)		-	30	mA
	I$_{SB2}$	Device deselected, I$_{OUT}$=0mA, ZZ≥V$_{DD}$-0.2V, f=Max, All Inputs≤V$_{IL}$ or ≥V$_{IH}$		-	30	mA
Output Low Voltage(3.3V I/O)	V$_{OL}$	I$_{OL}$ = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	V$_{OH}$	I$_{OH}$ = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	V$_{OL}$	I$_{OL}$ = 1.0mA		-	0.4	V
Output High Voltage(2.5V I/O)	V$_{OH}$	I$_{OH}$ = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	V$_{IL}$			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V$_{IH}$			2.0	V$_{DD}$+0.5**	V
Input Low Voltage(2.5V I/O)	V$_{IL}$			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V$_{IH}$			1.7	V$_{DD}$+0.5**	V

*   V$_{IL}$(Min)=-2.0(Pulse Width ≤ tCYC/2)

** V$_{IH}$(Max)=4.6(Pulse Width ≤ tCYC/2)

** In Case of I/O Pins, the Max. V$_{IH}$=V$_{DDQ}$+0.5V

TEST CONDITIONS
(V$_{DD}$=3.3V+0.3V/-0.165V,V$_{DDQ}$=3.3V+0.3/-0.165V or V$_{DD}$=3.3V+0.3V/-0.165V,V$_{DDQ}$=2.5V+0.4V/-0.125V, T$_A$=0 to 70°C)

| PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V$_{DDQ}$/2
Output Load	See Fig. 1

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Output Load(A)

Output Load(B)
(for tLZC, tLZOE, tHZOE & tHZC)

* Capacitive Load consists of all components of
  the test environment.

* Including Scope and Jig Capacitance
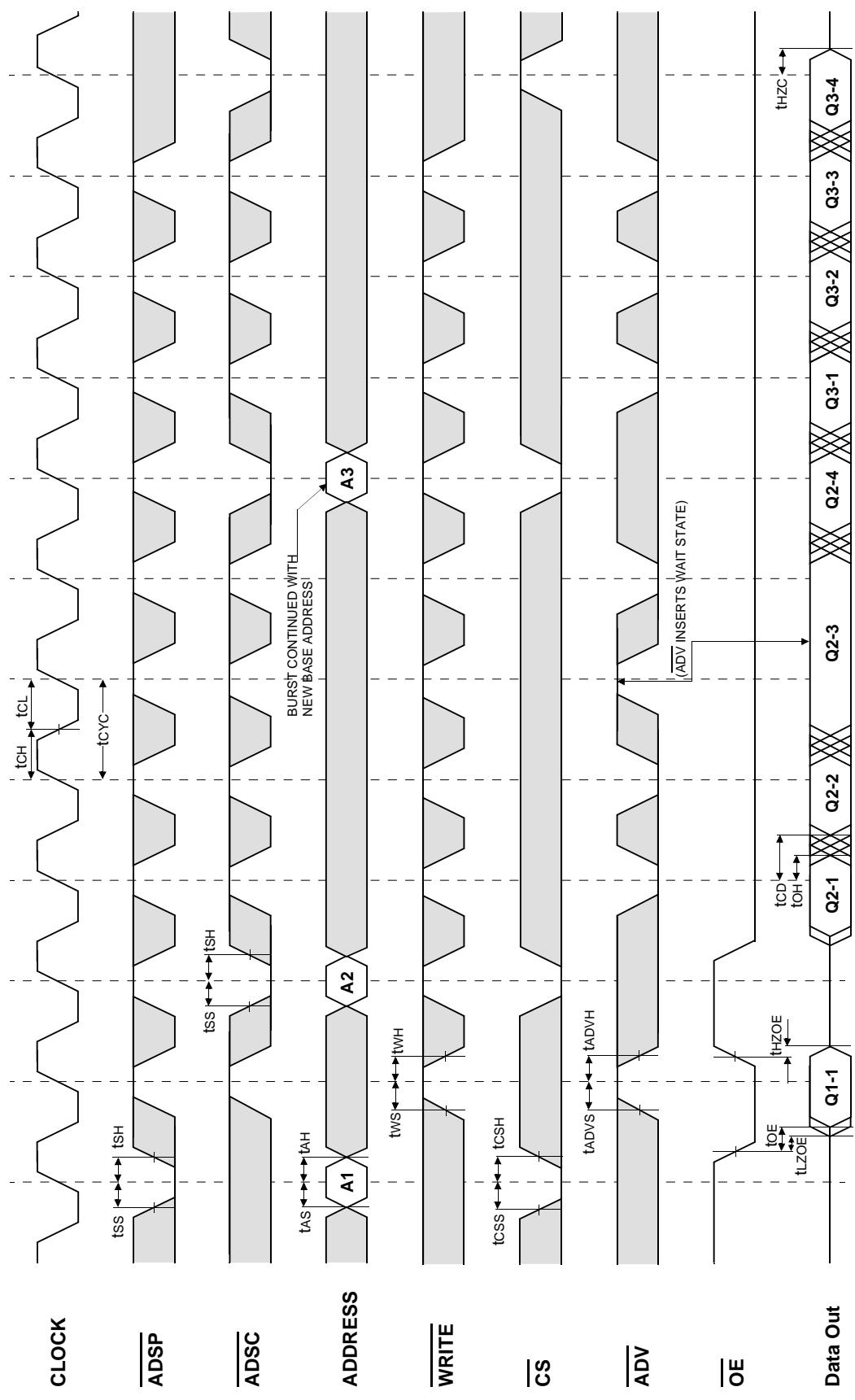
Fig. 1

AC TIMING CHARACTERISTICS(TA=0 to 70°C, VDD=3.3V+0.3V/-0.165V)

PARAMETER	SYMBOL	KM718V887-7		KM718V887-8		KM718V887-9		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	8.5	-	10	-	12	-	ns
Clock Access Time	tCD	-	7.5	-	8	-	9	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.5	-	3.5	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	2	-	2	-	2	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	3.5	-	3.5	ns
Clock High to Output High-Z	tHZC	2	3.5	2	3.5	2	3.5	ns
Clock High Pulse Width	tCH	3	-	4	-	4.5	-	ns
Clock Low Pulse Width	tCL	3	-	4	-	4.5	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High(GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and
CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.
4. At any given voltage and temperature, tHZC is less than tLZC.

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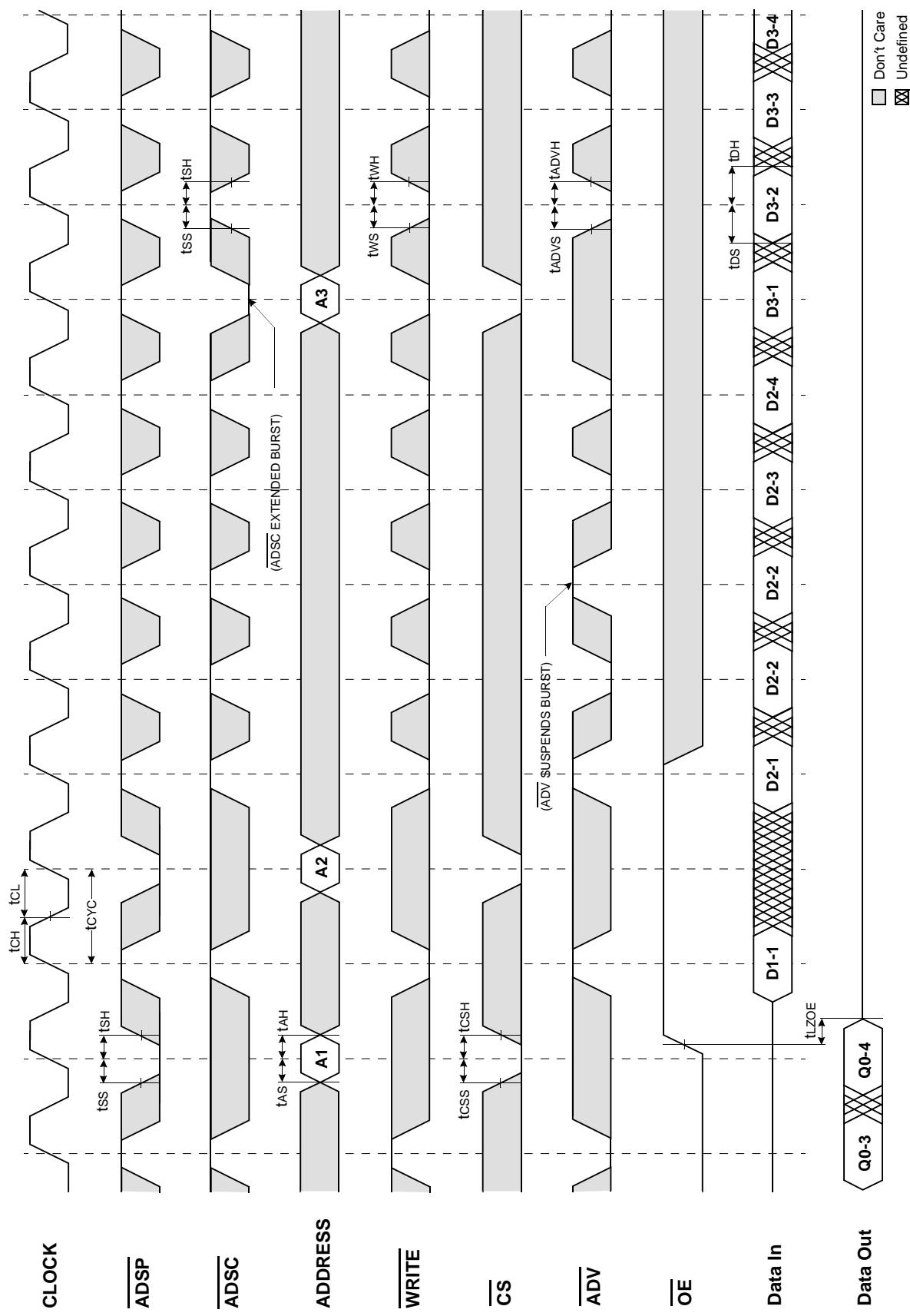
## TIMING WAVEFORM OF READ CYCLE

CLOCK

ADSP

ADSC

ADDRESS — A1, A2, A3

WRITE

CS

ADV

OE

Data Out — Q1-1, Q2-1, Q2-2, Q2-3, Q2-4, Q3-1, Q3-2, Q3-3, Q3-4

tSS, tSH, tCH, tCL, tCYC

tAS, tAH

tWS, tWH

tCSS, tCSH

tADVS, tADVH

tOE, tLZOE, tHZOE

tCD, tOH, tHZC

BURST CONTINUED WITH NEW BASE ADDRESS

(ADV INSERTS WAIT STATE)
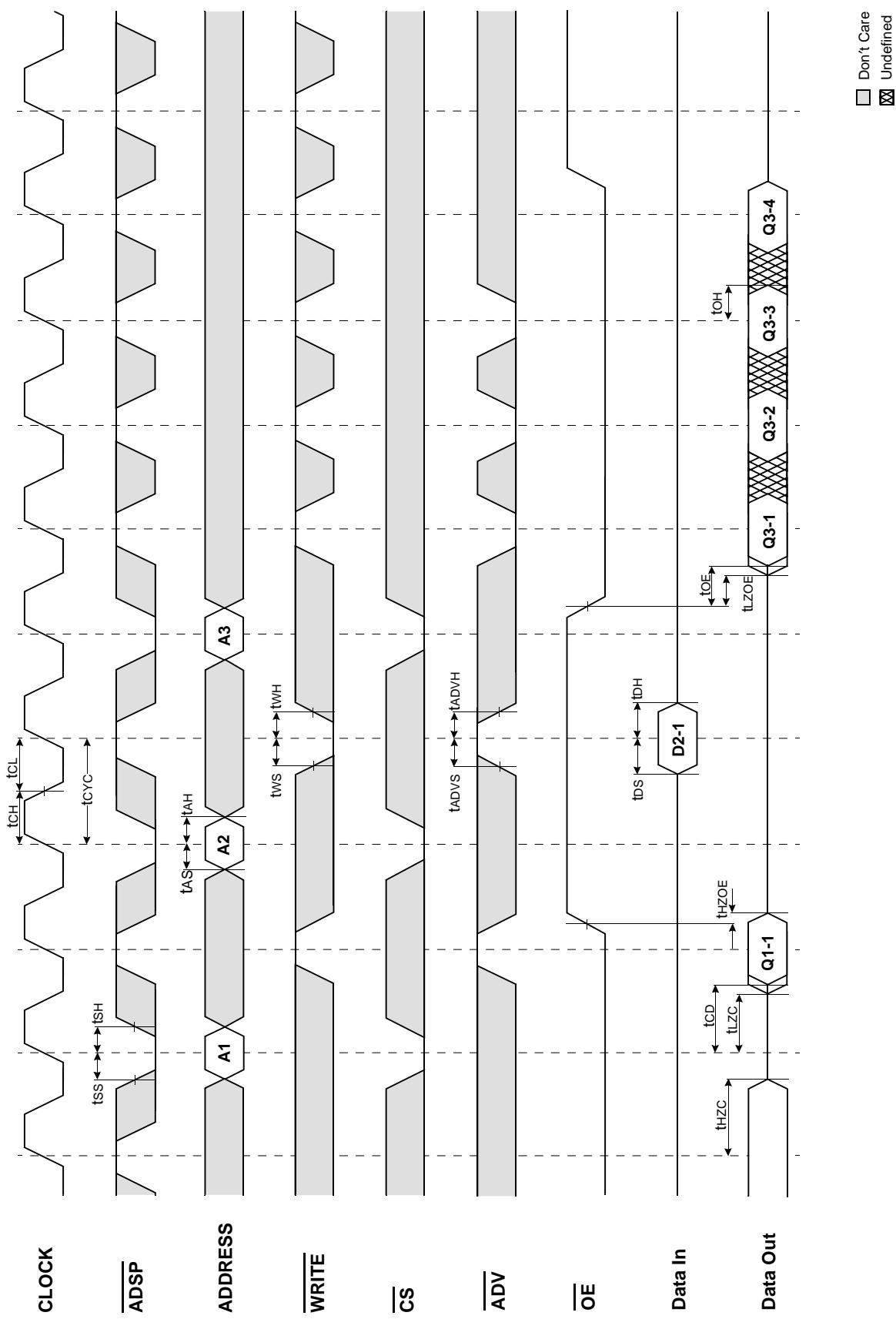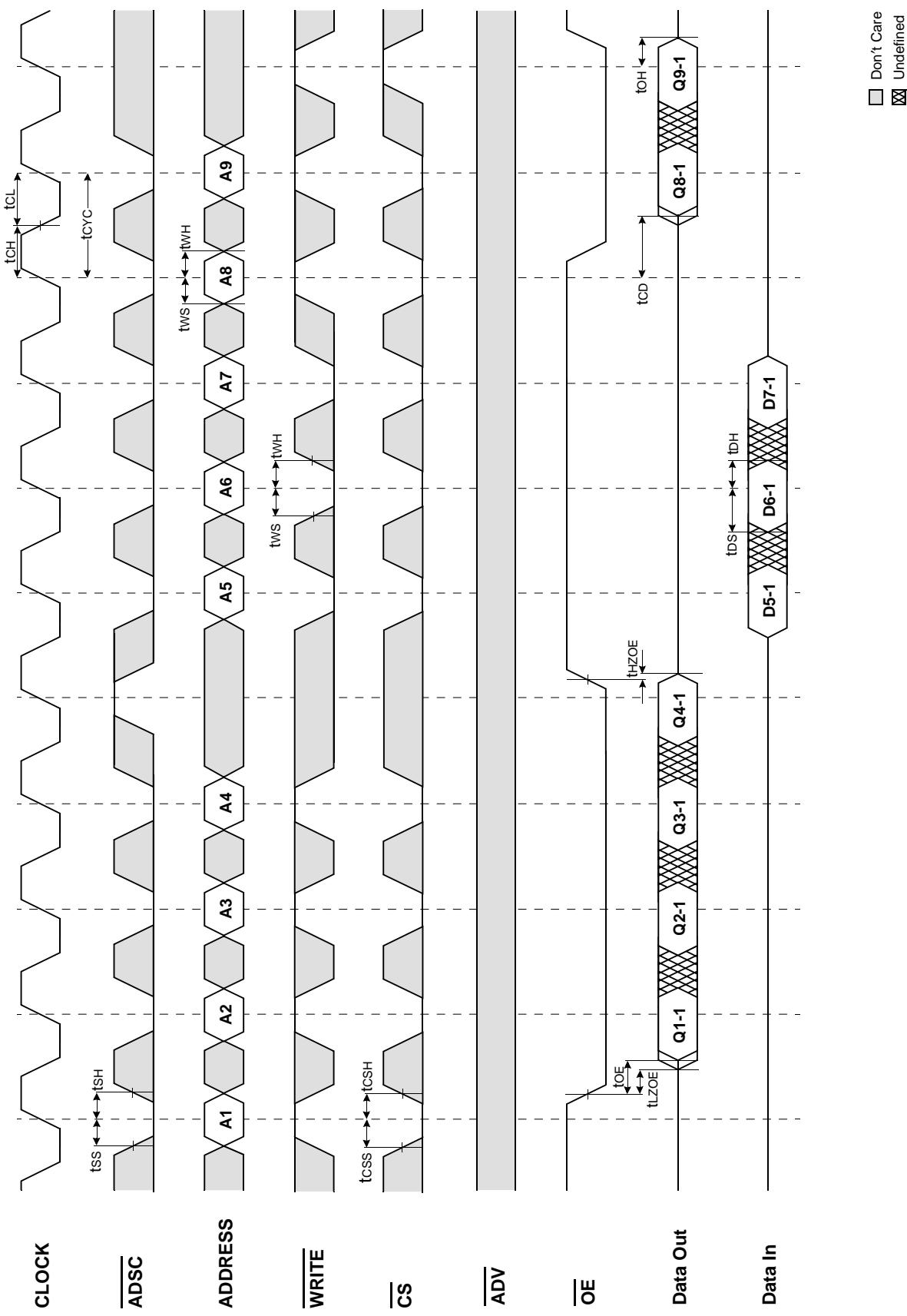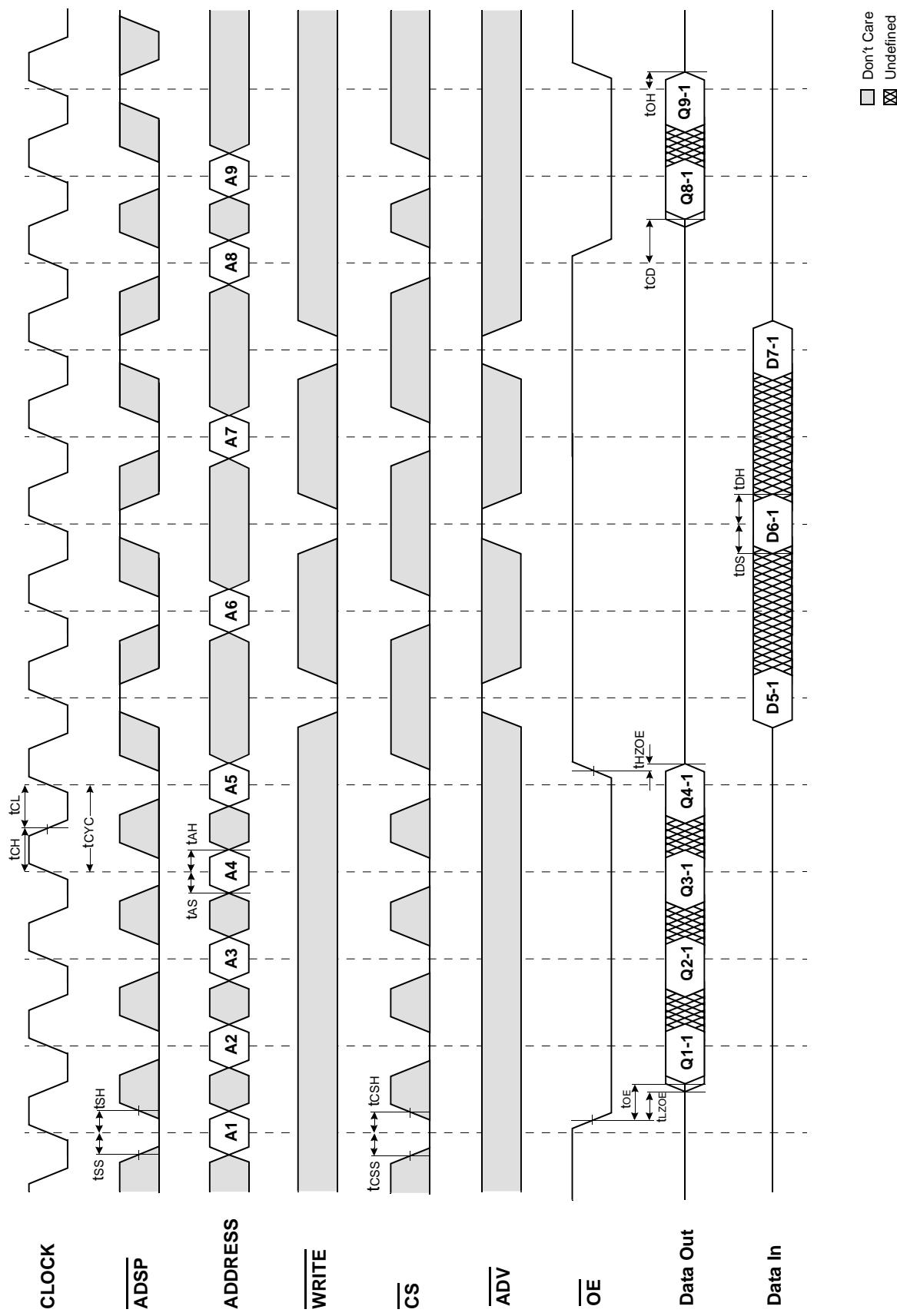
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WEx}$= L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or CS_2 = H, or $\overline{CS_1}$ = L, and CS_2 = L

☐ Don't Care
⊠ Undefined

TIMING WAVEFORM OF WRTE CYCLE

Signals: CLOCK, ADSP, ADSC, ADDRESS, WRITE, CS, ADV, OE, Data In, Data Out

Legend: □ Don't Care   ⊠ Undefined

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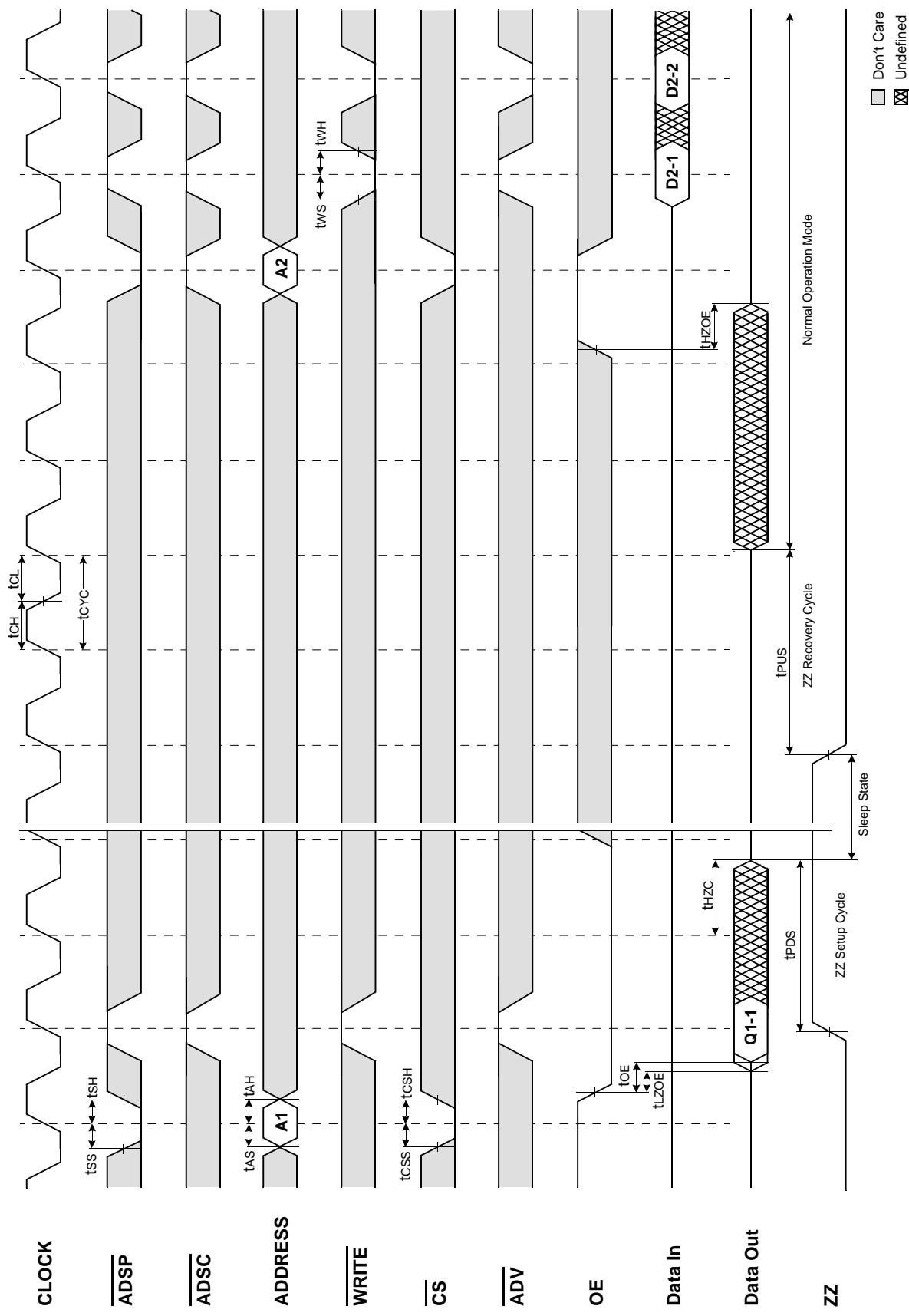
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

Don't Care
Undefined

CLOCK

ADSP

ADDRESS

WRITE

CS

ADV

OE

Data In

Data Out

A1　A2　A3

Q1-1　D2-1　Q3-1　Q3-2　Q3-3　Q3-4

tSS, tSH, tCH, tCL, tCYC, tAS, tAH, tWS, tWH, tADVS, tADVH, tDS, tDH, tHZC, tLZC, tCD, tHZOE, tLZOE, tOE, tOH

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TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

CLOCK

ADSP

ADDRESS   A1 A2 A3 A4 A5 A6 A7 A8 A9

WRITE

CS

ADV

OE

Data Out   Q1-1 Q2-1 Q3-1 Q4-1   Q8-1 Q9-1

Data In   D5-1 D6-1 D7-1

tSS tSH tCH tCL tCYC tAS tAH tCSS tCSH toE tLZOE tHZOE tCD toH tDS tDH

Don't Care   Undefined
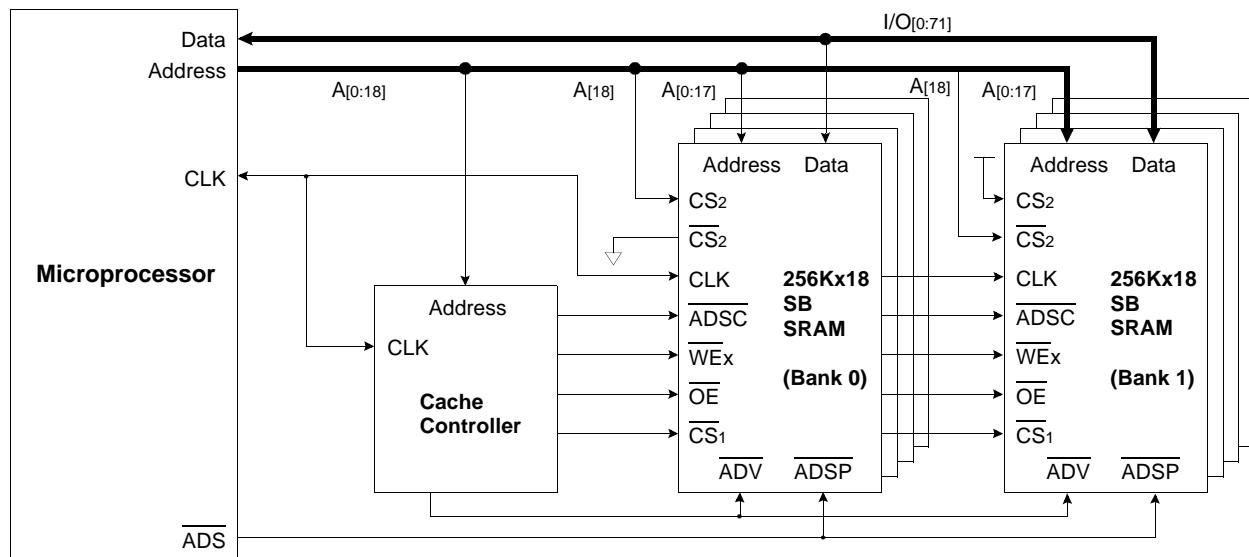
## TIMING WAVEFORM OF POWER DOWN CYCLE

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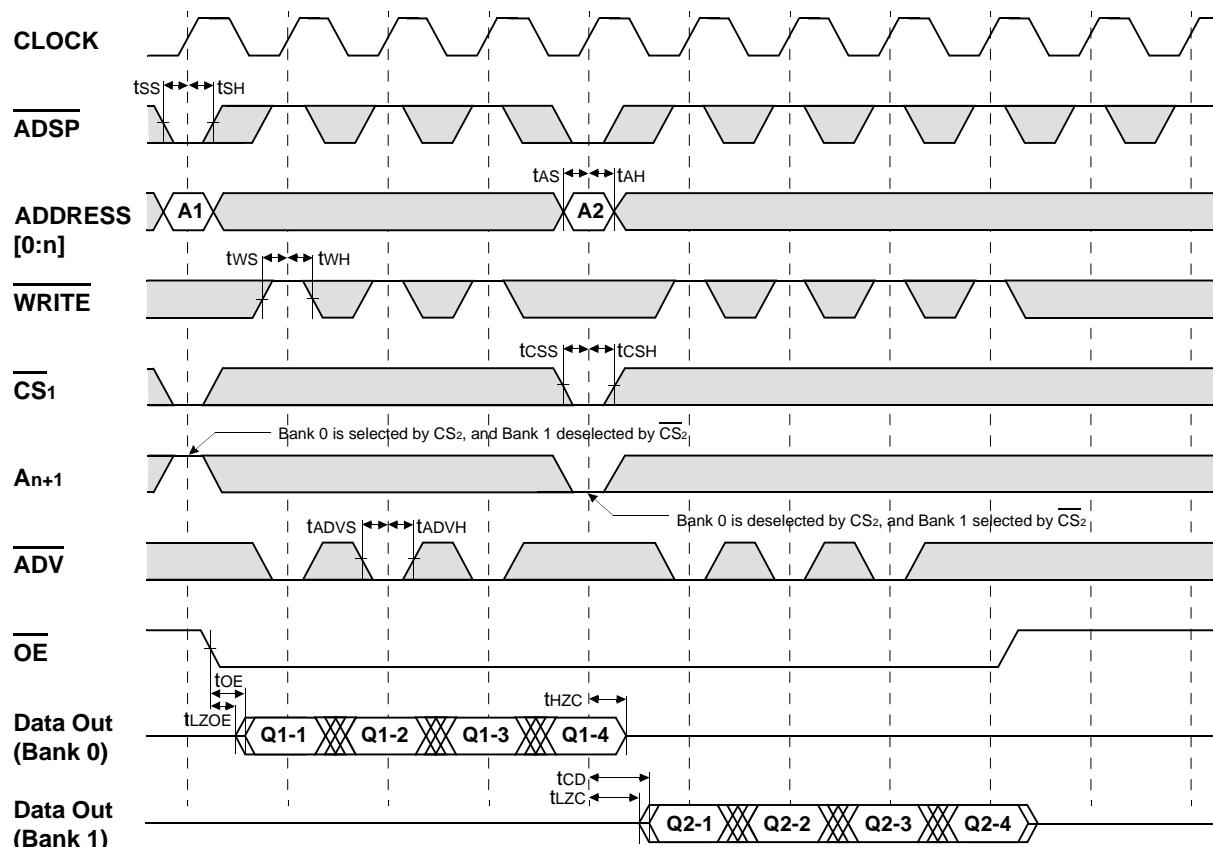
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 256Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{\text{ADSP}}$ CONTROLLED , $\overline{\text{ADSC}}$=HIGH)

*Notes : n = 14   32K depth, 15   64K depth, 16   128K depth, 17   256K depth   □ Don't Care   ▨ Undefined

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PACKAGE DIMENSIONS

100-TQFP-1420A   Units:millimeters/inches

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