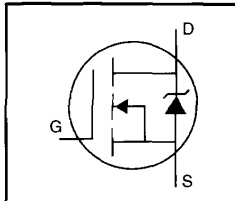


## HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 450V$$

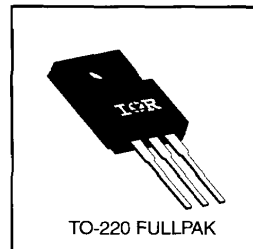
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 3.4A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.




### Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	3.4	A
$I_D @ T_C = 100^\circ C$	2.1	
$I_{DM}$	14	
$P_D @ T_C = 25^\circ C$	35	W
	Linear Derating Factor	0.28
$V_{GS}$	±20	V
$E_{AS}$	100	mJ
$I_{AR}$	3.4	A
$E_{AR}$	3.5	mJ
dv/dt	4.0	V/ns
$T_J$	-55 to +150	°C
$T_{STG}$	Soldering Temperature, for 10 seconds	
	Mounting Torque, 6-32 or M3 screw	
		300 (1.6mm from case)
		10 lbf·in (1.1 N·m)


### Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	3.6	°C/W
$R_{\theta JA}$	—	—	65	

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

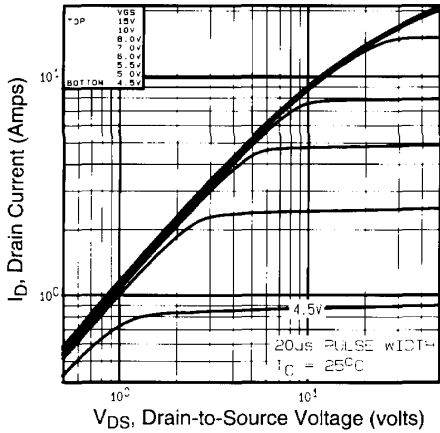
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	450	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =2.0A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	1.5	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =2.0A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =450V, V <sub>GS</sub> =0V
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	45	nC	I <sub>D</sub> =4.9A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	6.6	nC	V <sub>DS</sub> =360V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	24	nC	V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	5.9	—	ns	V <sub>DD</sub> =225V I <sub>D</sub> =4.9A R <sub>G</sub> =12Ω R <sub>D</sub> =45Ω See Figure 10 ④
t <sub>r</sub>	Rise Time	—	22	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	40	—		
t <sub>f</sub>	Fall Time	—	21	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	680	—	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz See Figure 5
C <sub>oss</sub>	Output Capacitance	—	190	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	75	—		
C	Drain to Sink Capacitance	—	12	—		

**Source-Drain Ratings and Characteristics**

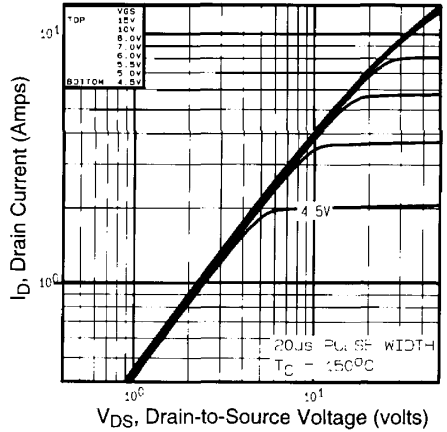
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	3.4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	14		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.0	V	T <sub>J</sub> =25°C, I <sub>S</sub> =4.9A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	460	690	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =4.9A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.8	2.7	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

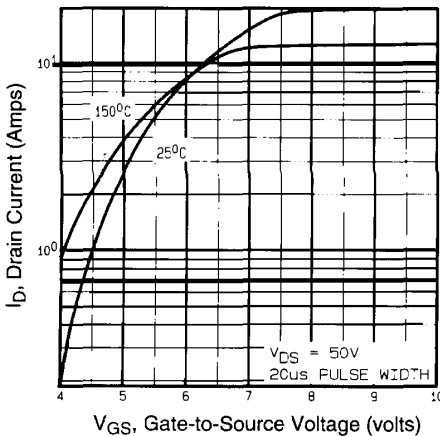
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=15mH R<sub>G</sub>=25Ω, I<sub>AS</sub>=3.4A (See Figure 12)
- ③ I<sub>SD</sub>≤4.9A, di/dt≤80A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.
- ⑤ t=60s, f=60Hz



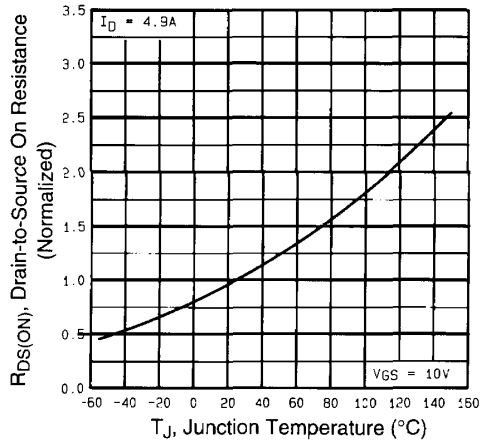
**Fig 1.** Typical Output Characteristics,  $T_C = 25^\circ\text{C}$



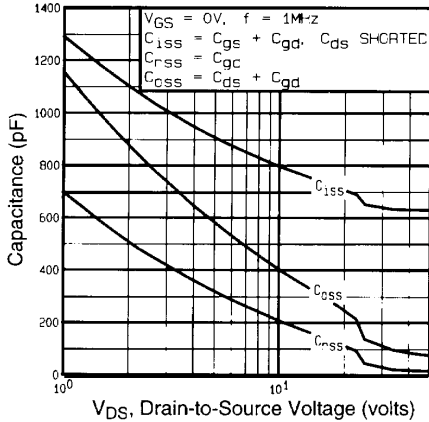
**Fig 2.** Typical Output Characteristics,  $T_C = 150^\circ\text{C}$



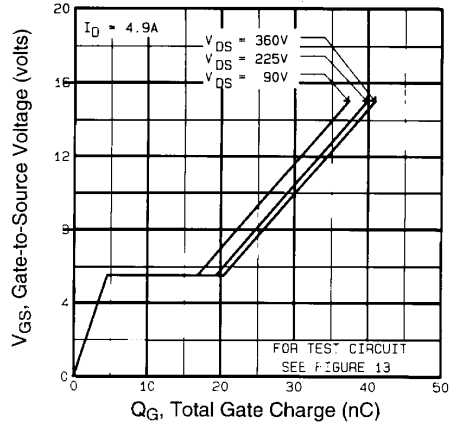
**Fig 3.** Typical Transfer Characteristics



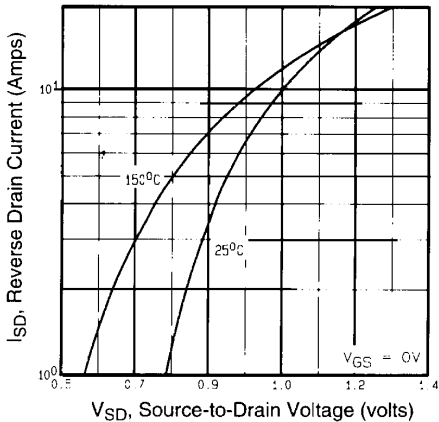
**Fig 4.** Normalized On-Resistance Vs. Temperature



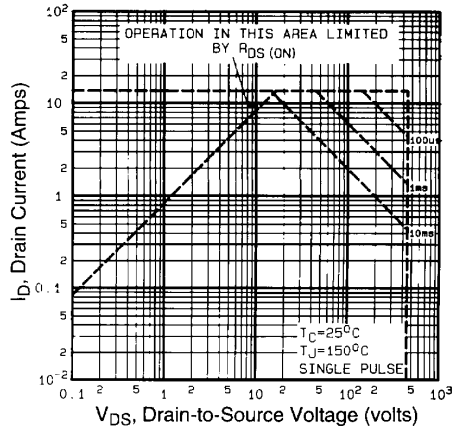
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



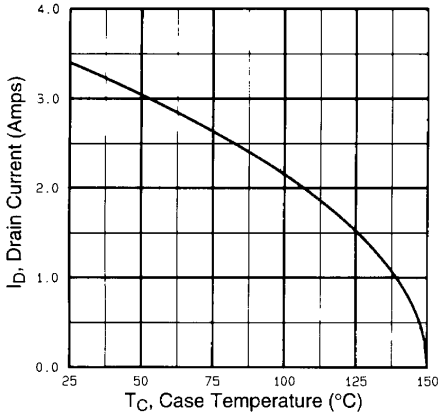
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



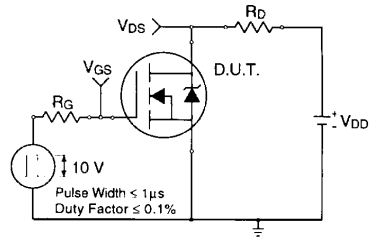
**Fig 7.** Typical Source-Drain Diode Forward Voltage



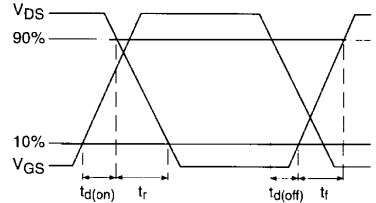
**Fig 8.** Maximum Safe Operating Area



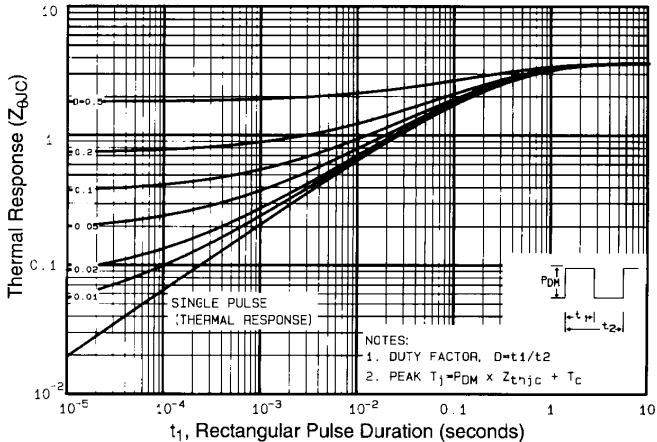
**Fig 9.** Maximum Drain Current Vs. Case Temperature



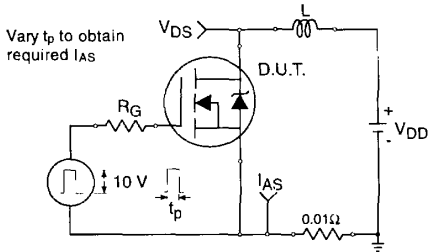
**Fig 10a.** Switching Time Test Circuit



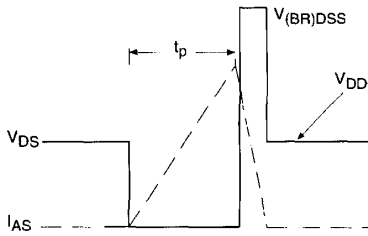
**Fig 10b.** Switching Time Waveforms



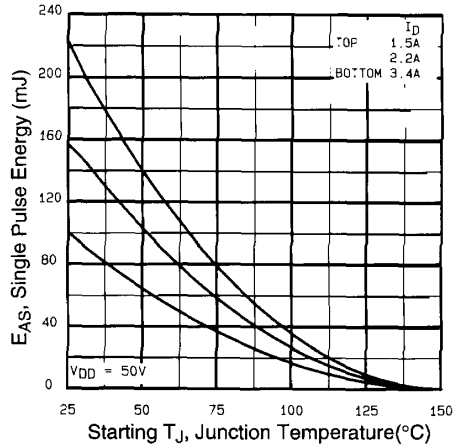
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



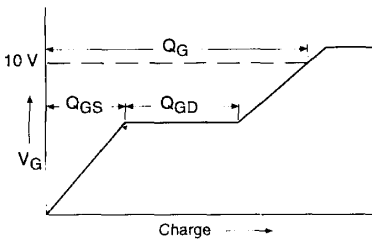
**Fig 12a.** Unclamped Inductive Test Circuit



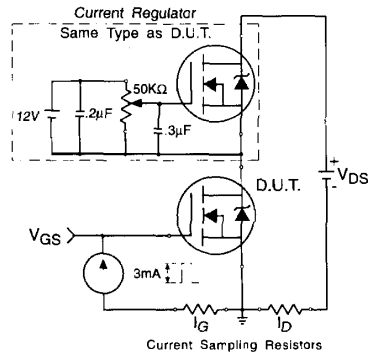
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit

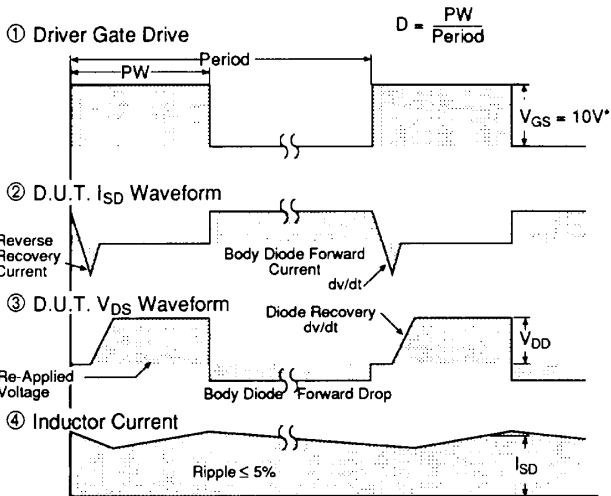
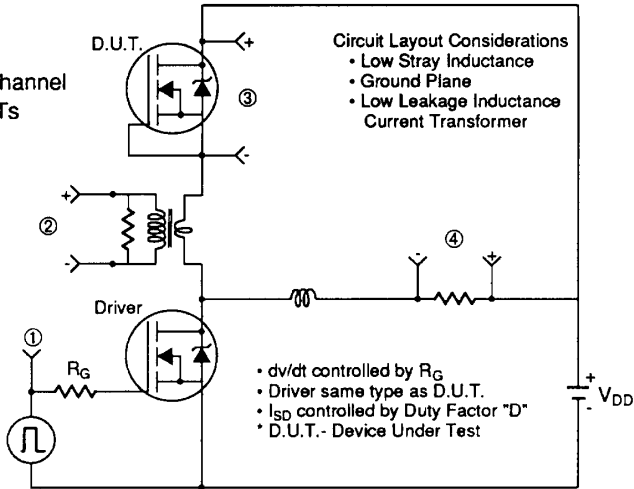
**Appendix B:** Package Outline Mechanical Drawing

**Appendix C:** Part Marking Information

## Appendix A

### Peak Diode Recovery dv/dt Test Circuit

**Fig 14.** For N-Channel HEXFETs

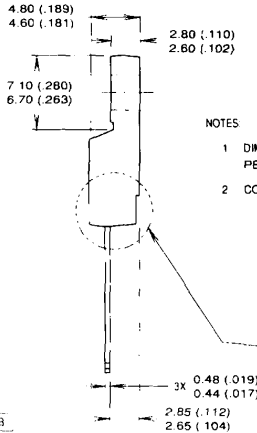
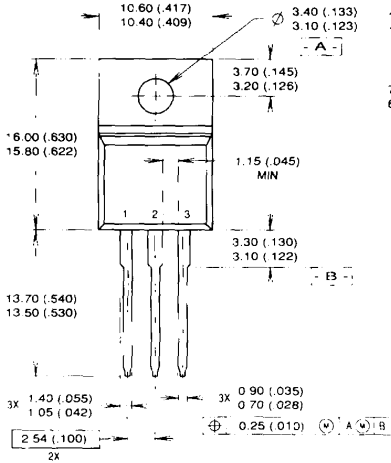


\*  $V_{GS} = 5V$  for Logic Level Devices

## Package Outline

### TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)

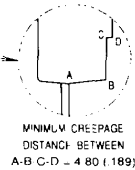


#### LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

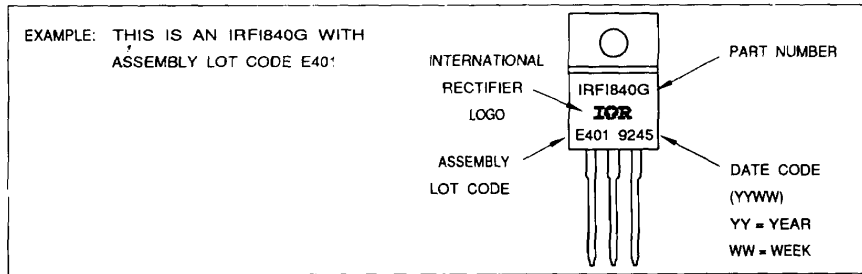
#### NOTES

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.



## Part Marking Information

### TO-220 FULL-PAK



Printed on Signet recycled offset: made from 50% recycled waste paper, including 10% de-inked, post-consumer waste.



# International Rectifier

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