CMOS Image Sensor with Image Signal Processing

HV7131RP

MagnaChip Semiconductor Ltd.

Version 1.5

Revision History

Revision	Script Date	Comments
V1.0	2003/10/15/Wed	- HV7131RP Preliminary is released
V1.1	2004/01/20/Tue	- register information is updated
V1.2	2004/03/22/Mon	- register information is updated
V1.3	2004/08/16/Mon	- register information is updated. (AE Anti-Flicker Step, AE Maximum Limit) - ENB setting is updated.
V1.4	2004/10/04/Mon	- MagnaChip Logo Changed
V1.5	2005/02/04/Fri	- Spectral response is updated. (p.13) - Anti-Banding Configuration is updated.(p.62) - Output Data according to Video Mode is updated.(p. 63) - Electro-Optical Characteristics is updated.(p.75)

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General Description

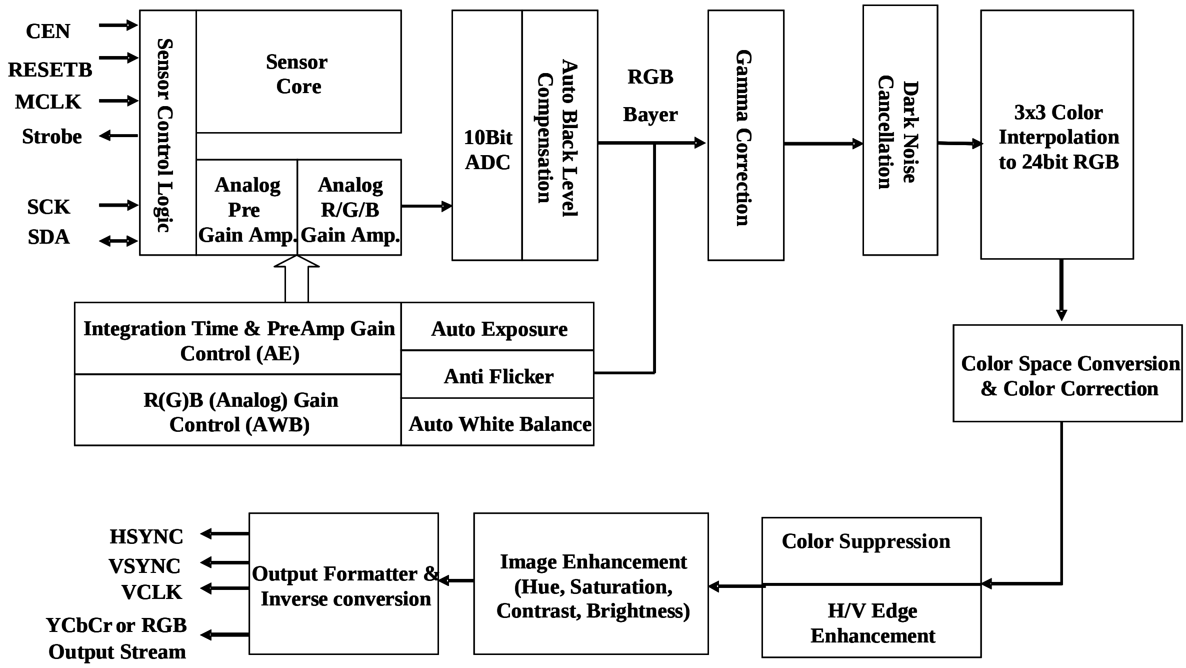
HV7131RP is a highly integrated single chip CMOS color image sensor implemented by proprietary MagnaChip 0.30um CMOS sensor process realizing high sensitivity and wide dynamic range. Total Pixel Array are 660x507 pixels. Each active pixel composed of 4 transistors has a micro-lens to enhance sensitivity, and converts photon energy to analog pixel voltage. On-chip 10bit Analog to Digital Converter (ADC) digitizes analog pixel voltage, and on-chip Correlated Double Sampling (CDS) scheme reduces Fixed Pattern Noise (FPN) dramatically. General image processing functions such as gamma correction, color interpolation, color correction, color space conversion, H/V Edge Enhancement, Image Enhancement, auto exposure, and auto white balance are implemented to diversify its applications, and various output formats are supported for the sensor to easily interface with different video codec chips. The integration of sensor function and image processing functions make HV7131RP especially very suitable for mobile imaging systems such as IMT-2000 phone's video part that requires very low power and system compactness.

Features

- 1/4.5 inch optical format
- Total pixel array : 660x507
- Active pixel array : 640x480
- 5.04um x 5.04um active square pixel
- Micro-lens for high sensitivity
- RGB mosaic color filter array
- On-chip 10 bit ADC
- Correlated double sampling for reduction of Fixed Pattern Noise
- Black Level Compensation
- Gamma correction by programmable piecewise linear approximation
- 3x3 Color interpolation
- Color correction by programmable 3x3 matrix operation
- Image Enhancement : Contrast, Hue, Saturation, Brightness
- Edge Enhancement
- Color space conversion from RGB to YCbCr
- Inverse Color Space conversion YCbCr to RGB
- Sub-sampling Modes : 2x2, 2x6, CIF, QCIF
- Various output formats : YCbCr 4:2:2, RGB 5:6:6, Bayer

- 8bit Data Bus Mode
- Automatic Exposure Control
- Automatic White Balance Control
- Frame Rate : 30 f/s at 25Mhz, HBLANK = 208, VBLANK = 8
- Power Consumption: 86mW @ 30f/s and 2.8V, 68mW @ 15f/s and 2.8V, 336uW @ power down
- Operation Voltage Range : 2.6V ~ 3.0V, Operation Temperature : -10 ~ +50 degrees Celsius
- Package Types : CLCC 40 PIN, COB(Chip-on-Board), COF(Chip-on-Flex)

Block Diagram

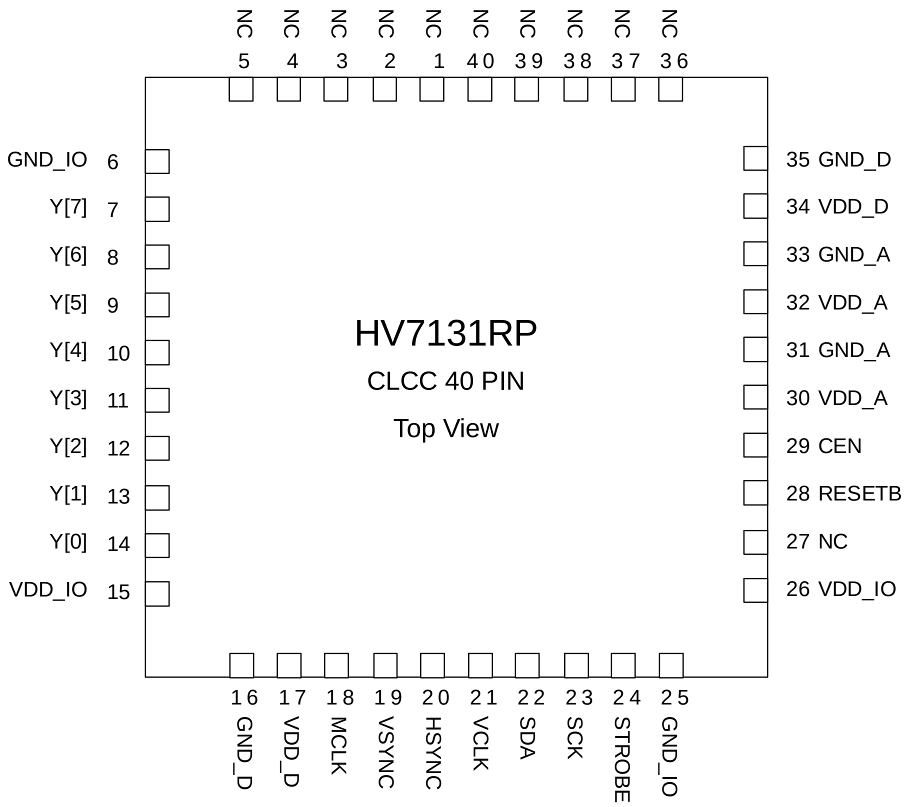


Pixel Array Structure

Metal Shielded Black Level Array [2 line]								
G	R	G	R	….	G	R	G	R
B	G	B	G	….	B	G	B	G
G	R	G	R	….	G	R	G	R
B	G	B	G	….	B	G	B	G
Metal Shielded Black Level Array [2 line]								

Note: If black level data output is enabled& ABLC enabled(SCTRC[1:0] set to 2'b11) with Bayer mode select(SCTRC[7] set to high), data output in the areas of Metal Shielded Black Level Array can be monitored during 4 line period of HSYNC right after VSYNC goes from high state to low state.

40LD Pin Diagram



Pin Description

Pin	Type	Symbol	Description
1-5	N	NC	No Connection
6	G	GND_IO	Ground for I/O Buffer
7~14	O	Y[7:0]	8Bits Video Data output
15	P	VDD_IO	Power for I/O Buffer
16	G	GND_D	Ground for Internal Digital Block
17	P	VDD_D	Power for Internal Digital Block
18	I	MCLK	Master Input Clock
19	O	VSYNC	Video Frame Synchronization signal. VSYNC is active at start of image data frame.
20	O	HSYNC	Video Horizontal Line Synchronization signal. Image data is valid, when HSYNC is high.
21	O	VCLK	Video Output Clock
22	B	SDA	I2C Standard data I/O port
23	I	SCK	I2C Clock Input
24	O	STROBE	Strobe Signal Output
25	G	GND_IO	Ground for I/O Buffer
26	P	VDD_IO	Power for I/O Bufrfer
27	N	NC	No Connection
28	I	RESETB	Sensor Reset, Low Active
29	I	CEN	Chip Enable, High Active CEN low : sleep mode, CEN high : normal operation mode
30	P	VDD_A	Power for Internal Analog Block
31	G	GND_A	Ground for Internal Analog Block
32	P	VDD_A	Power for Internal Analog Block
33	G	GND_A	Ground for Internal Analog Block
34	P	VDD_D	Power for Internal Digital Block
35	G	GND_D	Ground for Internal Digital Block
36-40	N	NC	No Connection

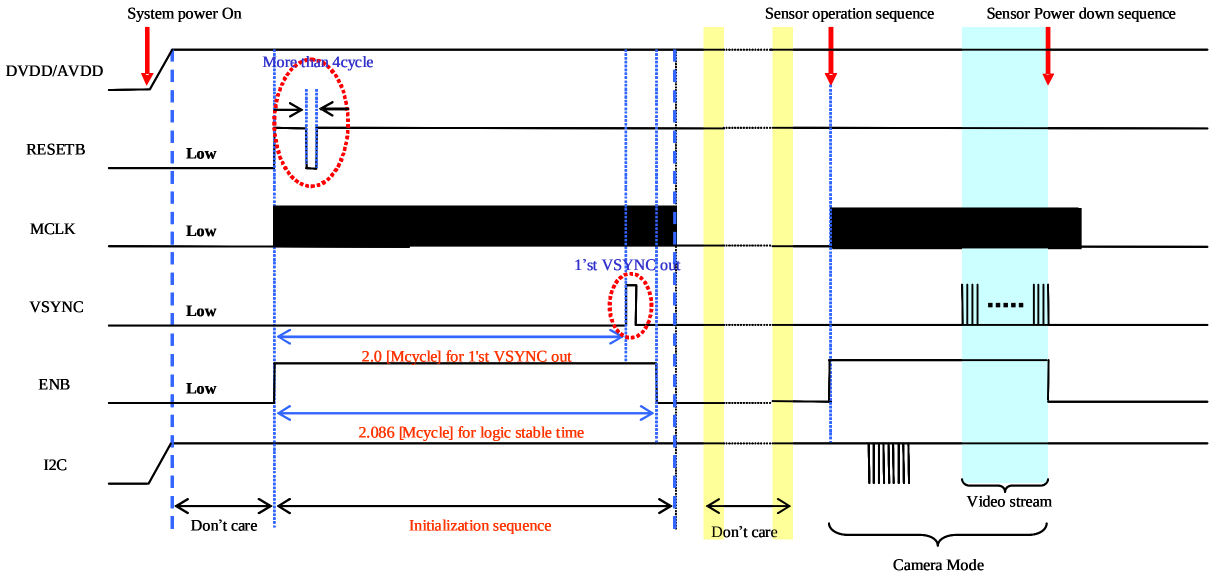
Functional Description

Pixel Architecture

Pixel architecture is a 4 transistor NMOS pixel design. The additional use of a dedicated transfer transistor in the architecture reduces most of reset level noise so that fixed pattern noise is not visible. Furthermore, micro-lens is placed upon each pixel in order to increase fill factor so that high pixel sensitivity is achieved.

ENB Setting guide information for normal stand-by mode

It is necessary that this kind of initialization sequence for the normal stand-by mode of HV7131RP after system power on



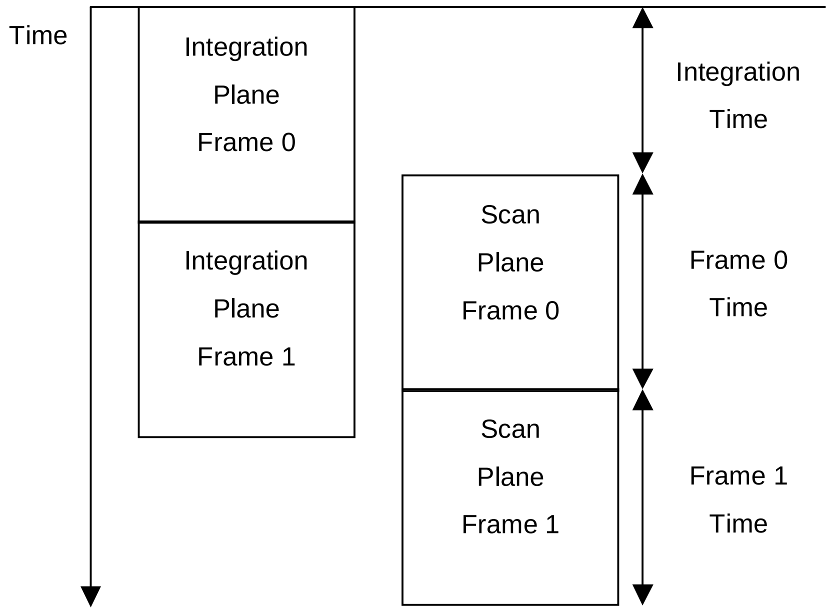
ex) If MCLK = 25[Mhz]

=> 2.086[Mcycle] / 25[MHz] = 83.44 ms

The time period of ENB high value have to keep for 83.44[ms] or more

Sensor Imaging Operation

Imaging operation is implemented by the offset mechanism of integration domain and scan domain (rolling shutter scheme). First integration plane is initiated, and after the programmed integration time is elapsed, scan plane is initiated, then image data start being produced.



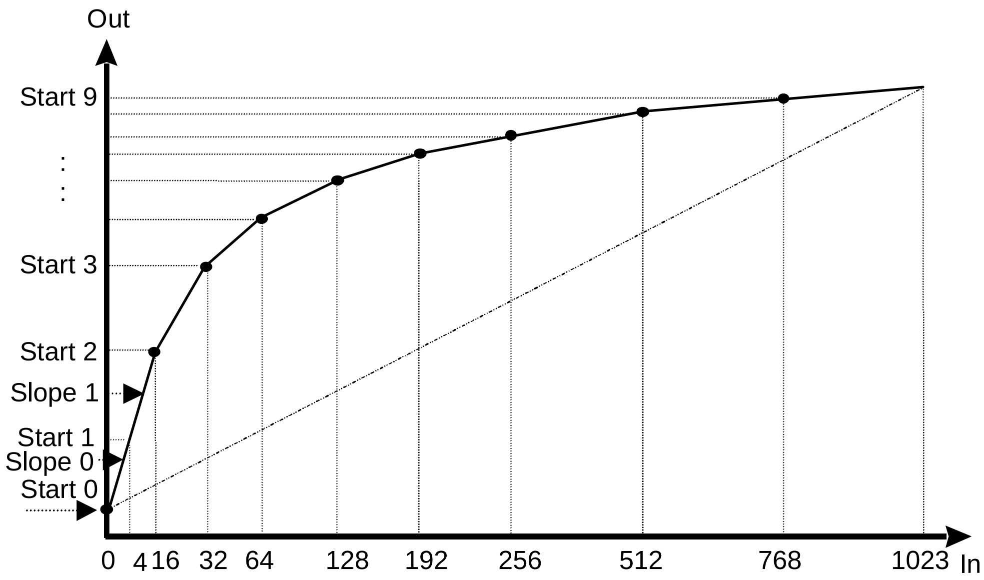
10bit on-chip ADC

On-chip ADC converts analog pixel voltage to 10bit digital data.

Gamma Correction

Piecewise linear gamma approximation method is implemented. Ten piece linear segments are supported and user-programmable.

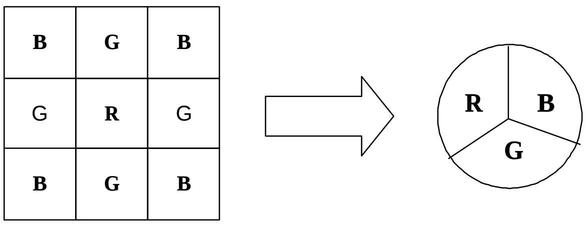
Gamma Slope Registers are programmed as the integer value of real slope value that is multiplied by 64.



Gamma Transfer Function

Color Interpolation

3x3 linear color interpolation is done by moving 3x3 interpolation window by one pixel horizontally and vertically



Color Correction & Color Space Conversion

Both of Color Correction and Color Space conversion are implemented by 3x3 matrix operation, so that two stages may be merged into one matrix stage.

Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. For color space conversion matrix, the equation from CCIR-601 standard is normally used. Therefore, the intended single matrix for color correction and color space conversion may be resolved as below.

*Intended single matrix = Color Space Conversion Matrix * Color Correction Matrix*

Intended single matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended single matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer (Real Coefficient Value x 64);

For negative values, CMAxx = Two Complement(Integer (Real Coefficient Value x 64));

Real Coefficient Value values from –127/64 to 127/64 can be programmed.

CCIR-601 YCbCr color space conversion equation

< Conversion Equation >
Y = (77R + 150G + 29B)/256 Range: 16 ~ 235
Cb = (-44R –87G + 131B)/256 + 128 Range: 16 ~ 240
Cr = (131R – 110G – 21B)/256 + 128 Range: 16 ~ 240

< Reverse Conversion >
R = Y + 1.371(Cr – 128)
G = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B = Y + 1.732(Cb – 128)

In the above equations, R, G, and B are gamma-corrected values.

Image Enhancement

Contrast, brightness, hue and saturation are programmable. Contrast and saturation factor range is 0.0 ~ 1.99. Brightness factor range is -127 ~ + 128. Hue factor range is -30° ~ + 30° .

Edge Enhancement

Edge enhancement is performed for increasing sharpness of image. Edge weight range is 0.5 ~ 8.0.

Output Formatting

The output formats such as Bayer Raw Data, RGB 5:6:5, and YCbCr 4:2:2 are supported and the sequence of Cb and Cr are programmable.

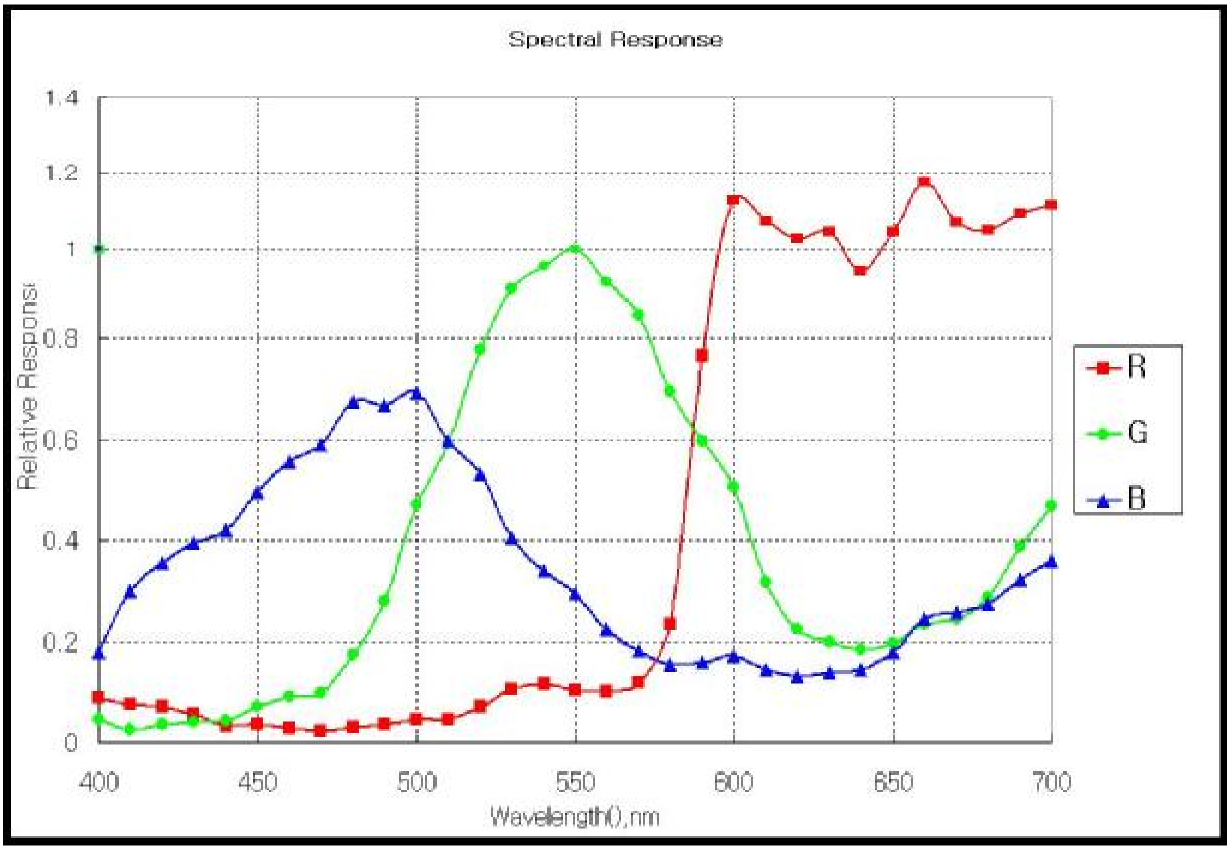
Auto Exposure Control

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to difference between target Y mean value and current frame Y mean value.

Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point.

Spectral Characteristics



Register Description

Register	Symbol	Add. (Hex)	Default (Hex)	Description
Device ID	DEVID	00	42	Product ID, Revision No.
Sensor Control A	SCTRA	01	23	Xflip, Yflip, CIF mode, SSSel, Vmode[1:0]
Sensor Control B	SCTRB	02	00	Power down, Clock division
Sensor Control C	SCTRC	03	01	Sensor Internal control Register
Row Start Address High	RSAU	08	00	Row Start Address Upper Byte
Row Start Address Low	RSAL	09	02	Row Start Address Lower Byte
Column Start Address High	CSAU	0a	00	Column Start Address Upper Byte
Column Start Address Low	CSAL	0b	02	Column Start Address Lower Byte
Window Height High	WIHU	0c	01	Window Height Address Upper Byte
Window Height Low	WIHL	0d	e0	Window Height Address Lower Byte
Window Width High	WIWU	0e	02	Window Width Address Upper Byte
Window Width Low	WIWL	0f	80	Window Width Address Lower Byte
HBLANK Time High	HBLU	10	00	HBLANK Time
HBLANK Time Low	HBLL	11	d0	208 clocks
VBLANK Time High	VBLU	12	00	VBLANK Time
VBLANK Time Low	VBLL	13	08	5 Lines
Red Color Gain	RCG	14	18	0.5 to 2 64 step 6bit resolution
Green Color Gain	GCG	15	18	0.5 to 2 64 step 6bit resolution
Blue Color Gain	BCG	16	18	0.5 to 2 64 step 6bit resolution
Preamp Gain	PgaVal	17	20	0.5 to 16.5 256 step 8bit resolution
Preamp Gain Min	PgaMIN	18	14	0.5 to 16.5 256 step 8bit resolution
Preamp Gain Max	PgaMAX	19	ff	0.5 to 16.5 256 step 8bit resolution
Preamp Gain Nominal	PgaNOM	1a	20	0.5 to 16.5 256 step 8bit resolution
Analog control A	ACTRA	1b	37	Amp Bias[3:0], CDS bias[6:4]
Reset Clamp	ACTRB	1c	7f	Reset Clamping[7:4], ADC bias[3:0]
Red Pixel Black Offset	ORedl	21	3f	-127 to +127 256 step
Green Pixel Black Offset	OGrnl	22	3f	MSB = '0' mean "-" {1'b0, [4:0]}
Blue Pixel Black Offset	OBlul	23	3f	LSB = '1' mean "+" {1'b0, [4:0]}
Red Pixel Active Offset	ORedU	24	RO	ADC Offset Value for Active Red Pixel
Green Pixel Active Offset	OGrnU	25	RO	ADC Offset Value for Active Green Pixel

Blue Pixel Active Offset	OBluU	26	RO	ADC Offset Value for Active Blue Pixel
Black Level Threshold	BLCTH	27	3f	Black Level Threshold Value(256)
ISP Function Enable	IspFen	30	02	Functions Enable & Edge Eh
ISP Output Format	OutFmT	31	60	Image data output formatting & Inversion
Dark Noise Cancellation	DncMode	33	41	Dnc Blocking[7:4], Dnc Th[3:2], Dnc Mode[1:0]
Dnc Enable Gain	DncGain	34	3e	Dnc enable at Pgain 4.3x
Dnc Enable Int. Time	DncIntH	35	13	Dnc enable at
	DncIntM	36	12	Int time > {DncIntH, DncIntM, 8'h00}
Color Matrix Coefficient 11	CMA11	37	2f	Color matrix coefficient 11
Color Matrix Coefficient 12	CMA12	38	db	Color matrix coefficient 12
Color Matrix Coefficient 13	CMA13	39	F6	Color matrix coefficient 13
Color Matrix Coefficient 21	CMA21	3a	0f	Color matrix coefficient 21
Color Matrix Coefficient 22	CMA22	3b	28	Color matrix coefficient 22
Color Matrix Coefficient 23	CMA23	3c	08	Color matrix coefficient 23
Color Matrix Coefficient 31	CMA31	3d	f5	Color matrix coefficient 31
Color Matrix Coefficient 32	CMA32	3e	ce	Color matrix coefficient 32
Color Matrix Coefficient 33	CMA33	3f	3d	Color matrix coefficient 33
Gamma Segment Point 0	GmaP0	40	00	Start point for gamma line segment 0
Gamma Segment Point 1	GmaP1	41	04	Start point for gamma line segment 1
Gamma Segment Point 2	GmaP2	42	12	Start point for gamma line segment 2
Gamma Segment Point 3	GmaP3	43	21	Start point for gamma line segment 3
Gamma Segment Point 4	GmaP4	44	37	Start point for gamma line segment 4
Gamma Segment Point 5	GmaP5	45	55	Start point for gamma line segment 5
Gamma Segment Point 6	GmaP6	46	6b	Start point for gamma line segment 6
Gamma Segment Point 7	GmaP7	47	7d	Start point for gamma line segment 7
Gamma Segment Point 8	GmaP8	48	B4	Start point for gamma line segment 8
Gamma Segment Point 9	GmaP9	49	dd	Start point for gamma line segment 9
Gamma Segment Slope 0	GmaS0	4a	40	Slope value for gamma line segment 0
Gamma Segment Slope 1	GmaS1	4b	4b	Slope value for gamma line segment 1
Gamma Segment Slope 2	GmaS2	4c	3c	Slope value for gamma line segment 2
Gamma Segment Slope 3	GmaS3	4d	2c	Slope value for gamma line segment 3
Gamma Segment Slope 4	GmaS4	4e	1e	Slope value for gamma line segment 4
Gamma Segment Slope 5	GmaS5	4f	16	Slope value for gamma line segment 5

Gamma Segment Slope 6	GmaS6	50	12	Slope value for gamma line segment 6
Gamma Segment Slope 7	GmaS7	51	0e	Slope value for gamma line segment 7
Gamma Segment Slope 8	GmaS8	52	0a	Slope value for gamma line segment 8
Gamma Segment Slope 9	GmaS9	53	09	Slope value for gamma line segment 9
Invers Color constant for R	RCrconst	54	57	Invers Color Constant for R
Invers Color constant for G	GCrconst	55	d4	Invers Color Constant for G
Invers Color constant for G	GCbconst	56	eb	Invers Color Constant for G
Invers Color constant for B	BCbconst	57	6e	Invers Color Constant for B
Hue Value 1	HUE1	58	00	Hue value 1
Hue Value 2	HUE2	59	80	Hue value 2
Contrast Value	Contrast	5a	80	Contrast Value
Brightness Value	Brightness	5b	00	Brightness Value
Saturation Value	Saturation	5c	80	Saturation Value
Edge Weight Control Value	EgWtCon	5d	00	Edge Weight Control Value
Edge Enhancement Vth Low	EdThLo	5e	10	Edge Enhancement Vth Low
Suppression Pre Amp Gain Min	SupGMin	60	24	Suppression Pre Amp Gain Min
Saturation Pre Amp Gain Min	SatGMin	61	24	Saturation Pre Amp Gain Min
Edge Pre Amp Gain Min	EdgGMin	62	24	Edge Gain Min
AE Mode 1	AeMode1	70	29	Auto exposure mode selection 1
AE Mode 2	AeMode2	71	ed	Auto exposure mode selection 2
AE Windows weight	AeWinWgt	72	cd	AE Windows weigth
Integration Time High	INTH	73	02	Integration Time High
Integration Time Middle	INTM	74	71	Integration Time Middle
Integration Time Low	INTL	75	00	Integration Time Low
AE Target OutDoor	LuTarget1	76	5a	AE Target OutDoor
AE Target InDoor	LuTarget2	77	5a	AE Target InDoor
AE Lock Boundary	AeLockFineBnd	78	f6	AE Lock Boundary
AE Unlock Boundary	AeUnlockBnd	79	2a	AE Unlock Boundary
AE Anti-Flicker Step High	AeintStepH	7a	01	AE Anti-Flicker Step High
AE Anti-Flicker Step Middle	AeintStepM	7b	38	AE Anti-Flicker Step Middle

AE Anti-Flicker Step Low	AeintStepL	7c	80	AE Anti-Flicker Step Low
AE Maximum Limit High	AeIntLimitH	7d	09	AE Maximum Limit High
AE Maximum Limit Middle	AeIntLimitM	7e	c4	AE Maximum Limit Middle
AE Maximum Limit Low	AeIntLimitL	7f	00	AE Maximum Limit Low
AWB Mode	AWBMode	80	18	AWB mode
AWB Windows Weight	AwbWinWgt	82	00	AWB Windows Weight
AWB Cb Target Position	CbTarget	83	80	AWB Cb Target Position
AWB Cr Target Position	CrTarget	84	80	AWB Cr Target Position
AWB Lock Boundary	AwbLockBnd	85	02	AWB Lock Boundary
AWB Unlock Boundary	AwbUnlockBnd	86	20	AWB Unlock Boundary
AWB Cb White Pixel Boundary	CbWhiteBnd	87	30	AWB White Pixel Boundary
AWB Cr White Pixel Boundary	CrWhiteBnd	88	30	AWB White Pixel Boundary
AWB C Boundary	AwbCBnd	89	30	AWB Cb+Cr Boundary
R/B Gain Max	AwbGainMax	8a	3f	R/B Gain Max
R/B Gain Min	AwbGainMin	8b	00	R/B Gain Min
AE State Machine	AeFSM	8c	RO	AE State Machine
AWB State Machine	AwbFSM	8d	RO	AWB State Machine
Lu Frame Mean	LuFMean	8e	RO	Lu Frame Mean Value
Cb Frame Mean	CbFMean	8f	RO	Cb Frame Mean Value
Cr Frame Mean	CrFMean	90	RO	Cr Frame Mean Value
Anti Banding Gain Min	KIBndMin	91	14	Anti Banding Pre Amp Gain Min
Anti Banding Gain Max	KIBndMax	92	3d	Anti Banding Pre Amp Gain Max
Awb White Pixel Boundary	AwbWhite	93	ff	Awb White Pixel Boundary
Awb Black Pixel Boundary	AwbBlack	94	00	Awb Black Pixel Boundary
Awb Valid Number	AwbNumber	95	02	Awb Valid Number
Integreation-Scan Plane Offset High	IntScnOfsH	96	R0	Integration-Scan Plane Offset High
Integreation-Scan Plane Offset Middle	IntScnOfsM	97	R0	Integration-Scan Plane Offset Middle
Integreation-Scan Plane Offset Low	IntScnOfsL	98	R0	Integration-Scan Plane Offset Low

Device ID [DEVID : 00h : 42h]

7	6	5	4	3	2	1	0
Product ID				Revision Number			
0	1	0	0	0	0	1	0

High nibble represents Sensor Array Resolution, Low Nibble represents Revision Number.

Sensor Control A [SCTRA : 01h : 23h]

7	6	5	4	3	2	1	0
Reserved		X-Flip	Y-Flip	CifMode	SSSel	Video Mode	
0	0	1	0	0	0	1	1

X-Flip	Image is horizontally flipped
Y-Flip	Image is vertically flipped
CifMode	When this register set to high and video mode(SCTRA[1:0]) set to "11" or "00", output data is CIF format. And if this register set to high and video mode(SCTRA[1:0]) set to "10", output data is QCIF format.
SSSel	0 ISP Sub-Sampling(High Image Quality, 1x Core Frame Rate) 1 Bayer Sub Sampling(Low Image Quality, 2x Core Frame Rate) * only applicable Row, Column is always ISP
Video Mode	11 No Scaling mode 10 2x2 subsampling mode (1/4 subsampling) 01 2x6 subsampling mode (1/16 subsampling) 00 No Scaling mode

* More detailed information is available on page 63

Sensor Control B [SCTRB : 02h : 00h]

7	6	5	4	3	2	1	0
AE/AWB Block Sleep	Data path Block Sleep	Analog Block Sleep	All Internal Block Sleep	Strobe Signal Enable	Clock Division		
0	0	0	0	0	0	0	0

< Clock Acronym Definition >

MCF : Master Clock Frequency	DCF : Divided Clock Frequency
SCF : Sensor Clock Frequency	ICF : Image Processing Clock Frequency
VCF : Video Clock Frequency	LCF : Line Clock Frequency

< Clock Frequency Relation >

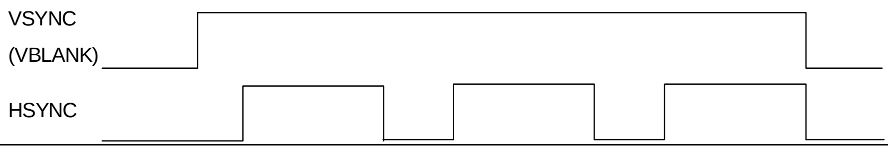
MCF : MCF	DCF : MCF/Clock Division	
SCF : DCF/2	ICF	SCF for 3x3 interpolation, SCF/2 for 1/4 subsampling mode SCF/4 for 1/16 subsampling mode
VCF : ICF*2 for 8bit output	LCF : 1/(HBLANK Period + HSYNC Period)	

AE/AWB Block Sleep	AE/AWB block goes into sleep mode with this bit set to high.
Data path Block Sleep	Image processing data path block goes into sleep mode with this bit set to high.
Analog Block Sleep	all internal analog block goes into sleep mode with this bit set to high. With All Digital Block Sleep active, sensor goes into power down mode.
All Internal Block Sleep	all internal digital and analog block goes into sleep with this bit set to high.
Strobe Signal Enable	When strobe signal is enabled by this bit, STROBE pin will indicates when strobe light should be splashed in the dark environment to get adequate lighted image.
Clock Division	divides input master clock(IMC) for internal use. Internal divided clock frequency (DCF) is defined as master clock frequency (MCF) divided by specified clock divisor. Internal divided clock frequency (DCF) is as follows. 000 : MCF, 001 : MCF/2, 010 : MCF/4, 011 : MCF/8

	100 : MCF/16, 101 : MCF/32, 110 : MCF/64, 111 : MCF/128

Sensor Control C [SCTRC : 03h : 01h]

7	6	5	4	3	2	1	0
Bayer Output Enable	Single Shot Mode	Black level average output	HSYNC in VBLANK	reserved	Unit Gain Mode	Black Level Data Enable	ABLC enable
0	0	0	0	0	0	0	1

Bayer Output Enable	0	Output format is set to RGB565 or YCbCr 4:2:2 by ISP Output Format [31h] value.
	1	Bayer Raw data which does not pass ISP function is printed out.
Single Shot Mode		With this register set to high, single video image is streamed out
Black Level Average Output	0	This bit enable R/G/B Active Offset registers[24h-26h] to represent updated active offset values
	1	This bit enable R/G/B Active Offset registers[24h-26h] to represent black level average value
HSYNC in VBLANK		VBLANK is equivalent to VSYNC, and HSYNC is the inversion of HBLANK, and this bit control whether HSYNC is active or not when VBLANK unit is LCF. 
Unit Gain Mode		If set to HIGH, the value of R Gain and B Gain will become equal to G Gain.
Black Level Data Enable		HSYNC is generated for light-shielded pixels in 4 lines.
Auto Black Level Compensation		Black level average values of light-shielded pixels are compensated when active image data is produced.

Row Start Address High [RSAU : 08h : 00h]

7	6	5	4	3	2	1	0
reserved							Row Start Address High
0	0	0	0	0	0	0	0

Row Start Address Low [RSAL : 09h : 02h]

7	6	5	4	3	2	1	0
Row Start Address Low							
0	0	0	0	0	0	1	0

Row Start Address register defines the row start address of image read out operation.

Column Start Address High [CSAU : 0ah : 00h]

7	6	5	4	3	2	1	0
reserved						Column Start Address High	
0	0	0	0	0	0	0	0

Column Start Address Low [CSAL : 0bh : 02h]

7	6	5	4	3	2	1	0
Column Start Address Low							
0	0	0	0	0	0	1	0

Column Start Address register defines the column start address of image read out operation.

Window Height High [WIHU : 0ch : 01h]

7	6	5	4	3	2	1	0
reserved							Window Height High
0	0	0	0	0	0	0	1

Window Height Low [WIHL : 0dh : e0h]

7	6	5	4	3	2	1	0
Window Height Low							
1	1	1	0	0	0	0	0

Window Height register defines the height of image to be read out.

Window Width High [WIWU : 0eh : 02h]

7	6	5	4	3	2	1	0
reserved						Window Width High	
0	0	0	0	0	0	1	0

Window Width Low [WIWL : 0fh : 80h]

7	6	5	4	3	2	1	0
Window Width Low							
1	0	0	0	0	0	0	0

Window Width Address register defines the width of image to be read out.

HBLANK Time High [HBLU : 10h : 00h]

7	6	5	4	3	2	1	0
HBLANK Time High							
0	0	0	0	0	0	0	0

HBLANK Time Low [HBLL : 11h : d0h]

7	6	5	4	3	2	1	0
HBLANK Time Low							
1	1	0	1	0	0	0	0

HBLANK Time register defines data blank time between current line and next line by using Sensor Clock Period unit (1/SCF), and should be larger than 208(d0h).

VBLANK Time High[VBLU : 12h : 00h]

7	6	5	4	3	2	1	0
VBLANK Time High							
0	0	0	0	0	0	0	0

VBLANK Time Low[VBLL : 13h : 08h]

7	6	5	4	3	2	1	0
VBLANK Time Low							
0	0	0	0	1	0	0	0

VBLANK Time register defines active high duration of VSYNC output. Active high VSYNC indicates frame boundary between continuous frames. For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing section.

Each sensor has a little different photo-diode characteristics so that the sensor provides internal adjustment registers that calibrate internal sensing circuit in order to get optimal performance. Sensor characteristics adjustment registers are as below.

Red Color Gain [RCG : 14h : 18h]

7	6	5	4	3	2	1	0
reserved		R Color Gain					
0	0	0	1	1	0	0	0

Green Color Gain [RCG : 15h : 18h]

7	6	5	4	3	2	1	0
reserved		G Color Gain					
0	0	0	1	1	0	0	0

Blue Color Gain [RCG : 16h : 18h]

7	6	5	4	3	2	1	0
reserved		B Color Gain					
0	0	0	1	1	0	0	0

There are three color gain registers for R, G, B pixels, respectively. Programmable range is from 0.5X ~ 2.5X. Effective Gain = 0.5 + B<5:0>/32. These registers may be used for white balance and color effect with independent R,G,B color control. Default gain is 1.25X.

Preamp Gain [PgaVal : 17h : 20h]

7	6	5	4	3	2	1	0
Preamp Gain							
0	0	1	0	0	0	0	0

Preamp Gain is common gain for R, G, B channel and used for auto exposure control. Programmable range is from 0.5X ~ 16.5X. Default gain is 2.5X.
Gain = 0.5 + B<7:0>/16

Preamp Gain Min [PgaMin : 18h : 14h]

7	6	5	4	3	2	1	0
Preamp Gain Min							
0	0	0	1	0	1	0	0

Preamp Gain Min is minimum value of preamp gain when sensor adjusts pre-amplifier gain for auto exposure control. Programmable range is same as preamp gain. Recommended value is 0.5X.

Preamp Gain Max [PgaMax : 19h : ffh]

7	6	5	4	3	2	1	0
Preamp Gain Max							
1	1	1	1	1	1	1	1

Preamp Gain Max is maximum value of preamp gain when sensor adjusts preamp gain for auto exposure control. Programmable range is same as preamp gain. Recommended value is 16.5X.

Preamp Gain Normal [PgaNom : 1ah : 20h]

7	6	5	4	3	2	1	0
Preamp Gain Normal							
0	0	1	0	0	0	0	0

Preamp Gain Normal is reference value of preamp gain when sensor adjusts preamp gain for auto exposure control. First, sensor controls integration time before adjusting preamp gain for auto exposure control. After integration time is changed to the minimum or maximum value, sensor adjusts preamp gain from this register value. Programmable range is same as preamp gain. Recommended value is 1.5X.

Analog control A [ACTRA : 1bh : 37h]

7	6	5	4	3	2	1	0
reserved	Pixel Bias			Amp Bias			
0	0	1	1	0	1	1	1

CDS Bias[6:4]	controls the amount of current in CDS bias circuit to amplify CDS output effectively. The larger register value increases the amount of current.
Amplifier Bias[3:0]	controls the amount of current in internal amplifier bias circuit to amplify pixel output effectively. The larger register value increases the amount of current.

Reset Clamp [ACTRB : 1ch : 7fh]

7	6	5	4	3	2	1	0
Reset Level Clamp				ADC Bias			
0	1	1	1	1	1	1	1

Reset Clamping[7:4]	Because extremely bright image like sun affects reset data voltage of pixel to lower, bright image is captured as black image in image sensor regardless of correlated double sampling. To solve this extraordinary phenomenon, we adopt the method to clamp reset data voltage. Reset Level Clamp controls the reset data voltage to prevent inversion of extremely bright image. The larger register value clamps the reset data level at highest voltage level. Default value is 7 to clamp the reset data level at appropriate voltage level.
ADC Bias[3:0]	ADC Bias controls the amount of current in ADC bias circuit to operate ADC effectively. The larger register value increases the amount of current.

Red Pixel Black Offset [ORedl : 21h : 3fh]

7	6	5	4	3	2	1	0
Red Pixel Black Offset							
0	0	1	1	1	1	1	1

Green Pixel Black Offset [OGrnl : 22h : 3fh]

7	6	5	4	3	2	1	0
Green Pixel Black Offset							
0	0	1	1	1	1	1	1

Blue Pixel Black Offset [OBluI : 23h : 3fh]

7	6	5	4	3	2	1	0
Blue Pixel Black Offset							
0	0	1	1	1	1	1	1

These registers control the offset voltage of ADC that changes the black level value for active pixels, red, green and blue pixel respectively. The registers are internally updated by black level compensation logic, and are read-only registers. Register bit functions are composed as follows.

Pixel Black Offset[7]	The bit specifies whether to subtract or add offset voltage in ADC input for light-shielded pixels.
Pixel Black Offset[6:0]	This value specifies the amount of offset voltage for light-shielded pixels.

Red Pixel Active Offset [ORedU : 24h : RO]

7	6	5	4	3	2	1	0
Red Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

Green Pixel Active Offset [OGrnU : 25h : RO]

7	6	5	4	3	2	1	0
Green Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

Blue Pixel Active Offset [OBluU : 26h : RO]

7	6	5	4	3	2	1	0
Blue Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

These registers control the offset voltage of ADC that changes the black level value for active pixels, red, green and blue pixel respectively. The registers are internally updated by black level compensation logic, and are read-only registers. Register bit functions are composed as follows.

Pixel Active Offset[7]	The bit specifies whether to subtract or add offset voltage in ADC input for active pixels.
Pixel Active Offset[6:0]	This value specifies the amount of offset voltage for active pixels.

Black Level Threshold [BLCTH : 27h : 3fh]

7	6	5	4	3	2	1	0
Black Level Threshold							
1	1	1	1	0	0	1	1

The register specifies the maximum value which determines whether light-shielded pixel output is valid. When light-shielded pixel output exceeds this limit, the pixel is not accounted for black level calculation.

ISP Function Enable [IspFen : 30h : 02h]

7	6	5	4	3	2	1	0
Saturation Suppression Enable	Color Suppression Enable	IspFen[5]	Smooth Filter Enable	Edge Enhance Enable	Edge Algorithm Select	Gamma Correction	IspFen[0]
0	0	0	0	0	0	1	0

Saturation Suppression Enable	0	Disable It always comes to apply the same Saturation [5ch] value in a certain environment.
	1	Enable. If preamp gain[17h] exceeds saturation preamp gain min[60h], saturation value[5ch] is suppressed.
Color Suppression Enable	0	Disable
	1	Enable. Chroma Suppressed U, V output
IspFen[5]	Set '0'	
Smooth Filter Enable	0	Disable.
	1	Enable. If Edge Enhancement is carried out, a image will become very sharp so by using smooth filter we can obtain a slightly soft image.
Edge Enhance Enable	0	Disable.
	1	Enable. In order to generate sharper image edge emphasizes and difference of the section of edge increases.
Edge Algorithm Select	This bit selects edge enhancement algorithm.	
	0	Use the algorithm which makes the line of edge vivid.
	1	Use the algorithm which makes the line of edge embossing.
Gamma Correction	0	Disable. Normal Bayer Output
	1	Enable. Gamma Corrected Bayer Output
IspFen[0]	Set '0'	

ISP Output Format [OutFmt : 31h : 60h]

7	6	5	4	3	2	1	0
reserved	UFirst	YFirst	RGB565 Enable	Clk HSC	Inv VSC	Inv HSC	Inv VCLK
-	1	1	0	0	0	0	0

U First	U pixel in front of V pixel for output data sequence.
Y First	Y pixel in front of U and V pixels for output data sequence.
RGB 565 Enable	Data format of RGB 565 mode is composed with {R[7:3]/G[7:5]}, {G[4:2]/B[7:3]} or {B[7:3]/G[7:5]}, {G[4:2]/R[7:3]}. If OutFmt[5](YFirst) register set to low, data format changes to BGR 565.
Clk HSC	In HSYNC, VCLK is embedded, that is, HSYNC is toggling at VCLK rate during normal HSYNC time
Inv VSC	VSYNC output polarity is inverted
Inv HSC	Do not support.
Inv VCLK	VCLK output polarity is inverted

Dark Noise Cancellation [DncMode : 33h : 41h]

7	6	5	4	3	2	1	0
DNC always performing zone				Dnc Threshold		Dnc Mode Select	
0	1	0	0	0	0	0	1

DNC always performing zone	Dark Noise always performed when 2 neighborhood pixel values are Less then this value x8.	
DNC Threshold	Determines the grade judged to be noise. (Tight)11 - 10 - 01 - 00(Loose)	
DNC Mode Select	10	Dark Noise Cancellation is always performed
	01	Dark Noise Cancellation is performed when Integration Time (73h-75h) exceeds (DNC enable integration Time[35h-36h] *256) or Pre-Amp Gain[17h] > Dnc Gain[34h]
	11, 00	Dark Noise Cancellation is turned off

DNC Enable Gain [DncGain : 34h : 3eh]

7	6	5	4	3	2	1	0
						Dnc Mode Select	
0	0	1	1	1	1	1	0

If Dnc mode[33h] set to "01" and Dnc enable gain exceeds preamp gain[17h], Dnc is enabled.

DNC Enable Int. Time High [DncIntH : 35h : 13h]

7	6	5	4	3	2	1	0
Dark Noise Cancellation							
0	0	0	1	0	0	1	1

DNC Enable Int. Time Mid [DncIntM : 36h : 12h]

7	6	5	4	3	2	1	0
Dark Noise Cancellation							
0	0	0	1	0	0	1	0

For Dnc mode [1:0] at "01", if {DncIntH, DncIntM, and 8'h00} value is smaller than Integration Time[73h - 75 h] , Dnc will operate.

Color Matrix Coefficients

Both of Color Correction and Color Space conversion are implemented by 3x3 matrix operation, so that two stages may be merged into one matrix stage.

Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. For color space conversion matrix, the equation from CCIR-601 standard is normally used. Therefore, the intended single matrix for color correction and color space conversion may be resolved as below.

*Intended single matrix = Color Space Conversion Matrix * Color Correction Matrix*

Intended single matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended single matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer(RealCoefficientValue x 64);

For negative values, CMAxx = TwoComplement(Integer(RealCoefficientValue x 64));

RealCoefficientValue values from –127/64 to 127/64 can be programmed.

CCIR-601 YCbCr color space conversion equation

< Conversion Equation >
Y = (77R + 150G + 29B)/256 Range: 16 ~ 235
Cb = (-44R –87G + 131B)/256 + 128 Range: 16 ~ 240
Cr = (131R – 110G – 21B)/256 + 128 Range: 16 ~ 240

< Reverse Conversion >
R = Y + 1.371(Cr – 128)
G = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B = Y + 1.732(Cb – 128)

In the above equations, R, G, and B are gamma-corrected values

Color Matrix Coefficient 11 [CMA11 : 37h : 2fh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 11							
0	0	1	0	1	1	1	1

Color Matrix Coefficient 12 [CMA12 : 38h : dbh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 12							
1	1	0	1	1	0	1	1

Color Matrix Coefficient 13 [CMA13 : 39h : f6h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 13							
1	1	1	1	0	1	1	0

Color Matrix Coefficient 21 [CMA21 : 3ah : 0fh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 21							
0	0	0	0	1	1	1	1

Color Matrix Coefficient 22 [CMA22 : 3bh : 28h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 22							
0	0	1	0	1	0	0	0

Color Matrix Coefficient 23 [CMA23 : 3ch : 08h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 23							
0	0	0	0	1	0	0	0

Color Matrix Coefficient 31 [CMA31 : 3dh : f5h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 31							
1	1	1	1	0	1	0	1

Color Matrix Coefficient 32 [CMA32 : 3eh : ceh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 32							
1	1	0	0	1	1	1	0

Color Matrix Coefficient 33 [CMA33 : 3fh : 3dh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 33							
0	0	1	1	1	1	0	1

Gamma Segment Start Points

Gamma Segment Start Points specify the start points of nine line segments for piecewise gamma approximation. Current default gamma curve is very selected for optimum gray gradation.

Gamma Segment Point 0 [GmaP0 : 40h : 00h]

7	6	5	4	3	2	1	0
Gamma Segment Point 0							
0	0	0	0	0	0	0	0

Gamma Segment Point 1 [GmaP1 : 41h : 04h]

7	6	5	4	3	2	1	0
Gamma Segment Point 1							
0	0	0	0	0	1	0	0

Gamma Segment Point 2 [GmaP2 : 42h : 12h]

7	6	5	4	3	2	1	0
Gamma Segment Point 2							
0	0	0	1	0	0	1	0

Gamma Segment Point 3 [GmaP3 : 43h : 21h]

7	6	5	4	3	2	1	0
Gamma Segment Point 3							
0	0	1	0	0	0	0	1

Gamma Segment Point 4 [GmaP4 : 44h : 37h]

7	6	5	4	3	2	1	0
Gamma Segment Point 4							
0	0	1	1	0	1	1	1

Gamma Segment Point 5 [GmaP5 : 45h : 55h]

7	6	5	4	3	2	1	0
Gamma Segment Point 5							
0	1	0	1	0	1	0	1

Gamma Segment Point 6 [GmaP6 : 46h : 6bh]

7	6	5	4	3	2	1	0
Gamma Segment Point 6							
0	1	1	0	1	0	1	1

Gamma Segment Point 7 [GmaP7 : 47h : 7dh]

7	6	5	4	3	2	1	0
Gamma Segment Point 7							
0	1-	1	1	1	1	0	1

Gamma Segment Point 8 [GmaP8 : 48h : b4h]

7	6	5	4	3	2	1	0
Gamma Segment Point 8							
1	0	1	1	0	1	0	0

Gamma Segment Point 9 [GmaP9 : 49h : ddh]

7	6	5	4	3	2	1	0
Gamma Segment Point 9							
1	1	0	1	1	1	0	1

Gamma Slope Values

Gamma Slope Registers are programmed as the integer value of real slope value that is multiplied by 64.

Gamma Segment Slope 0 [GmaS0 : 4ah : 40h]

7	6	5	4	3	2	1	0
Gamma Segment Slope 0							
0	1	0	0	0	0	0	0

Gamma Segment Slope 1 [GmaS1 : 4bh : 4bh]

7	6	5	4	3	2	1	0
Gamma Segment Slope 1							
0	1	0	0	1	0	1	1

Gamma Segment Slope 2 [GmaS2 : 4ch : 3ch]

7	6	5	4	3	2	1	0
Gamma Segment Slope 1							
0	0	1	1	1	1	0	0

Gamma Segment Slope 3 [GmaS3 : 4dh : 2ch]

7	6	5	4	3	2	1	0
Gamma Segment Slope 3							
0	0	1	0	1	1	0	0

Gamma Segment Slope 4 [GmaS4 : 4eh : 1eh]

7	6	5	4	3	2	1	0
Gamma Segment Slope 4							
0	0	0	1	1	1	1	0

Gamma Segment Slope 5 [GmaS5 : 4fh : 16h]

7	6	5	4	3	2	1	0
Gamma Segment Slope 5							
0	0	0	1	0	1	1	0

Gamma Segment Slope 6 [GmaS6 : 50h : 12h]

7	6	5	4	3	2	1	0
Gamma Segment Slope 6							
0	0	0	1	0	0	1	0

Gamma Segment Slope 7 [GmaS7 : 51h : 0eh]

7	6	5	4	3	2	1	0
Gamma Segment Slope 7							
0	0	0	0	1	1	1	0

Gamma Segment Slope 8 [GmaS8 : 52h : 0ah]

7	6	5	4	3	2	1	0
Gamma Segment Slope 8							
0	0	0	0	1	0	1	0

Gamma Segment Slope 9 [GmaS9 : 53h : 09h]

7	6	5	4	3	2	1	0
Gamma Segment Slope 9							
0	0	0	0	1	0	0	1

Inverse Color Space Conversion

Inverse color space conversion transforms YCbCr by RGB. It is a function only about RGB565 format. Default setting value is from CCIR-601 standard.

R = Y + A(Cr-128)

G = Y - B(Cr-128) – C(Cb-128)

B = Y + D(Cb-128)

A : Inverse Color constant for R[54h]

B : Inverse Color constant for G[55h]

C : Inverse Color constant for G[56h]

D : Inverse Color constant for B[57h]

Inverse Color constant for R [RCrconst : 54h : 57h]

7	6	5	4	3	2	1	0
Inverse Color constant for R							
0	1	0	1	0	1	1	1

For inverse color space conversion matrix, this register defines the constant(A) of following equation(CCIR-601 standard). R = Y + A(Cr-128)

Inverse Color constant for G [Gcrconst : 55h : d4h]

7	6	5	4	3	2	1	0
Inverse Color constant for G							
1	1	0	1	0	1	0	0

For inverse color space conversion matrix, this register defines the constant(A) of following equation(CCIR-601 standard). G = Y - A(Cr-128) – B(Cb-128)

Inverse Color constant for G [Gcrconst : 56h : ebh]

7	6	5	4	3	2	1	0
Inverse Color constant for G							
1	1	1	0	1	0	1	1

For inverse color space conversion matrix, this register defines the constant(B) of following equation(CCIR-601 standard). G = Y - A(Cr-128) – B(Cb-128)

Inverse Color constant for B [Bcrconst : 57h : 6eh]

7	6	5	4	3	2	1	0
Inverse Color constant for B							
0	1	1	0	1	1	1	0

For inverse color space conversion matrix, this register defines the constant(A) of following equation(CCIR-601 standard). B = Y + A(Cb-128)

Hue value 1 [HUE1 : 58h : 00h]

7	6	5	4	3	2	1	0
Hue value 1							
0	0	0	0	0	0	0	0

Hue value 2 [HUE2 : 59h : 80h]

7	6	5	4	3	2	1	0
Hue value 2							
1	0	0	0	0	0	0	0

Hue factor for hue adjustment. Rotate angle range : -30° ~ +30°

<Hue Reg Setting Parameter>

* HUE1 or HUE2 value is multiplied by 128

Angle (˚)	HUE1 (hex)	HUE2 (hex)	Angle (˚)	HUE1 (hex)	HUE2 (hex)	Angle (˚)	HUE1 (hex)	HUE2 (hex)
-30	C0	6E	-9	EC	7E	12	1A	7D
-29	C2	6F	-8	EF	7E	13	1C	7C
-28	C4	71	-7	F1	7F	14	1E	7C
-27	C6	72	-6	F3	7F	15	21	7B
-26	C8	73	-5	F5	7F	16	23	7B
-25	CA	74	-4	F8	7F	17	25	7A
-24	CC	74	-3	FA	7F	18	27	79
-23	CE	75	-2	FC	7F	19	29	79
-22	D1	76	-1	FE	7F	20	2B	78
-21	D3	77	0	00	80	21	2D	77
-20	D5	78	1	02	7F	22	2F	76
-19	D7	79	2	04	7F	23	32	75
-18	D9	79	3	06	7F	24	34	74
-17	DB	7A	4	08	7F	25	36	74
-16	DD	7B	5	0B	7F	26	38	73
-15	DF	7B	6	0D	7F	27	3A	72
-14	E2	7C	7	0F	7F	28	3C	71
-13	E4	7C	8	11	7E	29	3E	6F
-12	E6	7D	9	14	7E	30	40	6E
-11	E8	7D	10	16	7E			
-10	EA	7E	11	18	7D			

Contrast value [Contrast : 5ah : 80h]

7	6	5	4	3	2	1	0
Contrast value							
1	0	0	0	0	0	0	0

Contrast factor for contrast adjustment. Programmable range of Contrast value is 0.1 ~ 1.99.

The Contrast value is same as Saturation value.

Brightness value [Brightness : 5bh : 00h]

7	6	5	4	3	2	1	0
Brightness value							
0	0	0	0	0	0	0	0

Brightness adjustment is performed for summing Y data and brightness value. Brightness value is two's complement and its range is -127 ~ +128.

Bright Y = Y data + brightness value.

For positive value, Brightness[7:0] = Two's complement(integer)

Saturation value [Saturation : 5ch : 80h]

7	6	5	4	3	2	1	0
Saturation value							
1	0	0	0	0	0	0	0

Saturation adjustment is performed for multiplying Cr,Cb data by saturation value. Programmable range of saturation value is 0.1 ~ 1.99. For instance, Sat Cb,Cr = Cb,Cr data * Satuation[7:0] / 256

< Contrast & Saturation parameter >

* Contrast or Saturation Value is multiplied by 128

Number	Contrast & Saturation (hex)	Number	Contrast & Saturation (hex)
0.1	0D	1.1	8D
0.2	1A	1.2	9A
0.3	26	1.3	A6
0.4	33	1.4	B3
0.5	40	1.5	C0
0.6	4D	1.6	CD
0.7	5A	1.7	DA
0.8	66	1.8	E6
0.9	73	1.9	F3
1.0	80	1.99	FF

Edge Weight Control value [EgWtCon : 5dh : 00h]

7	6	5	4	3	2	1	0
Reserved				Edge Weight			
0	0	0	0	0	0	0	0

Edge weight : 0 -> 0.5 ~ f -> 8 0. Weight increases by 0.5 step and divides into 16 step.

Edge Enhancement Vth Low [EdThLo : 5eh : 10h]

7	6	5	4	3	2	1	0
Edge Enhancement Vth Low							
0	0	0	1	0	0	0	0

If edge value is higher than this register value, edge enhancement is enabled.

Suppression Pre Amp Gain Min [SupGMin : 60h : 24h]

7	6	5	4	3	2	1	0
Suppression Pre Amp Gain Min							
0	0	1	0	0	1	0	0

If preamp gain value is higher than this register value and Color Suppression Enable[30h] is HIGH, color suppression is enabled.

Saturation Pre Amp Gain Min [SatGMin : 61h : 24h]

7	6	5	4	3	2	1	0
Saturation Pre Amp Gain Min							
0	0	1	0	0	1	0	0

If preamp gain value is higher than this register value and Saturation Suppression Enable[30h] is HIGH, saturation suppression is enabled.

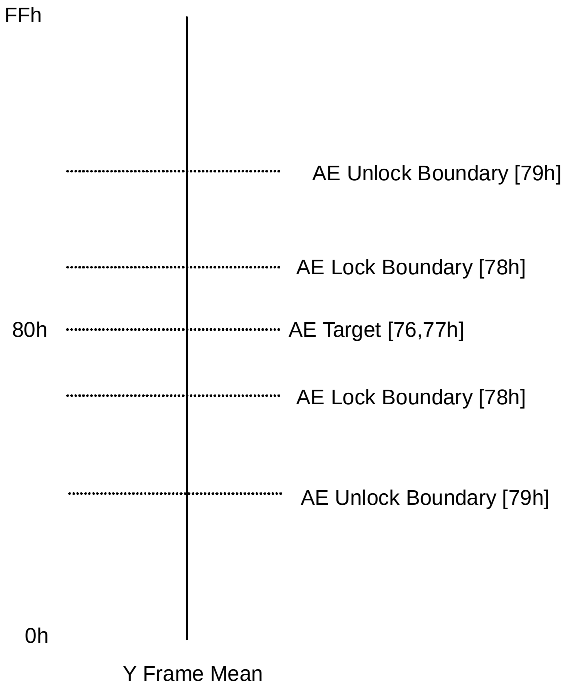
Edge Pre Amp Gain Min [EgeGMin : 62h : 24h]

7	6	5	4	3	2	1	0
Edge Pre Amp Gain Min							
0	0	1	0	0	1	0	0

If preamp gain value is higher than this register value and Edge Enhancement Enable[30h] is HIGH, edge suppression is enabled. Edge suppression is a function that edge weight decreases in dark environment automatically.

Auto Exposure

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to the displacement between current frame Y mean value and target Y mean value.



AE Mode 1 [AEMODE1 : 70h : 29h]

7	6	5	4	3	2	1	0
AEMODE1 [7]	Anti-Banding Enable	Anti-Banding Minimum Break	AeWinEn	Time Speed		AE Mode	
0	0	1	0	1	0	0	1

AEMODE1[7]	Set ‘0’

Anti-Banding Enable	When Anti-Banding is enabled, AE initializes Integration Time registers to 4 x Anti-Banding Step value, and integration increment/decrement amount is set to Anti-Banding Step value in order to remove banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition. In this mode, AE operates with very large unit, typically a reciprocal of (2 x power line frequency), so that minute integration time tuning is not liable. Therefore, this mode is recommended for only indoor use.
Anti-Banding Minimum Break	When AE is still of out lock state despite that AE preamp analog gain update value exceeds preamp minimum gain value(18h) and integration time(73h-75h) is reached to AE Anti-Banding Step(7ah-7ch), integration time(73h-75h) is broken to less than AE Anti-Banding Step(7ah-7ch).
AeWinEn	This bit uses during calculating the average of Y value at present frame for AE. When this bit is HIGH, AE Window Weight is equal. If not, calculate the average of Y using AE Window Weight.
Time Speed	(fast)11 - 10 - 01 - 00(slow)
AE Mode	11: Gain-Only control mode. Only preamp gain is controlled to get optimum exposure state. 10: Time-Only control mode. Only integration time is controlled to get optimum exposure state. 01: Time-Gain control mode. integration time and preamp gain are controlled to get optimum exposure state. 00: AE function is disabled

AE Mode 2 [AEMODE2 : 71h : edh]

7	6	5	4	3	2	1	0
Gain Speed 1		Gain Speed 2		Time Fine	Gain Fine	EnDGain	EnAGain
1	1	1	0	1	1	0	1

Gain Speed1	This Speed Only worked from dark luminance condition to white luminance condition rapidly. (fast)11 - 10 - 01 - 00(slow)

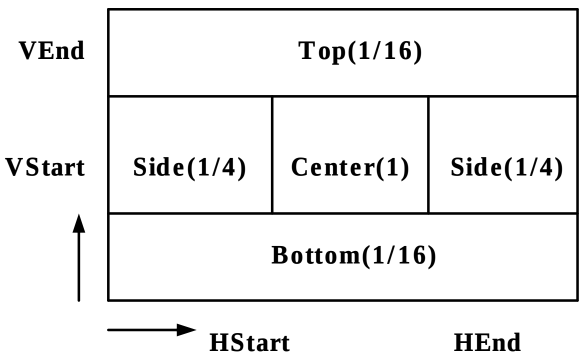
Gain Speed2	It's about situation except the case of Gain Speed 1. Gain update speed is specified as follows. (fast)11 - 10 - 01 - 00(slow)
Integration Time Fine Tune	Integration time fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly.
Preamp Gain Fine Tune	Preamp gain fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly.
Enable Digital Gain	If Pre-Amp Gain(17h) is less then Anti-Banding Gain Min(91h), Bayer pixel value are gained by ratio of Anti-Banding Gain Min / Pre-Amp Gain when this register value set to high.
AE Analog Gain Control	AE updates preamp gain register(17h) in order to reach optimum exposure state

AE Windows Weight [AEWINWGT : 72h : cdh]

7	6	5	4	3	2	1	0
Top window		Center window		Bottom window		Side window	
1	1	0	0	1	1	0	1

When calculate the average of Y, each window is able to have different weight.
Bottom Window in sensor means Top Window in display.

Value	Weight
'Zro	1
'One	1/4
'Two	1/8
'Tri	1/16



Integration Time High [INTH: 73h : 02h]

7	6	5	4	3	2	1	0
Integration Time High [23:16]							
0	0	0	0	0	0	1	0

Integration Time Middle [INTM: 74h: 71h]

7	6	5	4	3	2	1	0
Integration Time Middle[15:8]							
0	1	1	1	0	0	0	1

Integration Time Low [INTL: 75h: 00h]

7	6	5	4	3	2	1	0
Integration Time Low[7:0]							
0	0	0	0	0	0	0	0

Integration time value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time of general camera so that integration time need to be increased in dark environment and decreased according to lighting condition. Maximum integration time is register maximum value(2^{24}-1) x sensor clock period(80ns, SCF 12.5Mhz @ DCF 25Mhz) = 1.34sec.

AE Target OutDoor [LuTarget1 : 76h : 5ah]

7	6	5	4	3	2	1	0
AE Target OutDoor							
0	1	0	1	1	0	1	0

This register defines the target luminance value for AE operation in outdoor.

AE Target InDoor[LuTarget2 : 77h : 5ah]

7	6	5	4	3	2	1	0
AE Target InDoor							
0	1	0	1	1	0	1	0

This register defines the target luminance value for AE operation in indoor.

AE Lock Boundary [AeLockFineBnd : 78h : f6h]

7	6	5	4	3	2	1	0
AE Fine Boundary				AE Lock Boundary			
1	1	1	1	0	1	1	0

AE Lock Boundary specifies the displacement of Y Frame Mean value(8eh) from AE Target in which AE goes into LOCK state. With Anti-Banding is enabled, this displacement condition is discarded, and instead AE Speed Unlock Boundary is used as Lock boundary.

AE Fine Boundary specifies the displacement of Y Frame Mean value(8eh) from AE Target in which AE start to tune fine integration time or preamp gain in order to goes into lock state smoothly.

AE Unlock Boundary [AeUnlockBnd : 79h : 2ah]

7	6	5	4	3	2	1	0
AE Unlock Boundary							
0	0	1	0	1	0	1	0

AE Unlock Boundary specifies Y Frame Mean displacement from AE Target in which AE goes into UNLOCK state. In this state, integration time increment/decrement speed changes from 2x (integration unit step) to 1x (integration unit step). In anti-banding mode, this boundary is used as lock boundary for exposure control.

AE Anti-Flicker Step High [AeIntStepH : 7ah : 01h]

7	6	5	4	3	2	1	0
reserved						AE Anti-Flicker Step High	
0	0	0	0	0	0	0	1

AE Anti-Flicker Step Middle [AeIntStepM : 7bh : 38h]

7	6	5	4	3	2	1	0
AE Anti-Flicker Step High							
0	0	1	1	1	0	0	0

AE Anti-Flicker Step Low [AeIntStepL : 7ch : 80h]

7	6	5	4	3	2	1	0
AE Anti-Flicker Step Low							
1	0	0	0	0	0	0	0

AE Anti-Banding Step specifies integration time unit value that AE uses when Anti-Banding is enabled. Anti-Banding Step value is resolved by the following equation.

Anti-Banding Step Value = Sensor Operation Frequency (SCF) / (2x power line frequency)

The default value is set with SCF 12.5Mhz, 50Hz power line, that is,

Anti-Banding Step Value = 12.5Mhz / (2 x 50) = 125000d = 1e848h

To operate stably, AE Anti-Flicker Step Low [1:0] bits have to '00'.

So, Anti-Banding Step Value at HV7131RP is (1e848h & fffffch = 1e848h)

AE Maximum Limit High [AeIntLimitH : 7dh : 09h]

7	6	5	4	3	2	1	0
AE Maximum Limit High							
0	0	0	0	1	0	0	1

AE Maximum Limit Middle [AeIntLimitM : 7eh : c4h]

7	6	5	4	3	2	1	0
AE Maximum Limit Middle							
1	1	0	0	0	1	0	0

AE Maximum Limit Low [AeIntLimitL : 7fh : 00h]

7	6	5	4	3	2	1	0
AE Maximum Limit Low							
0	0	0	0	0	0	0	0

These three registers define the maximum integration time value that is allowed to sensor operation. It is desirable to set the value to multiples of AE Anti-Banding Step to easily operate with Anti-banding mode enabled. The default value is set to 1/8sec with SCF set to 25Mhz

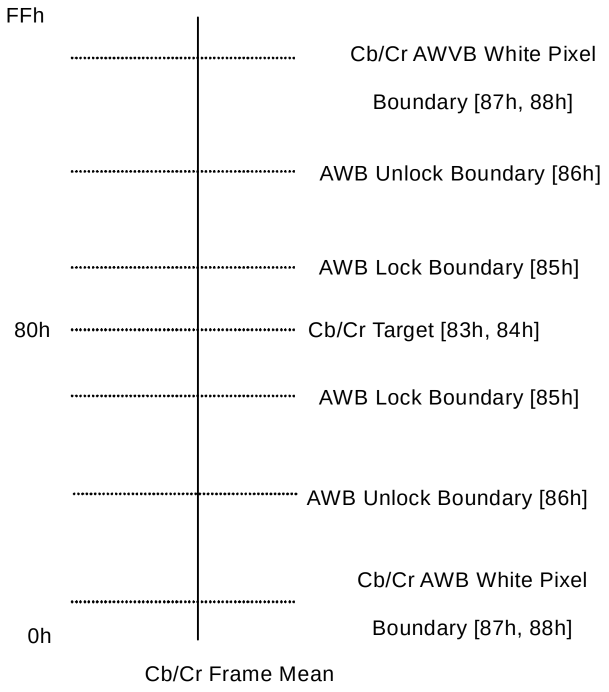
12.5Mhz / 8 = 1,562,500 = 17d784

To operate stably, AE Maximum Limit Low [1:0] bits have to '11'.

So, AE Maximum Limit at HV7131RP is (17d784h | 000003h = 17d787h)

Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.



AWB Mode [AWBMode : 80h : 18h]

7	6	5	4	3	2	1	0
reserved	AtoTstEn	Csp Val En	Awb Enable	AWB Window Enable	AWB Speed		AWB Mode[0]
-	0	0	1	1	0	0	0

AtoTstEn	This value is using at only simulation or test.
Csp Val En	When this bit set to high, color matrix coefficient [CMA11 ~ CMA33] is used for for color space conversion matrix. And if this bit set to low, the equation from CCIR-601 is used.

Awb Enable	Auto White Balance Control Enabled. AWB is carried out only when satisfying all the following cases. - the displacement of Cb/Cr Frame Mean value from AWB Target is larger than AWB Lock Boundary - the displacement of Cb/Cr Frame Mean value from AWB Target is smaller than AWB White Pixel Boundary - the displacement of the sum of Cb target and Cr target from the sum of average of Cb and Cr is smaller than AWB C Boundary
AWB Window Enable	This bit uses during calculating the average of Cb/Cr value at present frame for AWB. When this bit is HIGH, AWB Window Weight is equal. If not, calculate the average of Cb/Cr using AWB Window Weight.
AWB Speed	(Fast)11 - 10 - 01 - 00(slow)
AWB Mode[0]	Set '0'

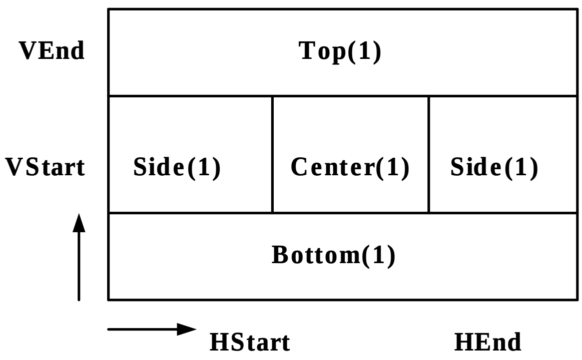
AWB Windows Weight [AwbWinWgt : 82h : 00h]

7	6	5	4	3	2	1	0
Top window		Center window		Bottom window		Side window	
0	0	0	0	0	0	0	0

When calculate the average of Cb/Cr, each window is able to have different weight.

Bottom Window in sensor means Top Window in display.

Value	Weight
'Zro	1
'One	1/4
'Two	1/8
'Tri	1/16



AWB Cb Target Position [CbTarget : 83h : 80h]

7	6	5	4	3	2	1	0
AWB Cb Target Position							
1	0	0	0	0	0	0	0

This register defines Cb target frame mean value for AWB operation.

AWB Cr Target Position [CbTarget : 84h : 80h]

7	6	5	4	3	2	1	0
AWB Cr Target Position							
1	0	0	0	0	0	0	0

This register defines Cr target frame mean value for AWB operation.

AWB Lock Boundary [AwbLockBnd : 85h : 02h]

7	6	5	4	3	2	1	0
reserved				AWB Lock Boundary			
0	0	0	0	0	0	1	0

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (83h-84h) value where AWB goes into LOCK state.

AWB Unlock Boundary [AwbUnlockBnd : 86h : 20h]

7	6	5	4	3	2	1	0
AWB Unlock Boundary							
0	0	1	0	0	0	0	0

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (83h-84h) where AWB is released from LOCK state. AWB operation retains LOCK state unless Cb/Cr frame mean values' displacement value exceeds this boundary. The value should be larger AWB Lock Boundary.

AWB Cb White Pixel Boundary [CbWhiteBnd : 87h : 30h]

7	6	5	4	3	2	1	0
AWB Cb White Pixel Boundary							
0	0	1	1	0	0	0	0

When Cb frame mean values' displacement from Cb Target exceeds AWB White Pixel Boundary value, AWB accept frame color as it is and does not try to correct white balance deviation.

AWB Cr White Pixel Boundary [CrWhiteBnd : 88h : 30h]

7	6	5	4	3	2	1	0
AWB Cr White Pixel Boundary							
0	0	1	1	0	0	0	0

When Cr frame mean values' displacement from Cr Target exceeds AWB White Pixel Boundary value, AWB accept frame color as it is and does not try to correct white balance deviation.

AWB C Boundary [AwbCBnd : 89h : 30h]

7	6	5	4	3	2	1	0
AWB C Boundary							
0	0	1	1	0	0	0	0

In case of the single color which is not a light source, this register uses in order not to operate AWB.

R/B Gain Max [AwbGainMax : 8ah : 3f]

7	6	5	4	3	2	1	0
R/B Gain Max							
0	0	1	1	1	1	1	1

The register specifies maximum boundary of AWB R/B gain

R/B Gain Min [AwbGainMin : 8bh : 00]

7	6	5	4	3	2	1	0
R/B Gain Min							
0	0	0	0	0	0	0	0

The register specifies minimum boundary of AWB R/B gain

AE State Machine [AeFSM : 8ch : RO]

7	6	5	4	3	2	1	0
AE Mode State				AE Lock state			
RO	RO	RO	RO	RO	RO	RO	RO

AE Mode State	This nibble represents the mode where internal Y plane FSM is currently placed among time-gain control, time-only control, or gain-only control modes. "0000" : outdoor exposure control in anti-banding enabled "0001" : gain negative control mode

	"0010" : exposure bidirectional control state "0011" : gain positive control mode "0100" : exposure only control mode "0101" : gain only control mode
AE Lock State	Y channel FSM status "0000" means that AE Y plane is in lock state "0001" means that AE Y plane is in unlock state "0010" means that AE Y plane is in far state

AWB State Machine [AwbFSM : 8dh : RO]

7	6	5	4	3	2	1	0
reserved			AE/AWB Lock	Cb Lock State		Cr Lock State	
RO	RO	RO	RO	RO	RO	RO	RO

AE/AWB Lock	This single status bit indicates that AE and AWB are in lock state for optimum still image capture.
Cb Lock State	Cb channel FSM status. "00" means that AWB Cb plane is in lock state.
Cr Lock State	Cr channel FSM status. "00" means that AWB Cr plane is in lock state

Lu Frame Mean [LuFMean : 8eh : RO]

7	6	5	4	3	2	1	0
Lu Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Y plane frame mean value.

Cb Frame Mean [CbFMean : 8fh : RO]

7	6	5	4	3	2	1	0
Cb Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Cb plane frame mean value.

Cr Frame Mean [CrFMean : 90h : RO]

7	6	5	4	3	2	1	0
Cr Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Cr plane frame mean value.

Anti-Banding Gain Min [KlBndMin : 91h : 14h]

7	6	5	4	3	2	1	0
Anti-Banding Gain Min							
0	0	0	1	0	1	0	0

The register specifies the minimum limit to which AE may decrease preamp gain or Y digital gain in order to get optimum exposure value while Anti-Banding Mode is enabled and the following condition is met.

AE Lock Boundary < (Y Frame Mean - AE Target) < AE Unlock Boundary.

Anti-Banding Gain Max [KlBndMax : 92h : 3dh]

7	6	5	4	3	2	1	0
Anti-Banding Gain Max							
0	0	1	1	1	1	0	1

The register specifies the maximum limit to which AE may increase preamp gain or Y digital gain in order to get optimum exposure value while Anti-Banding Mode is enabled and the following condition is met.

AE Lock Boundary < (AE Target - Y Frame Mean) < AE Unlock Boundary.

AWB White Pixel Boundary [AwbWhite : 93h : ffh]

7	6	5	4	3	2	1	0
AWB White Pixel Boundary							
1	1	1	1	1	1	1	1

During Cb, Cr frame mean value calculation, AWB discards pixel of which luminance is larger than this register value.

AWB Black Pixel Boundary [AwbBlack : 94h : 00h]

7	6	5	4	3	2	1	0
AWB Black Pixel Boundary							
0	0	0	0	0	0	0	0

During Cb, Cr frame mean value calculation, AWB discards pixel of which luminance is smaller than this register value.

AWB Valid Number [AwbNumber : 95h : 02h]

7	6	5	4	3	2	1	0
AWB Valid Number							
0	0	0	0	0	0	1	0

AWB update when the number of valid color pixel is larger than (this valid value x 64).

Integration-Scan Plane Offset High [IntScn0fsH : 96h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset High							
RO	RO	RO	RO	RO	RO	RO	RO

Integration-Scan Plane Offset Middle [IntScn0fsM : 97h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset Middle							
RO	RO	RO	RO	RO	RO	RO	RO

Integration-Scan Plane Offset Low [IntScn0fsL : 98h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset Low							
RO	RO	RO	RO	RO	RO	RO	RO

The register represents time offset between integration plane and scan plane. The value should be the same as the value specified by integration time register(73h – 75h).

Frame Timing

For clear description of frame timing, clocks' acronym and relation are reminded in here again.

< Clock Acronym Definition >

MCF : Master Clock Frequency	DCF : Divided Clock Frequency
SCF : Sensor Clock Frequency	ICF : Image Processing Clock Frequency
VCF : Video Clock Frequency	LCF : Line Clock Frequency

< Clock Frequency Relation >

MCF : MCF	DCF : MCF/Clock Division	
SCF : DCF/2	ICF	SCF for No Scale Image mode, SCF/2 for 2 X 2 subsampling mode SCF/4 for 2 X 6 subsampling mode
VCF : ICF*2 for 8bit output	LCF : 1/(HBLANK Period + HSYNC Period)	

HBLANK Period : HBLANK Time register value * (1/SCF)

HSYNC Period : HSYNC Active Time

< Frame Time Calculation >

Core Frame Time is

(IDLE SLOT + Video Height * LCP)

and Real Frame Time is resolved as follows.

When Integration Time > Core Frame Time, Real Frame Time is (Integration Time + VBLANK * LCP), otherwise is (Core Frame Time + VBLANK * LCP).

1. No Scale Image Timing

No Scale Image Frame Timing Related Parameters			
Master Clock Frequency(MCF)	20Mhz	Divided Clock Frequency(DCF)	MCF/1 = 20Mhz
Sensor Clock Frequency(SCF)	DCF/2 = 10Mhz	Sensor Clock Period(SCP)	1/10Mhz = 100ns
Window Width	640	Window Height	480
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 SCPs
Output Bus Width	8bit	VGA Video Output Frequency	SCF * 2 = 20Mhz
Final Video Output Size	640x480	.	.

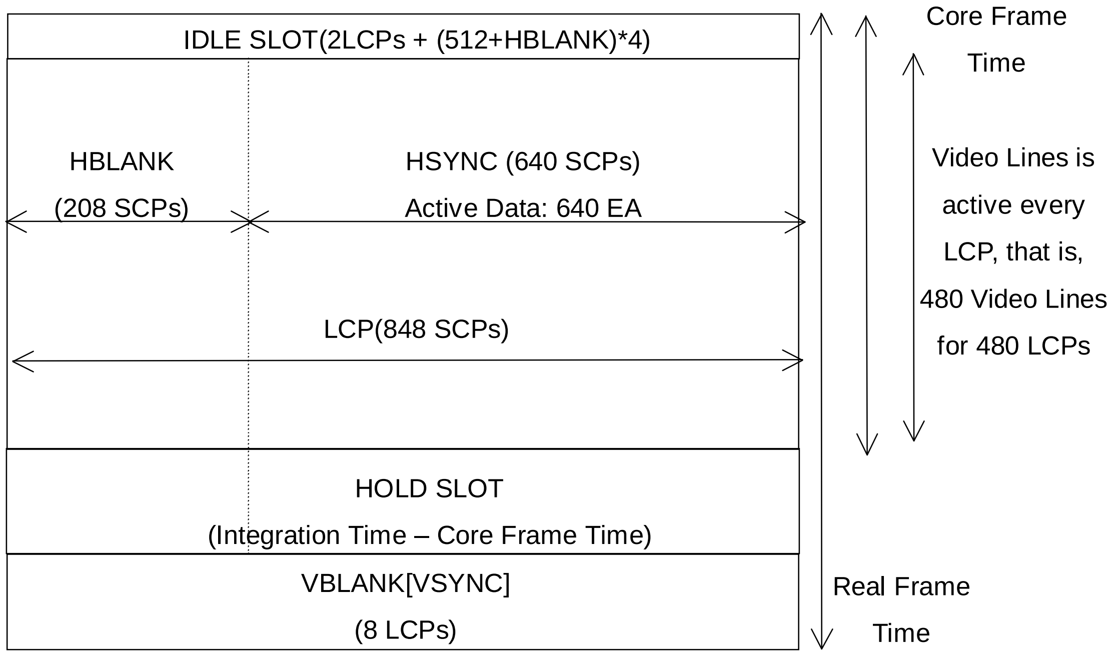
If Integration Time < Core Frame Time, Real Frame Time is

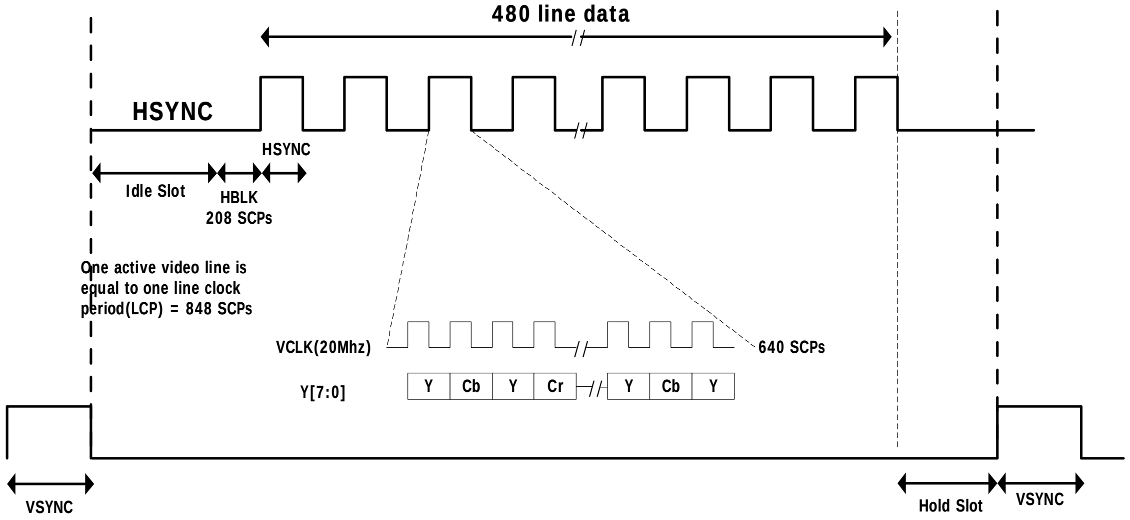
2 * (208 + 640) SCPs + 480 * (208 + 640) SCPs + 8 * (208 + 640) SCPs = 415520 SCPs = 0.041552sec

else Real Frame Time is

Integration Time * SCPs + 8 * (208 + 640) SCPs.

HOLD SLOT in frame timing appears only if integration time is larger than core frame time.

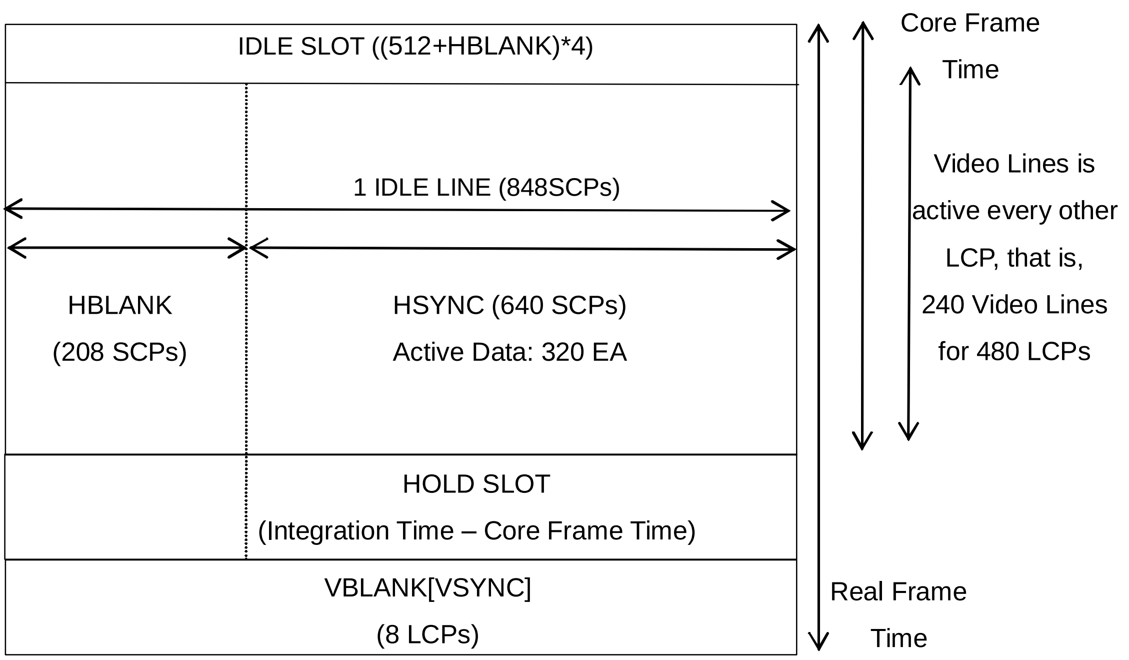


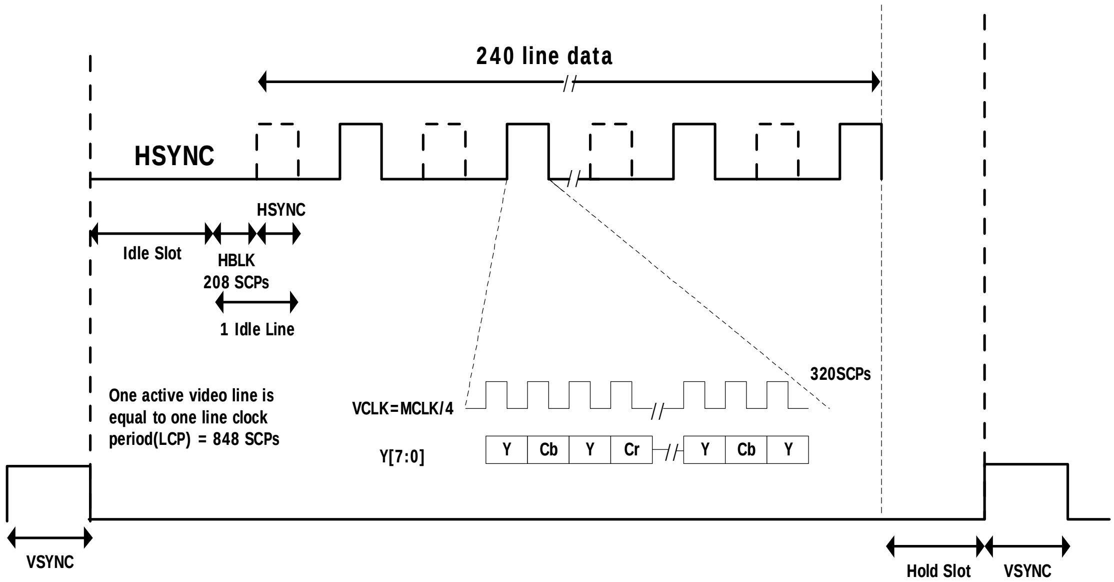

480 line data
HSYNC
HSYNC
Idle Slot
HBLK
208 SCPs
One active video line is
equal to one line clock
period(LCP) = 848 SCPs
VCLK(20Mhz)
640 SCPs
Y[7:0]
Y
Cb
Y
Cr
Y
Cb
Y
VSYNC
Hold Slot
VSYNC

2. 2x2 Subsampling Timing

2 X 2 Subsampling Frame Timing Related Parameters			
Master Clock Frequency(MCF)	20Mhz	Divided Clock Frequency(DCF)	MCF/1 = 20Mhz
Sensor Clock Frequency(SCF)	DCF/2 = 10Mhz	Sensor Clock Period(SCP)	1/10Mhz = 100ns
Window Width	640	Window Height	480
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 * 2 SCPs
Output Bus Width	8bit	SIF Video Output Frequency	SCF * 1 = 10Mhz
Final Video Output Size	320x240		

In 2 X 2sub-sampling mode, valid video data is produced every other line, i.e. for 480 LCPs, active video lines are 240. HSYNC active time is equal to HSYNC active time of No Scale Image mode, but video clock frequency is half of No Scale Image mode's to produce half size output in horizontal direction.

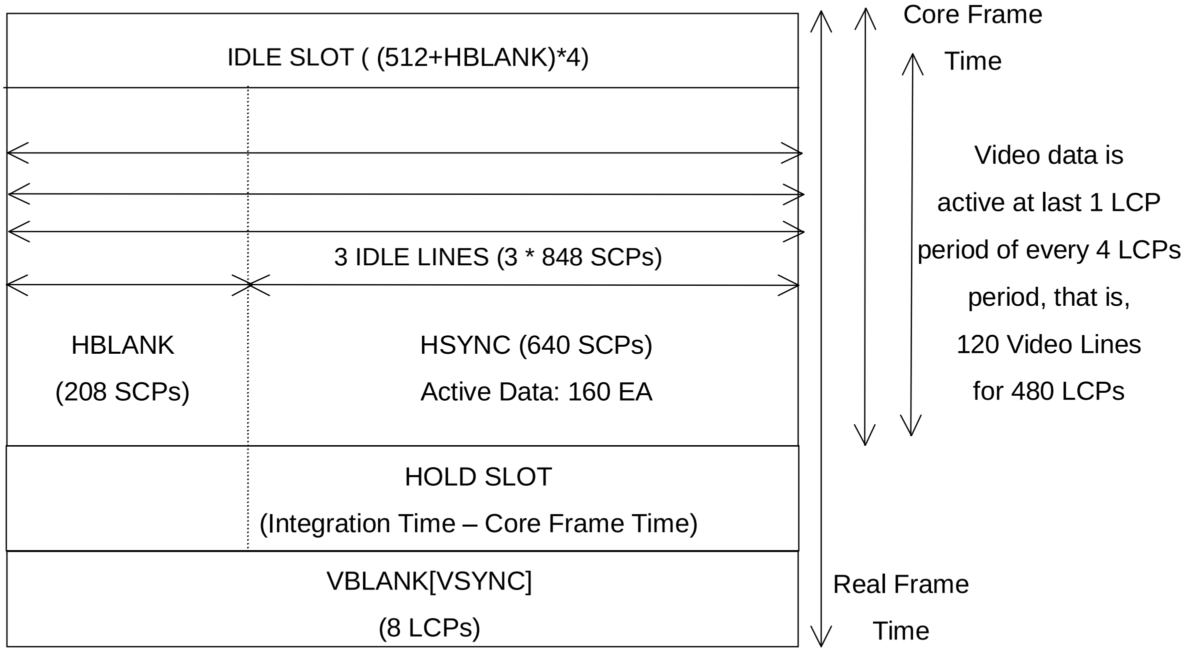


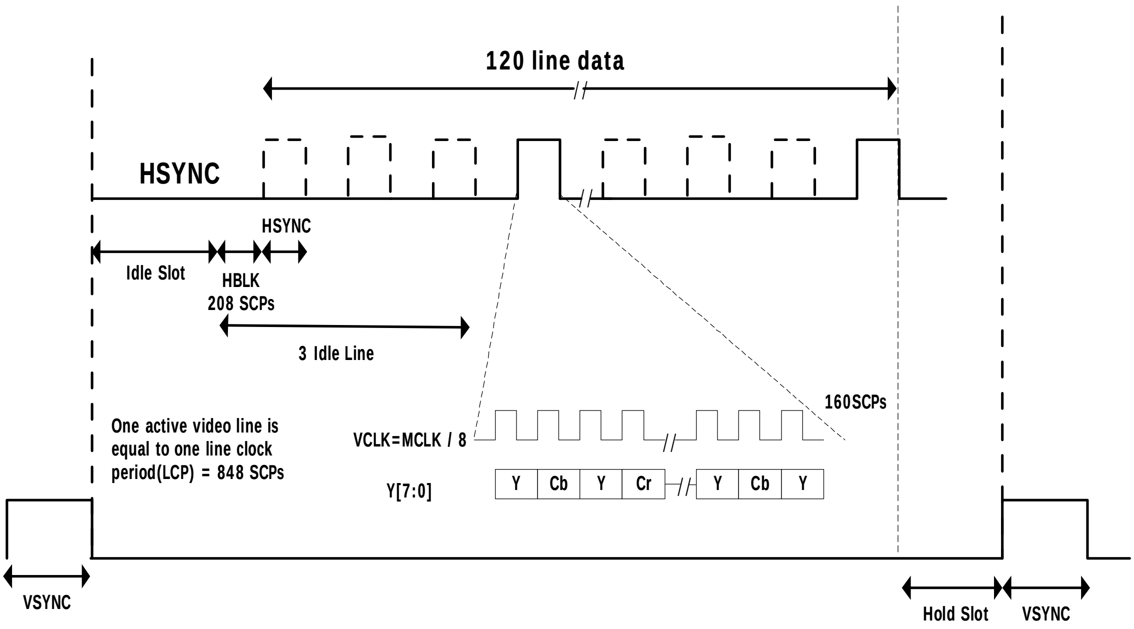


3. 2 X 6 Subsampling Timing

2 X 6 Subsampling Frame Timing Related Parameters			
Master Clock Frequency(MCF)	20Mhz	Divided Clock Frequency(DCF)	MCF/1 = 20Mhz
Sensor Clock Frequency(SCF)	DCF/2 = 10Mhz	Sensor Clock Period(SCP)	1/10Mhz = 100ns
Window Width	640	Window Height	480
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 * 4 SCPs
Output Bus Width	8bit	QSIF Video Output Frequency	SCF / 2 = 5Mhz
Final Video Output Size	160x120		

In 2 X 6 subsampling mode, valid video data is produced every four line, i.e. for 480 LCPs, active video lines are 120. HSYNC active time is equal to HSYNC active time of No Scale Image mode, but video clock frequency is a quarter of No Scale Image mode's to produce a quarter size output in horizontal direction.


IDLE SLOT ((512+HBLANK)*4)
3 IDLE LINES (3 * 848 SCPs)
HBLANK
(208 SCPs)
HSYNC (640 SCPs)
Active Data: 160 EA
HOLD SLOT
(Integration Time – Core Frame Time)
VBLANK[VSYNC]
(8 LCPs)
Core Frame
Time
Video data is
active at last 1 LCP
period of every 4 LCPs
period, that is,
120 Video Lines
for 480 LCPs
Real Frame
Time


120 line data
HSYNC
HSYNC
Idle Slot
HBLK
208 SCPs
3 Idle Line
160SCPs
One active video line is
equal to one line clock
period(LCP) = 848 SCPs
VCLK=MCLK / 8
Y[7:0]
Y
Cb
Y
Cr
Y
Cb
Y
VSYNC
Hold Slot
VSYNC

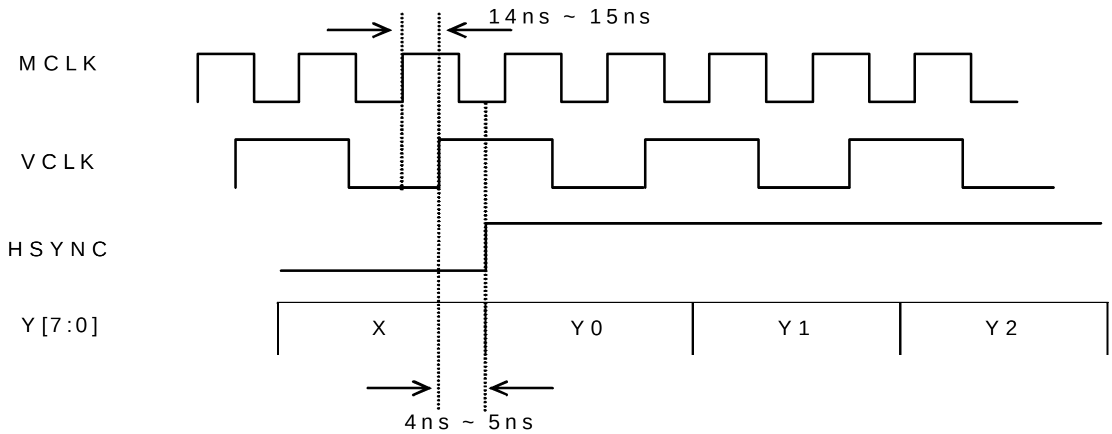
Anti-Banding Configuration

For Anti-Banding mode to work correctly, the following registers should be configured to the appropriate values.

AE Mode	70h	Anti-Banding Enable[7]
AE Anti-Banding Step	7a-7ch	SCF / (2 x power line frequency)
AE Integration Time Limit	7d-7fh	The value should be multiples of AE Anti-Banding Step

When Anti-Banding is enabled, AE initializes Integration Time registers[73-75h] to 4 x Anti-Banding Step value[7a-7ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove anti-banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition.

Data Output Timing and Interface



As specified in the above data output timing diagram, the timing margin between video clock pin (VCLK) and data pins (Y[7:0]) is about 4ns ~ 5ns. This margin may be sufficient or not according to how much video clock and data pins are delayed internally in the backend chip, respectively. To safely latch the data output in the backend chip, it is recommended that data be latched at negative edge of VCLK.

Output Data according to Video Mode

Output Data according to Video Mode is controlled by configuring Sensor Control A[01h]. Configurable options are specified again for your reference.

< Video Mode Setting >

	Row Sub-Sampling	YCbCr 4:2:2 OUTFMT[6:4] = 6h	RGB 5:6:5 OUTFMT[6:4] = 7h	Bayer SCTRC[7] = 1
VGA(640x480) SCTRA[2:0] = 0h or 3h	ISP(SSSel = 0)	Support	Support	None
	Bayer(SSSel = 1)	Support	Support	Support
QVGA(320x240) SCTRA[2:0] = 2h	ISP(SSSel = 0)	Support	Support	None
	Bayer(SSSel = 1)	Support	Support	Support
QQVGA(160x120) SCTRA[2:0] = 1h	ISP(SSSel = 0)	Support	Support	None
	Bayer(SSSel = 1)	Support	Support	Support
CIF(236x288) SCTRA[2:0] = 8h or Bh	ISP(SSSel = 0)	Support	Support	Not Support
	Bayer(SSSel = 1)	Support	Support	Not Support
QCIF(178x144) SCTRA[2:0] = Ah	ISP(SSSel = 0)	Support	Support	Not Support
	Bayer(SSSel = 1)	Support	Support	Not Support

< Video Mode Setting >

Output Format		Sensor Control A [0x01]	Sensor Control C [0x05]	Output Format [0x31]
YCbCr422 ISP Sub-sampling	VGA (640 x 480)	0x00, 0x03	0x00	0x60
	QVGA (320 x 240)	0x02	0x00	0x60
	QQVGA (160 x 120)	0x01	0x00	0x60
	CIF (356 x 288)	0x08, 0x0b	0x00	0x60
	QCIF (178 x 144)	0x0a	0x00	0x60
YCbCr422 Bayer Sub-sampling	VGA (640 x 480)	0x04, 0x07	0x00	0x60
	QVGA (320 x 240)	0x06	0x00	0x60
	QQVGA (160 x 120)	0x05	0x00	0x60
	CIF (356 x 288)	0x0c, 0x0f	0x00	0x60
	QCIF (178 x 144)	0x0e	0x00	0x60
RGB565 ISP Sub-sampling	VGA (640 x 480)	0x00, 0x03	0x00	0x10
	QVGA (320 x 240)	0x02	0x00	0x10
	QQVGA (160 x 120)	0x01	0x00	0x10
	CIF (356 x 288)	0x08, 0x0b	0x00	0x10
	QCIF (178 x 144)	0x0a	0x00	0x10
RGB565 Bayer Sub-sampling	VGA (640 x 480)	0x04, 0x07	0x00	0x10
	QVGA (320 x 240)	0x06	0x00	0x10
	QQVGA (160 x 120)	0x05	0x00	0x10
	CIF (356 x 288)	0x0c, 0x0f	0x00	0x10
	QCIF (178 x 144)	0x0e	0x00	0x10
Bayer Sub-sampling	VGA (640 x 480)	0x04, 0x07	0x80	0x00
	QVGA (320 x 240)	0x06	0x80	0x00
	QQVGA (160 x 120)	0x05	0x80	0x00

Output timings for general configurations are described below. Slot named as “X” means that it is has no meaningful value and should be discarded.

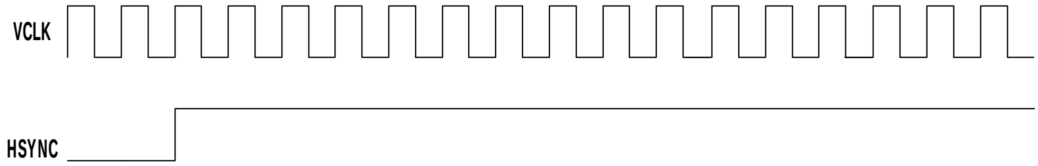
No Scale Image Mode or Sub-sampling (2x2, 2x6) Mode

1. YCbCr 4:2:2 Mode or Sub-sampling (2x2, 2x6) Mode

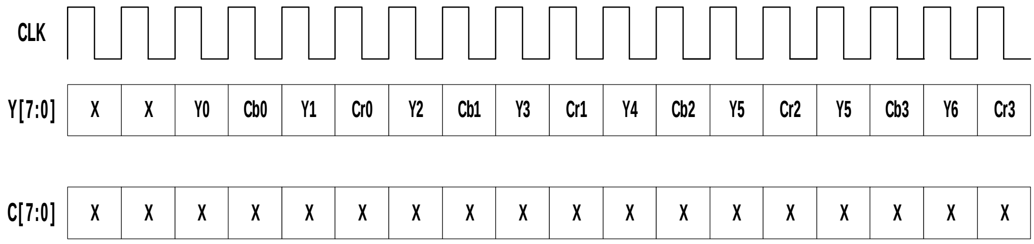
Register bit configurations

Sensor Control A : No Scale Mode or Sub-sampling Mode

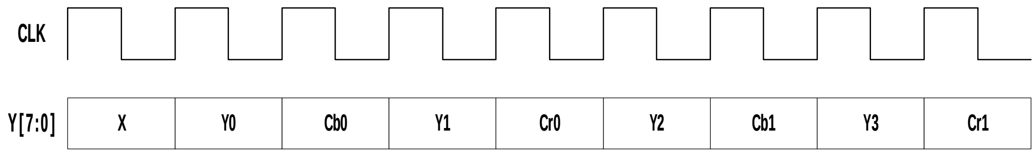
Output Format : 8bit Output, Y First, U First.



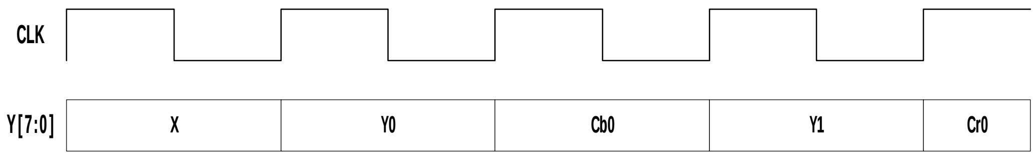
No Scale Mode Video Clock & Output Data



2 X 2 Video Clock & Output Data



2 X 6 Video Clock & Output Data

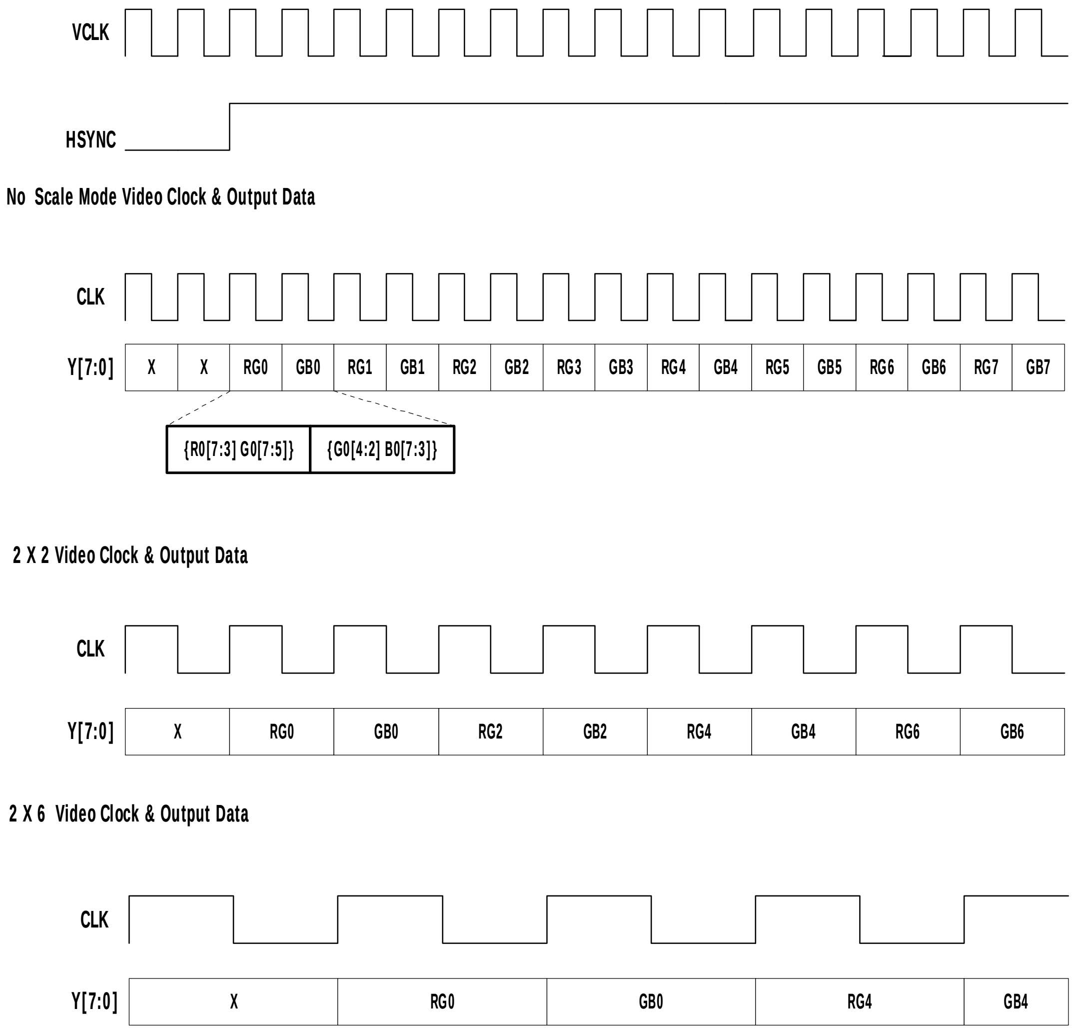


2. RGB565 Mode or Sub-sampling (2x2, 2x6) Mode

Register bit configurations

Sensor Control A : No Scale Mode or Sub-sampling Mode

Output Format : 8bit Output, Y First, U First and RGB565 enable.

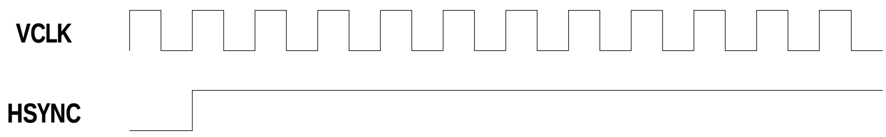


3. Bayer Mode or Sub-sampling (2x2, 2x6) Mode

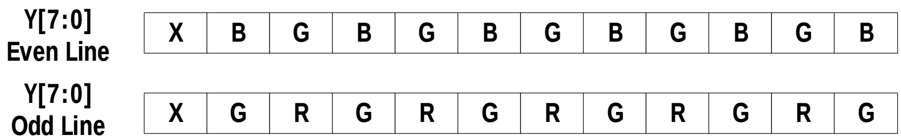
Register bit configurations

Sensor Control A : Bayer Mode(SSSel enable) or Sub-sampling Mode

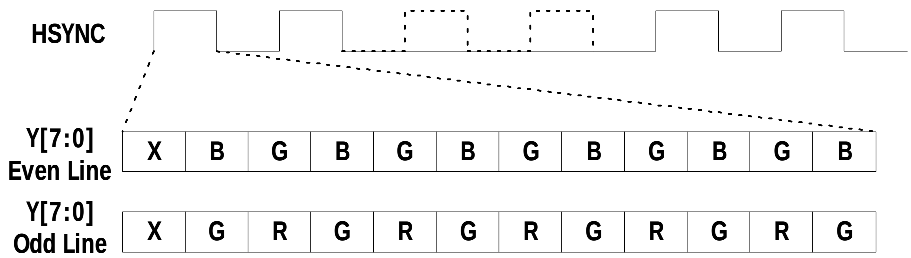
Output Format : 8bit Output, Y First, U First



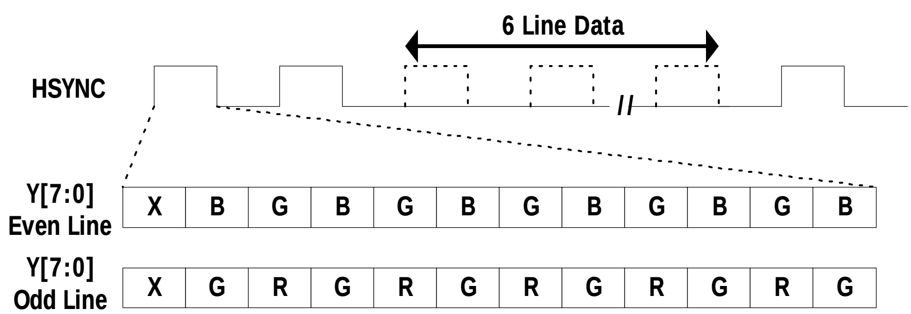
Bayer Mode Video Clock & Output Data



2 X 2 Video Clock & Output Data



2 X 6 Video Clock & Output Data



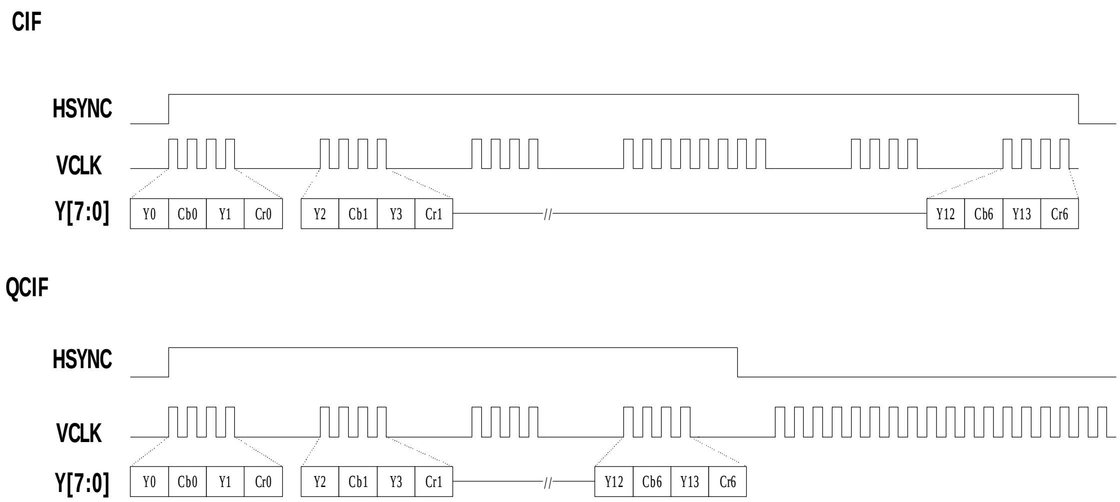
CIF or QCIF Mode

1. YCbCr 4:2:2 with 8bit Output

Register bit configurations

Sensor Control A : No Scale Mode and CIF Mode

Output Format : 8bit Output, Y First, U First



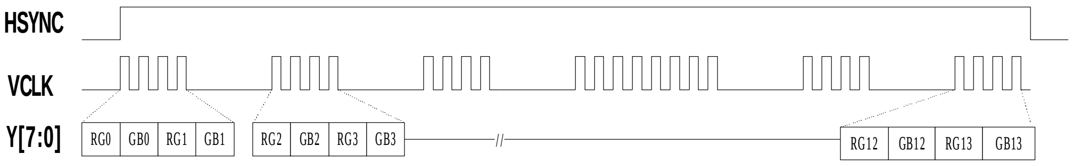
2. RGB565 with 8bit Output

Register bit configurations

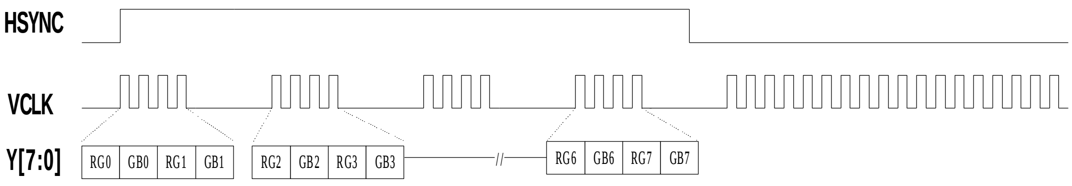
Sensor Control A : No Scale Mode or CIF Mode

Output Format : 8bit Output, Y First, U First and RGB565 enable.

CIF


HSYNC
VCLK
Y[7:0]
RG0
GB0
RG1
GB1
RG2
GB2
RG3
GB3
RG12
GB12
RG13
GB13

QCIF


HSYNC
VCLK
Y[7:0]
RG0
GB0
RG1
GB1
RG2
GB2
RG3
GB3
RG6
GB6
RG7
GB7

I2C Chip Interface

Register Write Sequences

One Byte Write

S	22H	A	01H	A	03H	A	P
*1	*2	*3	*4	*5	*6	*7	*8

Set "Sensor Control A" register into Window mode

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 03H [Video Mode : CIF

*7. Read: acknowledge from sensor

*8. Drive: I2C stop condition

Multiple Byte Write using Auto Address Increment

S	22H	A	6aH	A	51H	A	61H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

Set "AE Integration Step High/Low" register as 5161H with auto address increment

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 6aH [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 51H [AE Integration Step High]

*7. Read: acknowledge from sensor

*8. Drive: 61H [AE Integration Step Low]

*9. Read: acknowledge from sensor

*10. Drive: I2C stop condition

Register Read Sequence

S	22H	A	50H	A	S	23H	A	Data of 50H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11

Read "Reset Level Control" register from HV7131RP

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 50H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

*8. Read: acknowledge from sensor

*9. Read: Read “Reset Level Control Value” from sensor

*10. Drive: acknowledge to sensor. If there is more data bytes to read, SDA should be driven to low and data read states(*9, *10) is repeated. Otherwise SDA should be driven to high to prepare for the read transaction end.

*11. Drive: I2C stop condition

AC/DC Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Units	Min.	Max.
Vdpp	Digital supply voltage	Volts	-0.3	7.0
Vapp	Analog supply voltage	Volts	-0.3	7.0
Vipp	Input signal voltage	Volts	-0.3	7.0
Top	Operating Temperature	°C	-10	50
Tst	Storage Temperature	°C	-30	80

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

DC Operating Conditions

Symbol	Parameter	Units	Min.	Max.	Load[pF]	Notes
V_{dd}	Internal operation supply voltage	Volt	2.6	3.0		
V_{ih}	Input voltage logic "1"	Volt	2.0	3.0	6.5	
V_{il}	Input voltage logic "0"	Volt	0	0.8	6.5	
V_{oh}	Output voltage logic "1"	Volt	2.15		60	at Ioh = -1mA
V_{ol}	Output voltage logic "0"	Volt		0.4	60	
I_{oh}	Output High Current	mA		-4	60	
I_{ol}	Output Low Current	mA		4	60	
T_a	Ambient operating temperature	Celsius	-10	50		

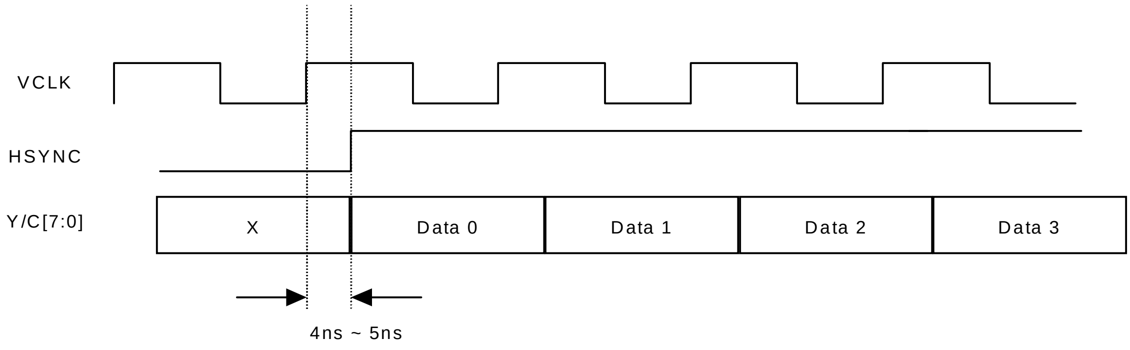
AC Operating Conditions

Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	25	MHz	1,2
SCK	I^2C clock frequency	400	KHz	3

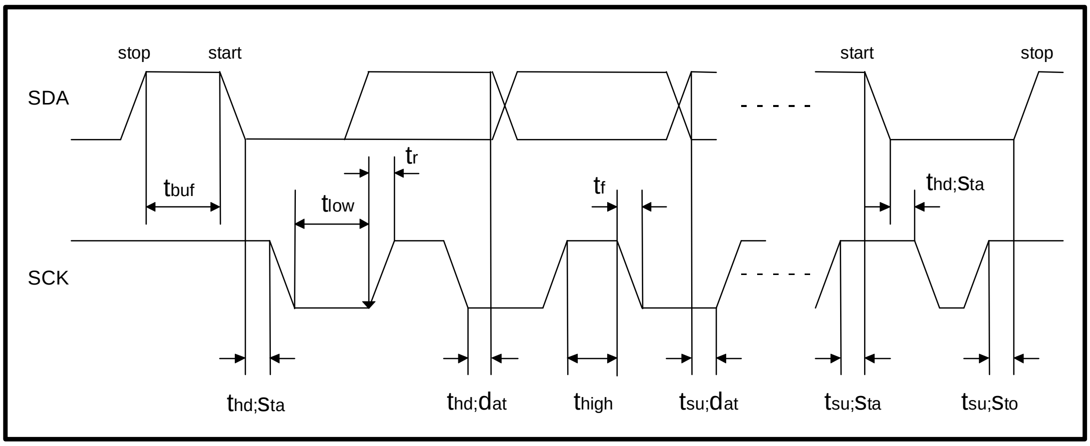
1. MCLK may be divided by internal clock division logic for easy integration with high speed video codec system.
2. Frame Rate : 30 frames/sec at 25Mhz, HBLANK = 208, VBLANK = 8
3. SCK is driven by host processor. For the detail serial bus timing, refer to I2C chip interface section

Output AC Characteristics

All output timing delays are measured with output load 60[pF]. Output delay includes the internal clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design. Due to the variable valid time delay of the output, video output signals Y[7:0], C[7:0], HSYNC, and VSYNC may be latched in the negative edge of VCLK for the stable data transfer between the image sensor and video codec.


VCLK
HSYNC
Y/C[7:0]
X
Data 0
Data 1
Data 2
Data 3
4ns ~ 5ns

I2C Bus Timing



Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I^2C bus must be free before a new transmission can start	t_{buf}	1.2	-	us
Hold time for a START	$t_{hd;Sta}$	1.0	-	us
LOW period of SCK	t_{low}	1.2	-	us
HIGH period of SCK	t_{high}	1.0	-	us
Setup time for START	$t_{su;Sta}$	1.2	-	us
Data hold time	$t_{hd;dat}$	100	-	ns
Data setup time	$t_{su;dat}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	250	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su;Sto}$	1.2	-	us
Capacitive load of SCK/SDA	C_b	-	-	pf

Electro-Optical Characteristics

Parameter	Units	Min.	Typical	Max.	Note
Sensitivity	mV / luxžsec		2200		Green Pixel
Dark Signal	mV		12		1/10” , 60℃
Output Saturation Signal	mV		780		

- Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

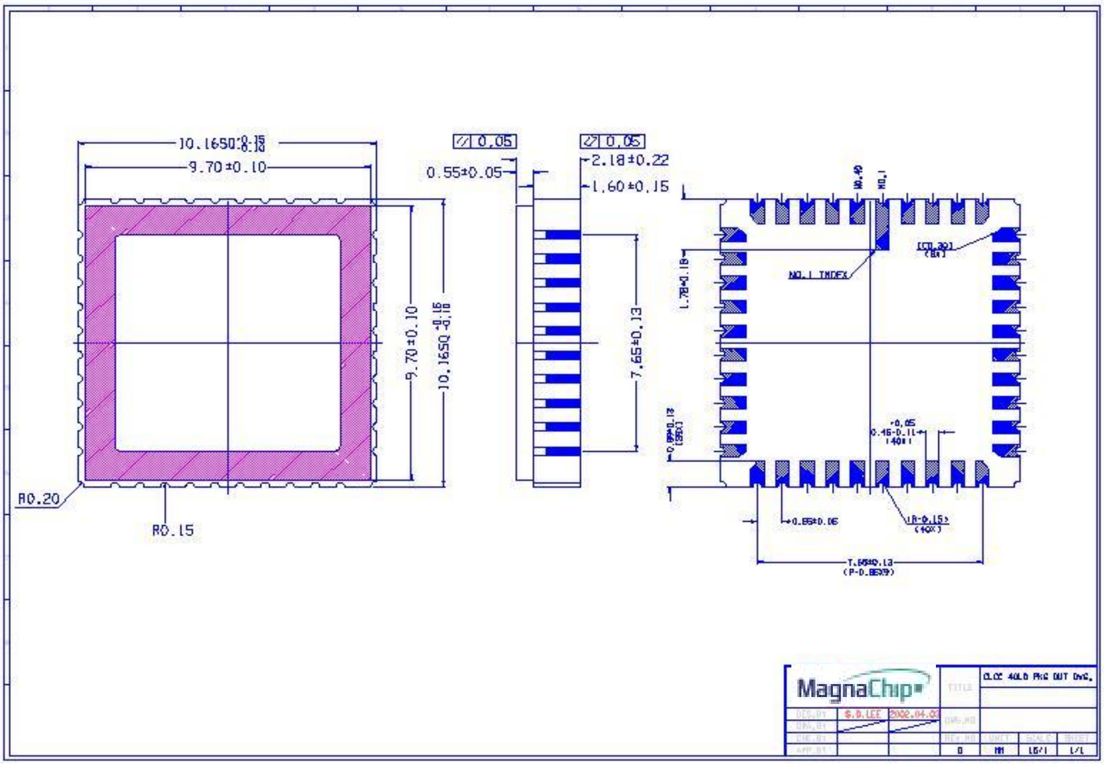
Soldering

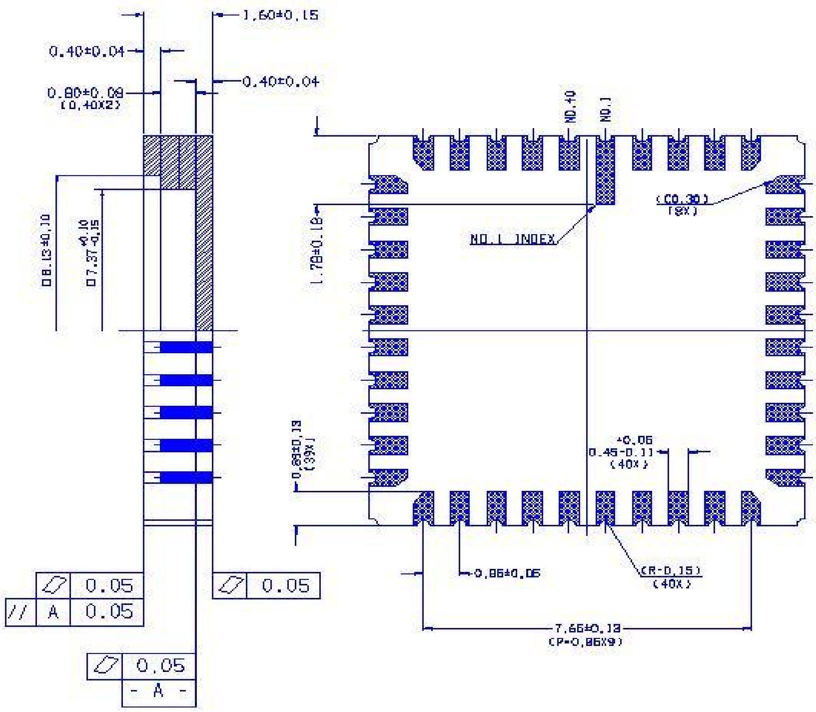
Infrared(IR) / Convection solder reflow condition

Parameter	Units	Min.	Typical	Max.	Note
Peak Temperature Range	Celsius	-	230	240	1)

Note: 1) Time within 5 Celsius of actual peak temperature, 10sec

CLCC Package Specification





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