

### Typical Applications

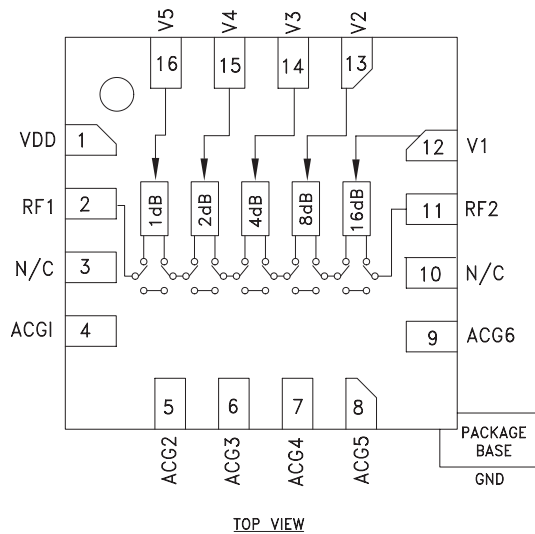
The HMC470LP3 /HMC470LP3E is ideal for both RF and IF applications:

- Cellular; UMTS/3G Infrastructure
- ISM, MMDS, WLAN, WiMAX
- Microwave Radio & VSAT
- Test Equipment and Sensors

### Features

- 1 dB LSB Steps to 31 dB
- Single Control Line Per Bit
- TTL/CMOS Compatible Control
- +/- 0.3 dB Typical Step Error
- Single +5V Supply
- 3 mm x 3 mm x 1 mm SMT Package

### Functional Diagram



### General Description

The HMC470LP3 & HMC470LP3E are broadband 5-bit GaAs IC digital attenuators in low cost lead-less surface mount packages. This single positive control line per bit digital attenuator incorporates off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 3.0 GHz, the insertion loss is less than 1.5 dB typical. The attenuator bit values are 1 (LSB), 2, 4, 8, and 16 dB for a total attenuation of 31 dB. Attenuation accuracy is excellent at  $\pm 0.3$  dB typical step error with an IIP3 of +45 dBm. Five TTL/CMOS control inputs are used to select each attenuation state. A single Vdd bias of +5V is required.

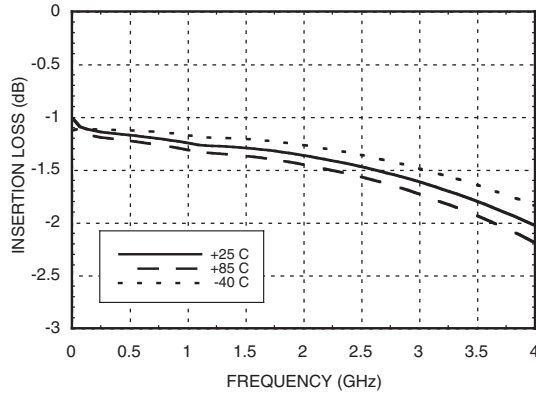
### Electrical Specifications,

$T_a = +25^\circ C$ , With Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

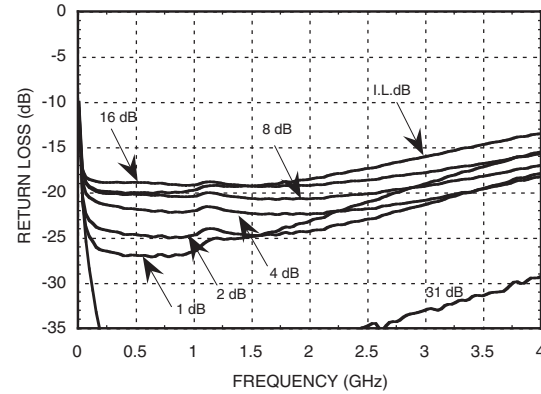
Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.5 GHz		1.3	1.6	dB
	1.5 - 2.3 GHz		1.4	1.7	dB
	2.3 - 3.0 GHz		1.7	2.0	dB
Attenuation Range	DC - 3.0 GHz		31		dB
Return Loss (RF1 & RF2, All Atten. States)	DC - 3.0 GHz		17		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	DC - 2.3 GHz	$\pm (0.3 + 2\% \text{ of Atten. Setting}) \text{ Max.}$			dB
	2.3 - 3.0 GHz	$\pm (0.3 + 3\% \text{ of Atten. Setting}) \text{ Max.}$			dB
	2.3 - 3.0 GHz	$\pm (0.3 + 6\% \text{ of Atten. Setting}) \text{ Max.}$			dB
Input Power for 0.1 dB Compression	0.1 - 3.0 GHz		20		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	0.1 - 3.0 GHz	REF - 15 dB States	45		dBm
		16 - 31 dB States	35		dBm
Switching Characteristics	DC - 3.0 GHz	tRISE, tFALL (10/90% RF)	160		ns
		tON, tOFF (50% CTL to 10/90% RF)	180		ns

**1 dB LSB GaAs MMIC 5-BIT DIGITAL  
POSITIVE CONTROL ATTENUATOR, DC - 3.0 GHz**

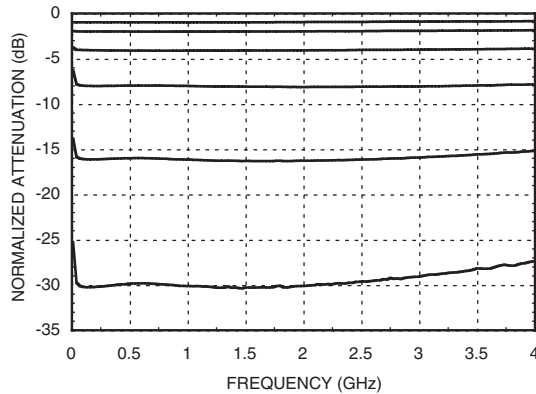
**Insertion Loss**



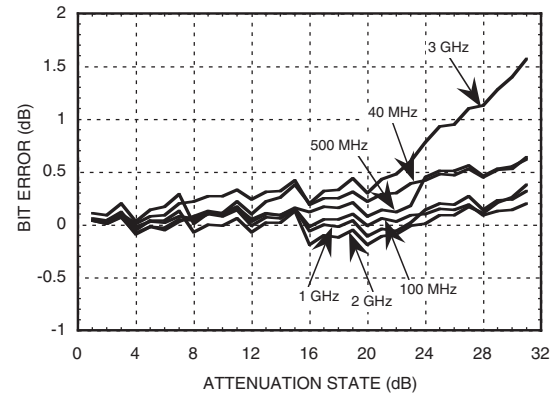
**Return Loss RF1, RF2**  
(Only Major States are Shown)



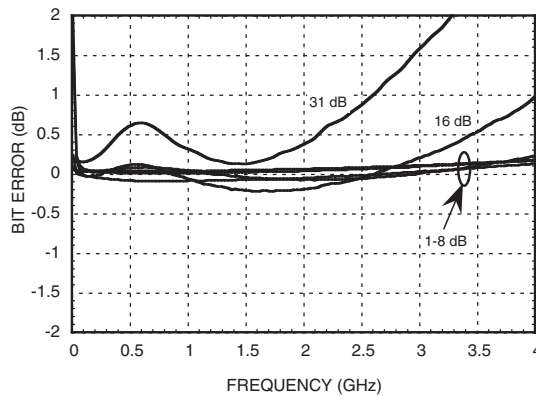
**Normalized Attenuation**  
(Only Major States are Shown)



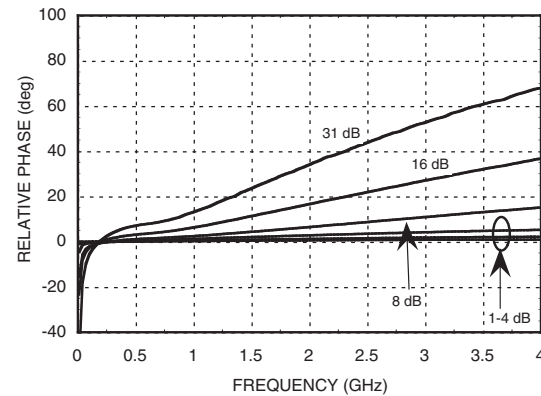
**Bit Error vs. Attenuation State**



**Bit Error vs. Frequency**  
(Only Major States are Shown)



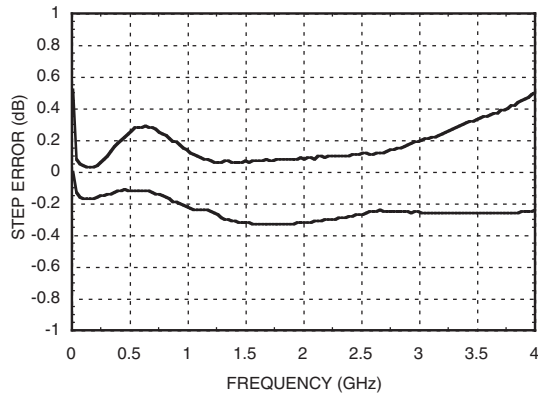
**Relative Phase vs. Frequency**  
(Only Major States are Shown)





**1 dB LSB GaAs MMIC 5-BIT DIGITAL  
POSITIVE CONTROL ATTENUATOR, DC - 3.0 GHz**

**Worst Case Step Error  
Between Successive Attenuation States**



**Bias Voltage & Current**

Vdd = +5.0 Vdc ± 10%	
Vdd (VDC)	Idd (Typ.) (mA)
+4.5	4.0
+5.0	4.2
+5.5	4.4

**Control Voltage**

State	Bias Condition
Low	0 to +0.8V @ -5 uA Typ.
High	+2.0 to + 5.0 Vdc @ 40 uA Typ.

Note: Vdd = +5V

**Truth Table**

Control Voltage Input					Attenuation State RF1 - RF2
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	
High	High	High	High	High	Reference I.L.
High	High	High	High	Low	1 dB
High	High	High	Low	High	2 dB
High	High	Low	High	High	4 dB
High	Low	High	High	High	8 dB
Low	High	High	High	High	16 dB
Low	Low	Low	Low	Low	31 dB

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.



**1 dB LSB GaAs MMIC 5-BIT DIGITAL  
POSITIVE CONTROL ATTENUATOR, DC - 3.0 GHz**

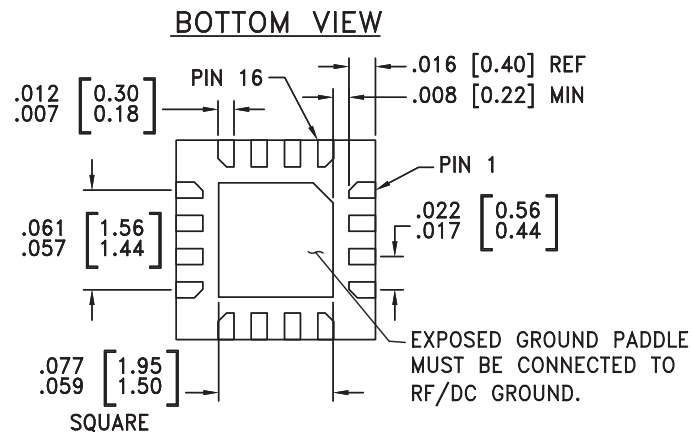
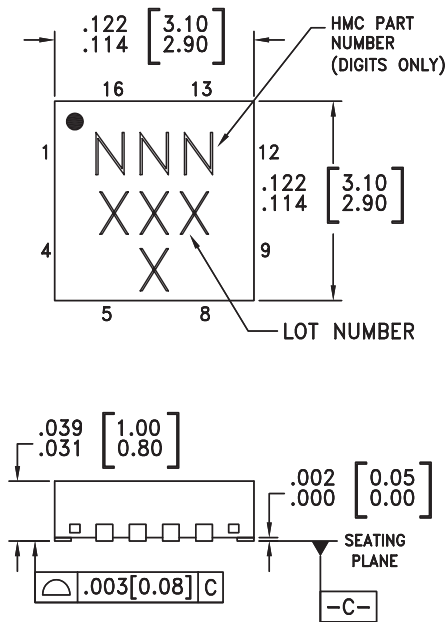
**Absolute Maximum Ratings**

RF Input Power (DC - 3.0 GHz)	+27 dBm (T = +85 °C)
Control Voltage Range (V1 to V5)	-1V to Vdd +1V
Bias Voltage (Vdd)	+7.0 Vdc
Channel Temperature	150 °C
Continuous P <sub>diss</sub> (T = 85 °C) (derate 7.7 mW/°C above 85 °C)	0.5 W
Thermal Resistance	130 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

**Outline Drawing**



**NOTES:**

- LEADFRAME MATERIAL: COPPER ALLOY
- DIMENSIONS ARE IN INCHES [MILLIMETERS]
- LEAD SPACING TOLERANCE IS NON-CUMULATIVE
- PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.  
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

**Package Information**

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking <sup>[3]</sup>
HMC470LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 <sup>[1]</sup>	470 XXXX
HMC470LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 <sup>[2]</sup>	470 XXXX

[1] Max peak reflow temperature of 235 °C

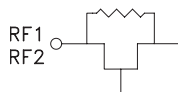
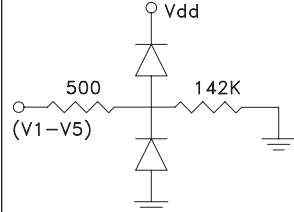

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

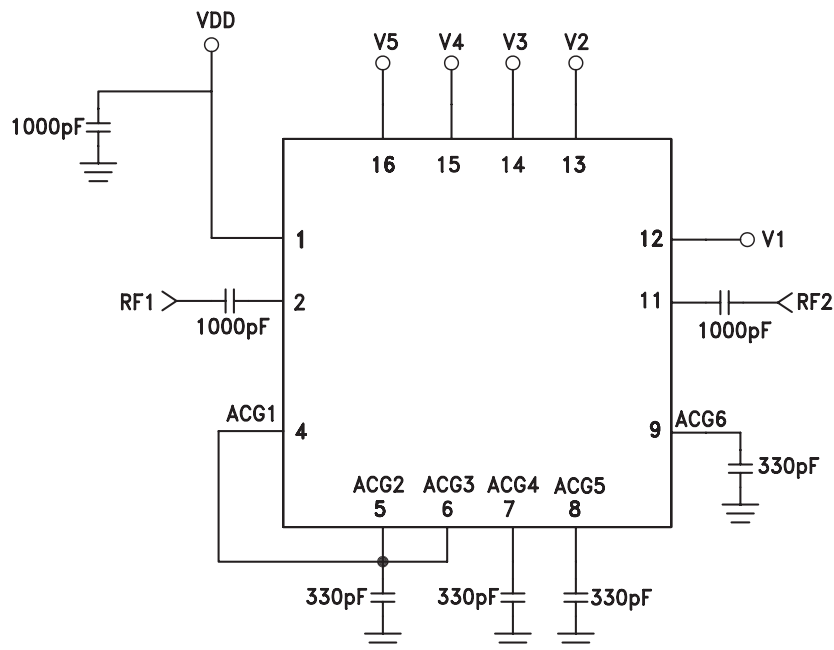


**1 dB LSB GaAs MMIC 5-BIT DIGITAL  
POSITIVE CONTROL ATTENUATOR, DC - 3.0 GHz**

**Pin Descriptions**

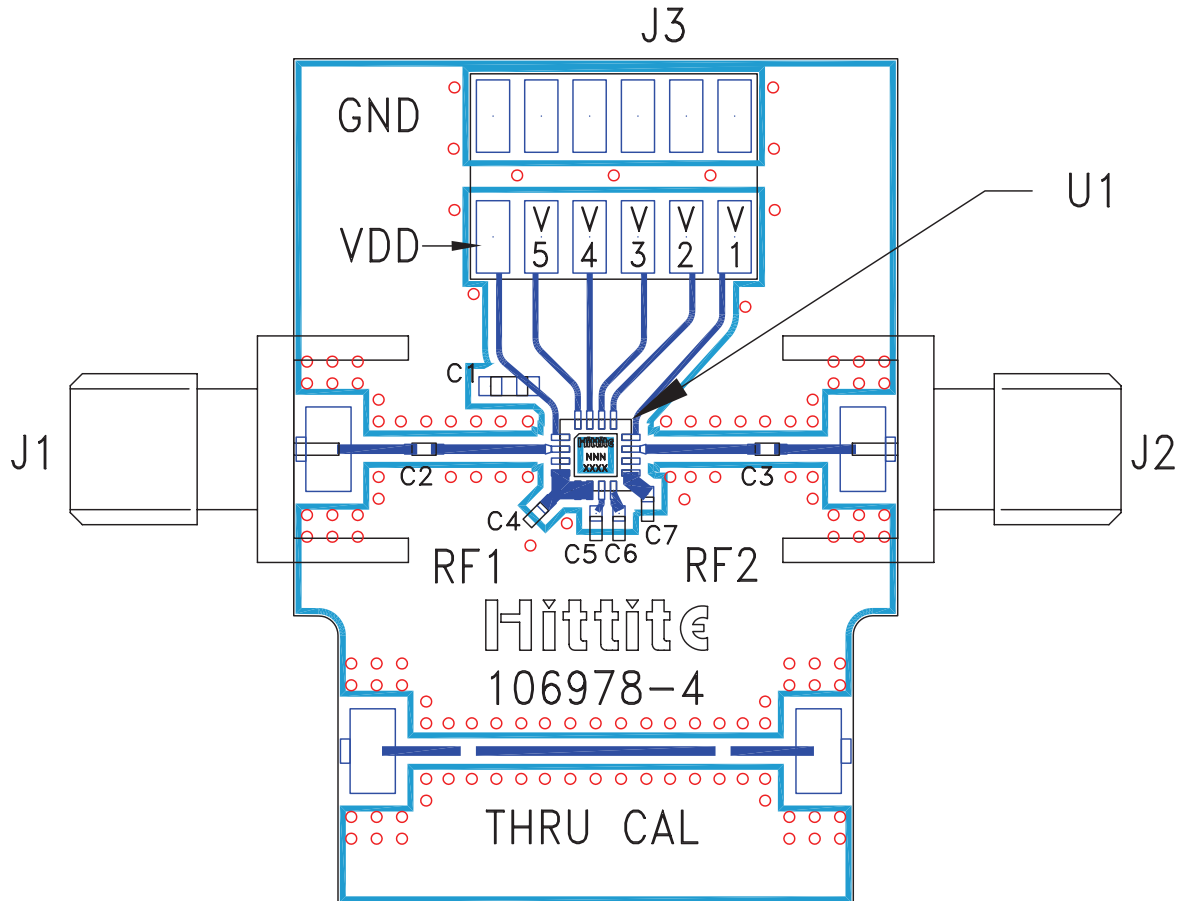
Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2, 11	RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. Select value based on lowest frequency of operation.	
3, 10	N/C	These pins should be connected to PCB RF ground to maximize performance.	
4 - 9	ACG1 - ACG6	External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
12 - 16	V1 - V5	See truth table and control voltage table.	
	GND	Package bottom has an exposed metal paddle that must also be connected to RF Ground.	

**Application Circuit**





**Evaluation PCB**



**List of Material for Evaluation PCB 107006 [1]**

Item	Description
J1 - J2	PC Mount SMA Connector
J3	12 Pin DC Connector
C1	1000 pF Capacitor, 0603 Pkg.
C2, C3	1000 pF Capacitor, 0402 Pkg.
C4 - C7	330 pF Capacitor, 0402 Pkg.
U1	HMC470LP3 / HMC470LP3E Digital Attenuator
PCB [2]	106978 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350Re

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.