HD153129

Color Palette with Triple 6-bit DA Converter

The HD153129P is a high-speed, high-density, low-power color palette with triple 6-bit DA converter.

Manufactured using a Hi-BiCMOS process, it realizes advanced DA conversion, high-speed SRAM and high-speed logic all on a single LSI chip with its color palette, advanced functions, small size and low cost, the HD153129P is an essential component for advanced graphics systems.

Features

- Displays 256 colors simultaneously from a total of 262,144 possible colors.
- Three 6-bit DA converters for RGB video output on a single chip
- Pixel mask function for display control
- Compatible with personal system/2
- Dot rate maximum of 50/65 MHz
- TTL compatible I/O levels
- 28-pin plastic DIP

Ordering Information

Type No.	Max. Operating Freq.	Package
HD153129P	50 MHz	600 mil 28 pin plastic DIP (DP-28)
HD153129P-65	65 MHz	

Note: Personal system/2 is a registered trademark of IBM.

Pin Arrangement

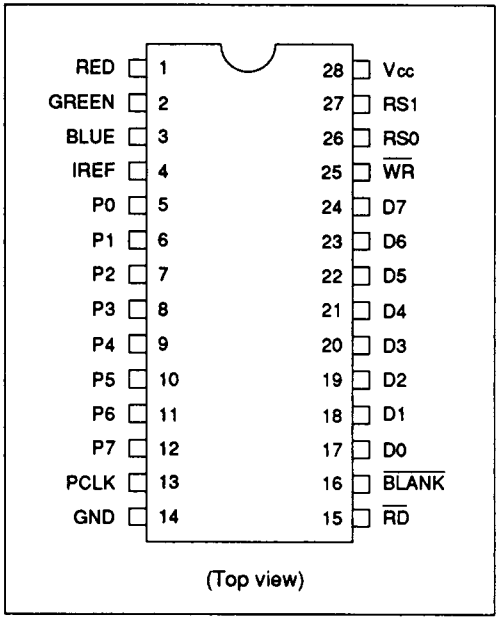


Figure 1 Pin Arrangement

Block Diagram

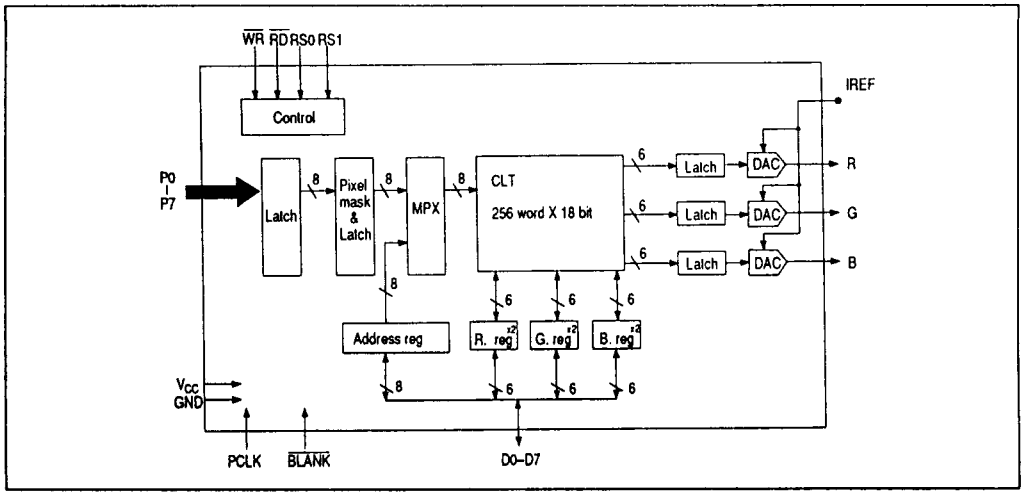


Figure 2 Block Diagram

Table 1 Pin Description

Pin name	Pin number	Description
P0 – P7	5, 6, 7, 8, 9, 10, 11, 12	CLT address inputs. P7 is MSB, P0 is LSB.
D0 – D7	17, 18, 19, 20, 21, 22, 23, 24	Data port for reading/writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB.
$\overline{RD}$	15	Read clock input. Strobes data from CLT or address, pixel mask, R, G or B registers during read operation.
$\overline{WR}$	25	Write clock input. Strobes data to CLT or address, pixel mask, R, G or B registers during write operation.
RS0, RS1	26, 27	Select inputs for CLT, address register or pixel mask register.
IREF	4	Terminal for connecting reference resistor to set DAC analog output level
RED, GREEN BLUE	1, 2, 3	DAC analog output signals
$\overline{BLANK}$	16	Video blank input for activating blank signal levels at DAC analog outputs.
PCLK	13	Reference clock input for digital and analog sections. On the rise of this signal, CLT and $\overline{BLANK}$ operations are processed and analog signal outputs become active.
V_{CC}	28	Power supply
GND	14	Ground

Functions

Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see table 2).

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

Address register: To perform read/write operations on the CLT, the CLT address must be set in the address register through D7 to D0 (D7 is the MSB and D0 is the LSB).
For a CLT write operation, write the CLT address via D7 to D0 with RS0 = "0" and RS1 = "0" (in order to select the address register, write mode).
To set up the address register for a CLT read operation, write the CLT address via D7 to D0 with RS0 = "1" and RS1 = "1" (in order to select the address register, read mode).
Also, the address register contents can be read as shown in figure 10 and figure 11.

Pixel mask register: The pixel mask register allows displayed colors to be modified by altering the value input from video memory and the contents of the CLT. The pixel mask register is set by writing a pixel mask value to D7 (MSB) to D0 (LSB) with RS0 "0" and RS1 = "1" (in order to select the pixel mask register for a data write) as shown in figure 13. During color palette operations, the value input from video memory at P7 (MSB) to P0 (LSB) is ANDed with the pixel mask register value, and the resulting value is applied as an address to the CLT. Consequently, pixel mask "0" bits will cancel corresponding video memory value "1" bits. The following table shows the CLT address that results for a particular pixel mask register value and video memory value.

Table 3 Pixel Mask Example

Pixel mask register	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**
Address input (P7 – P0)	Pd_7	Pd_6	Pd_5	Pd_4	Pd_3	Pd_2	Pd_1	Pd_0
CTL address value	Pd_7	0	Pd_5	0	Pd_3	Pd_2	0	Pd_0

RGB registers: There are two RGB register types: one for writing color information to the CLT and one for reading color information from the CLT. Each register type is organized as an 18-bit word.
To read or write data to the CLT, set RS0 = '0' to select the appropriate RGB register wrile performing the read or write via data port D5 (MSB) to D0 (LSB). Bits D6 and D7 may be either '0' or '1' at this time. Write or read the data in the order of R, G, B as shown in figure 7 and figure 8.

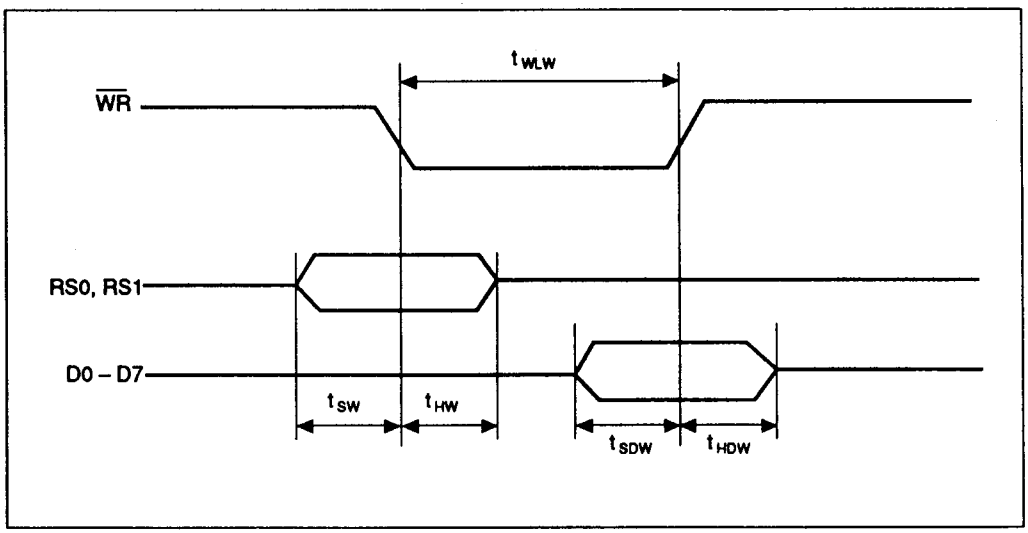


Figure 3 Write Timing

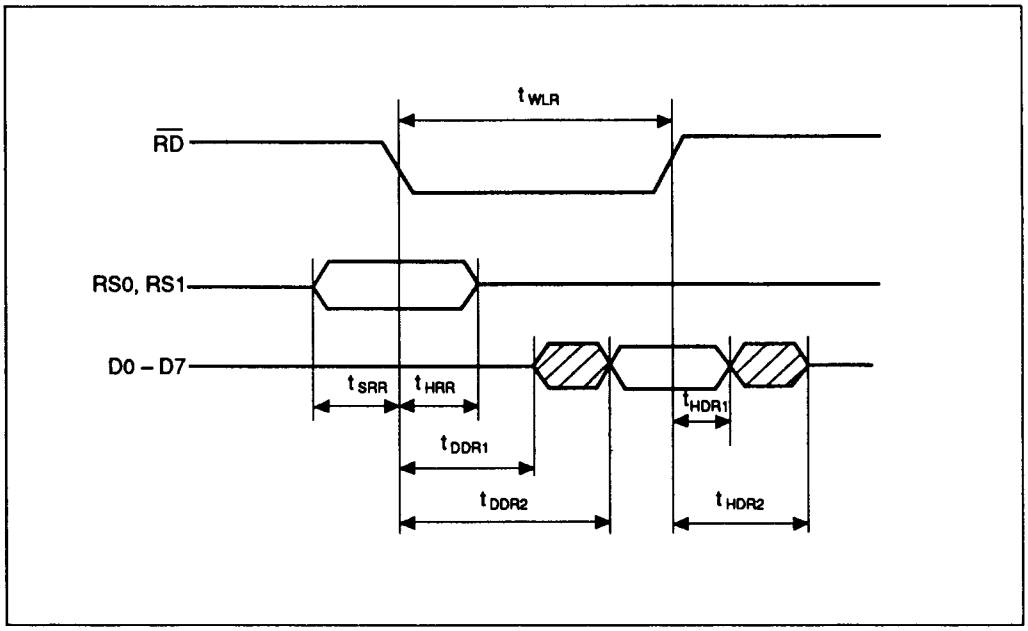


Figure 4 Read Timing

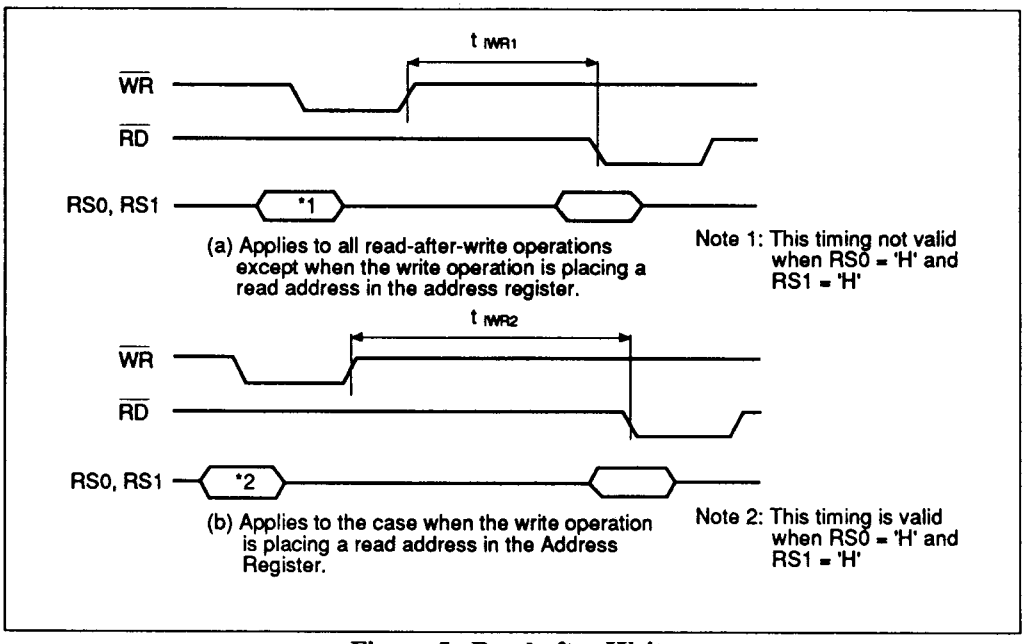


Figure 5 Read after Write

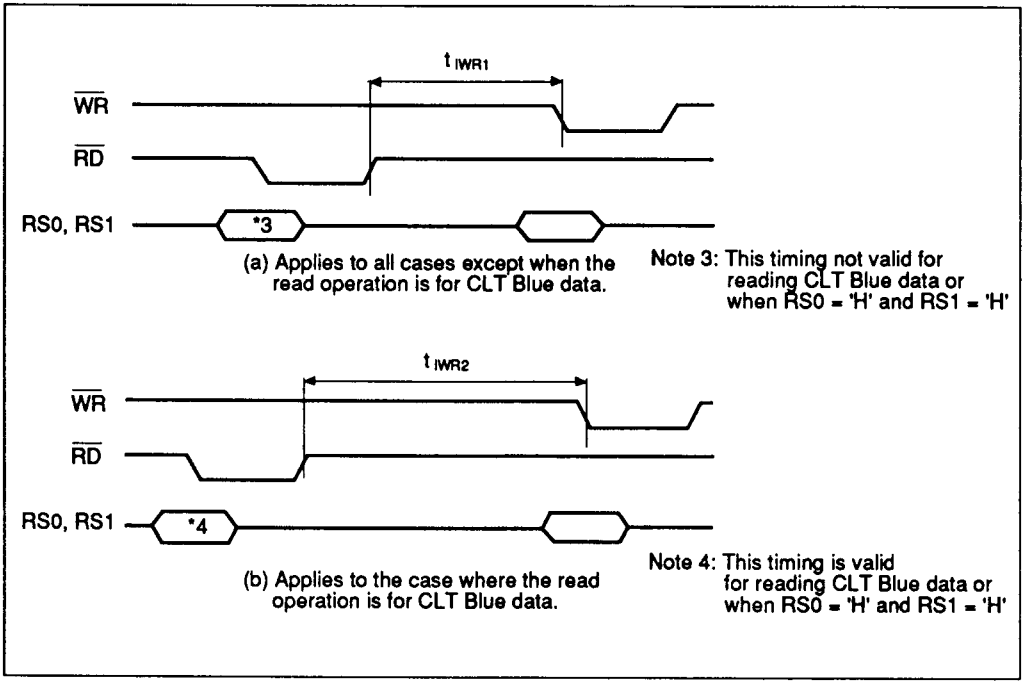
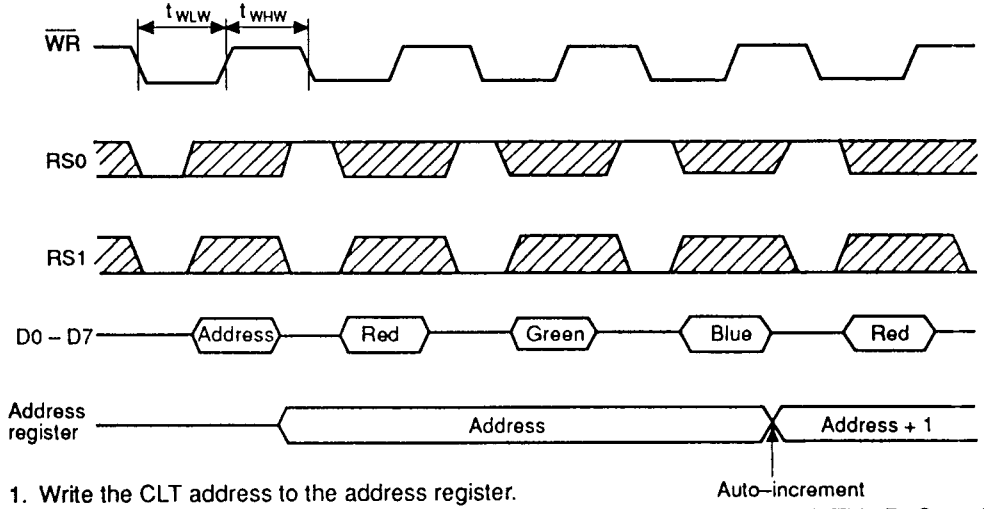
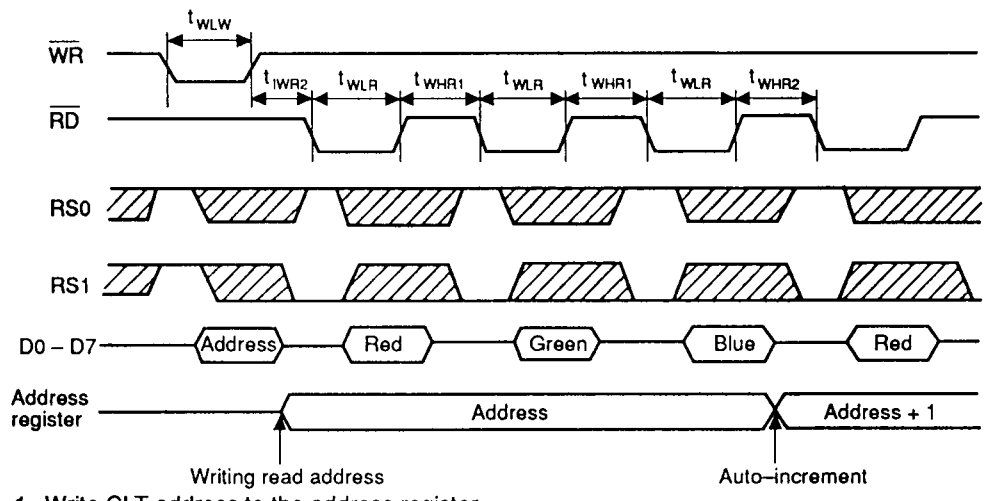


Figure 6 Write after Read



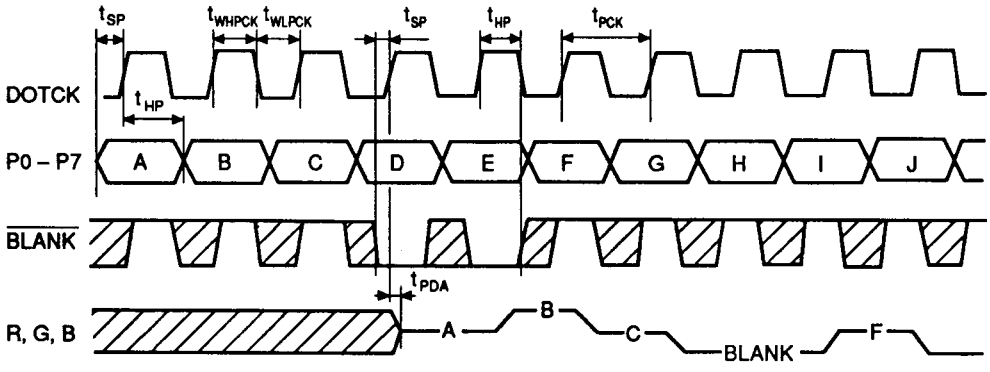
1. Write the CLT address to the address register.
2. Write the data (NRZ format) in the order red, green, then blue to D0 to D5. This R, G, and B data forms an 18-bit word that is written to the CLT.
3. When the R, G and B data writes are completed, the address is automatically incremented by 1 and the next data set can be applied again in RGB order. All subsequent CLT data writes should continue in this manner.

Figure 7 CLT Write



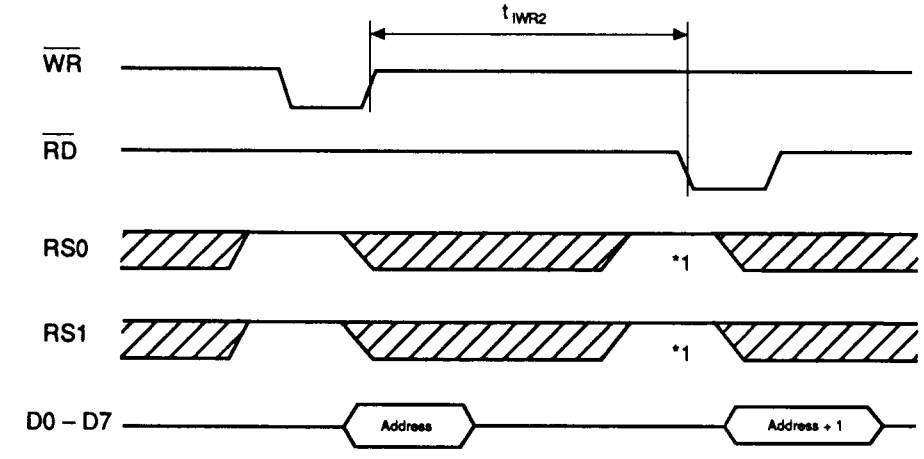
1. Write CLT address to the address register.
2. With each strobe of the RD line, CLT data can be read in the order red, green and blue at D0 to D5.
3. When the blue data read is completed, the address is automatically incremented and the CLT data for that address can then be read in the order of R, G and B.

Figure 8 CLT Read



Video output is generated when a CLT data location is selected by the address input at P7 to P0 and subsequently output as analog RGB signals. The video output lags behind the PCLK strobe of its corresponding address at P7 to P0 by three PCLK clock periods.

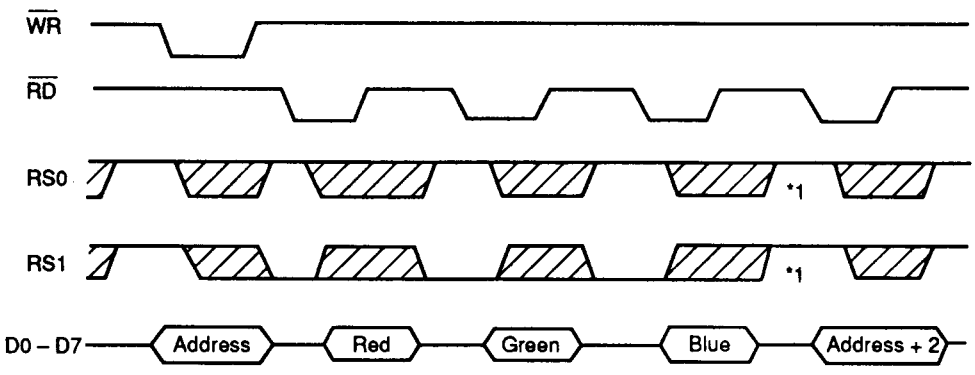
Figure 9 Video Output



1. Use $\overline{WR}$ to select the address register and to write the CLT read address.
2. Use $\overline{RD}$ to read the contents of the address register. At this time, the contents of the address register is incremented by 1.

Note *1: The address register can also be read when RS0 and RS1 are both set to 'L'.

Figure 10 Address Register Read (1)



1. Use $\overline{WR}$ to select the address register and to write the CLT address.
2. Use $\overline{RD}$ three times in succession to read CLT data in the order red, green and blue.
3. Using $\overline{RD}$ again will read the contents of the address register. This read of the address register plus the previous read of red, blue and green data will increment the contents of the address register by 2.

Note *1: The address register can also be read when RS0 and RS1 are both set to 'L'.

Figure 11 Address Register Read (2)

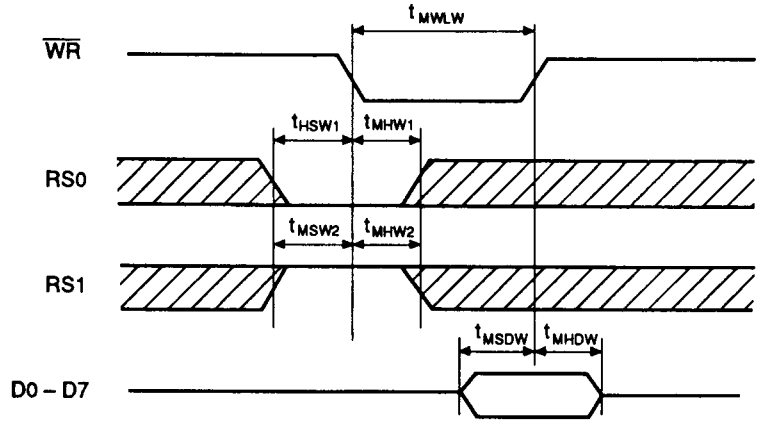


Figure 12 Pixel Mask Register Write

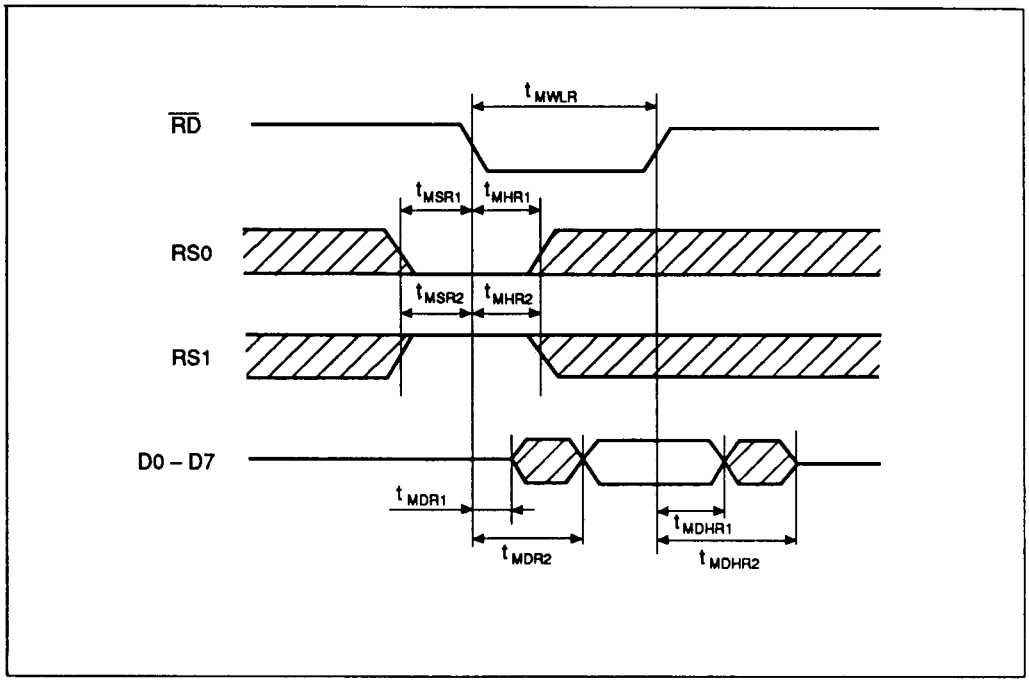


Figure 13 Pixel Mask Register Read

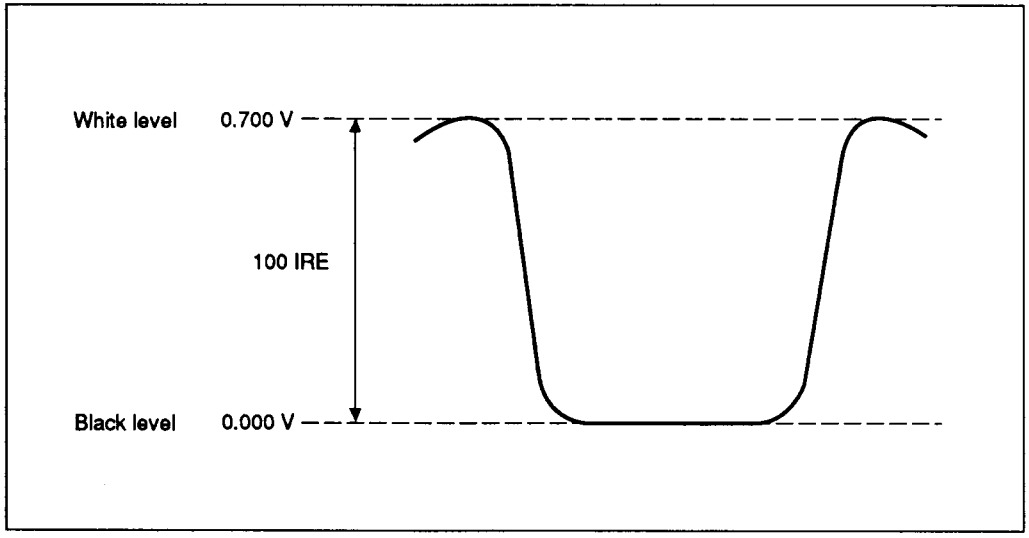


Figure 14 Video Output Waveform

Registers Correspondence with the CLT

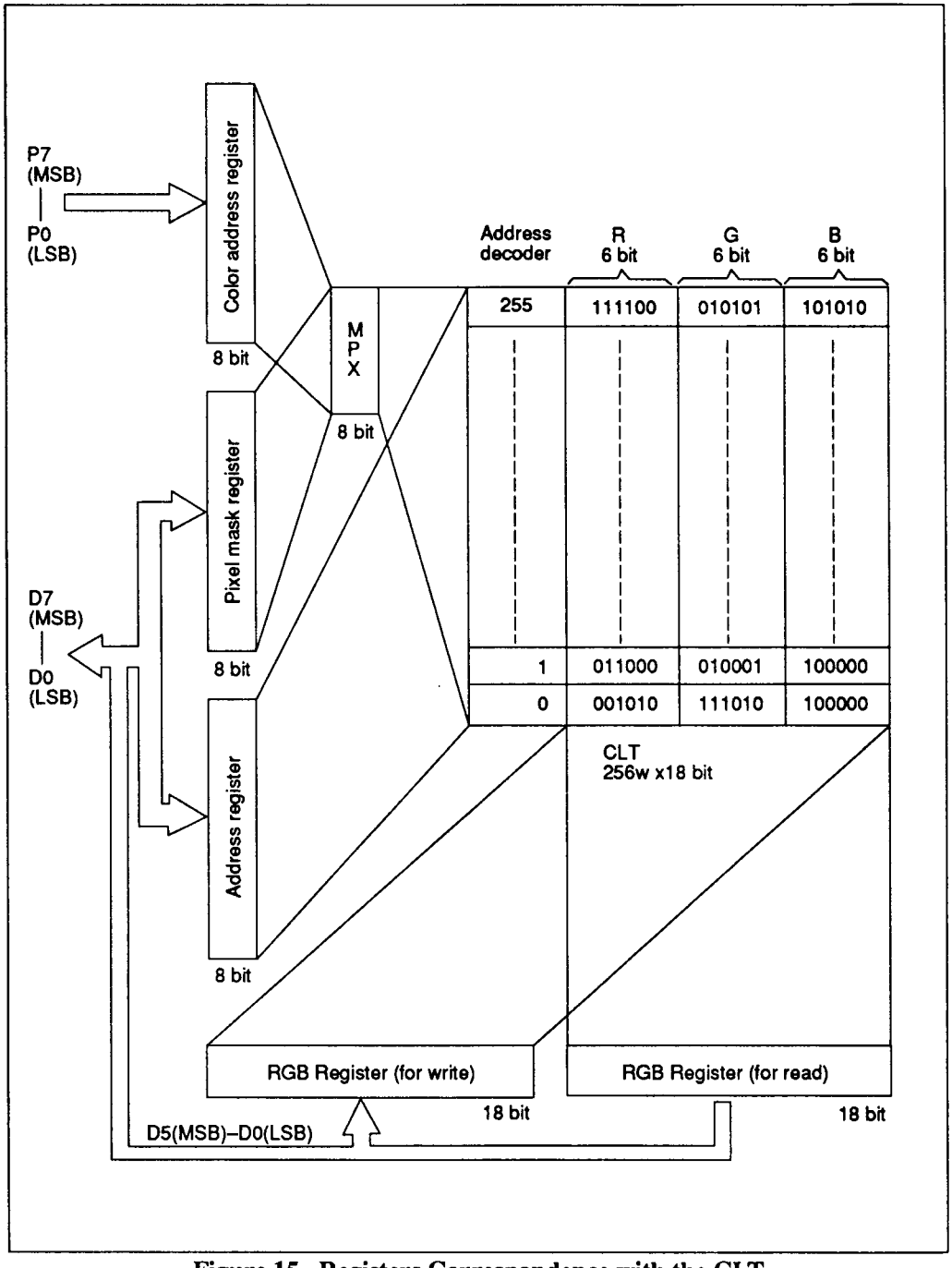


Figure 15 Registers Correspondence with the CLT

System Configuration Example

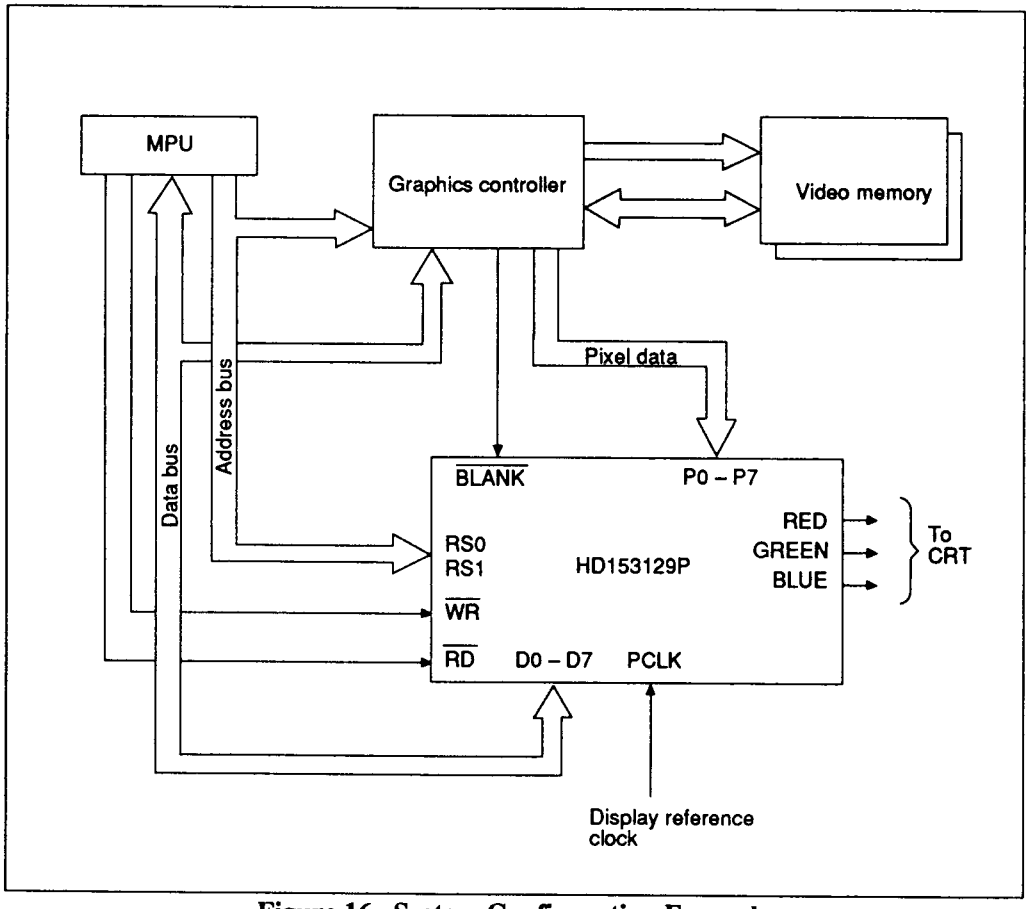


Figure 16 System Configuration Example

Table 4 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	0 to V_{CC}	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Electrical Characteristics

Table 5 DAC Section Electrical Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		6	6	6	bits	
Maximum operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage	V_A (Full)	–5	—	5	% of FSR	
I_{REF} = –4.44 mA	V_A (Zero)	–2	—	2	% of FSR	
Differential linearity	DLE	–1	—	+1	LSB	
Integral linearity	ILE	–1	—	+1	LSB	
Output rise time (20 – 80 %)	tr	—	—	10	ns	C_L = 15 pF
Output fall time (80 – 20 %)	tf	—	—	10	ns	C_L = 15 pF
Settling time	ts	—	—	30	ns	C_L = 15 pF
Glitch energy	E_G	—	90	—	PVS	

Table 6 Digital Section DC Characteristics (unless otherwise specified V_{CC} = 5 V ± 5 %, Ta = 0 to +70 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input "High" level voltage	V_{IH}	2.2	—	V_{CC}	V	
Input "Low" level voltage	V_{IL}	–0.3	—	0.8	V	
Input clamp voltage	V_I	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA
Output "High" level voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, I_{OH} = –400 µA
Output "Low" level voltage	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA
Input current	I_I	—	—	1	mA	V_{CC} = 5.25 V, V_I = 5.5 V
"High" level input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
"Low" level input current	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V, V_I = 0.4 V
Supply current	I_{CC}	—	110	170	mA	V_{CC} = 5.25 V, I_{REF} = –4.44 mA

Table 7 Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
PCLK cycle time	t_{PCK}	20	—	15.3	—	ns		9
PCLK low level time	t_{WLPCK}	8	—	6	—	ns		9
PCLK high level time	t_{WHPCK}	8	—	6	—	ns		9
Data setup time	t_{SP}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	C_L = 15 pF	9
$\overline{WR}$ low level time	t_{WLW}	50	—	50	—	ns		3, 7, 8
$\overline{WR}$ high level time	t_{WHW}	3 x t_{DCK}	—	3 x t_{DCK}	—	ns		7
$\overline{RD}$ low level time	t_{WLR}	50	—	50	—	ns		4, 8
$\overline{RD}$ high level time	t_{WHR1}	3 x t_{DCK}	—	3 x t_{DCK}	—	ns		8
	t_{WHR2}	6 x t_{DCK}	—	6 x t_{DCK}	—	ns		8
$\overline{WR}$/$\overline{RD}$ interval time	t_{IWR1}	3 x t_{DCK}	—	3 x t_{DCK}	—	ns		5, 6
	t_{IWR2}	6 x t_{DCK}	—	6 x t_{DCK}	—	ns		5, 6, 8, 9
$\overline{WR}$/RS0, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}$/RS0, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}$/RS0, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}$/RS0, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
$\overline{WR}$ data setup time	t_{SDW}	10	—	10	—	ns		3
$\overline{WR}$ data hold time	t_{HDW}	10	—	10	—	ns		3
$\overline{RD}$ data output delay time	t_{DDR1}	5	—	5	—	ns	C_L = 15 pF	4
	t_{DDR2}	—	40	—	40	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time	t_{HDR1}	5	—	5	—	ns	C_L = 15 pF	4
	t_{HDR2}	—	20	—	20	ns	C_L = 15 pF	4
$\overline{WR}$ low level time	t_{MWLW}	50	—	50	—	ns		12
$\overline{RD}$ low level time	t_{MWLR}	50	—	50	—	ns		13
$\overline{WR}$/RS0, RS1 setup time	t_{MSW1}	10	—	10	—	ns		12
	t_{MSW2}	10	—	10	—	ns		12

Unit mm (inch)

Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{WR}$/RS0, RS1 hold time	t_{MHW1}	10	—	10	—	ns		12
	t_{MHW2}	10	—	10	—	ns		12
$\overline{RD}$/RS0, RS1 setup time	t_{MSR1}	10	—	10	—	ns		13
	t_{MSR2}	10	—	10	—	ns		13
$\overline{RD}$/RS0, RS1 hold time	t_{MHR1}	10	—	10	—	ns		13
	t_{MHR2}	10	—	10	—	ns		13
$\overline{WR}$ data setup time	t_{MSDW}	10	—	10	—	ns		12
$\overline{WR}$ data hold time	t_{MHDW}	10	—	10	—	ns		12
$\overline{RD}$ data output delay time	t_{MDR1}	5	—	5	—	ns	C_L = 15 pF	13
	t_{MDR2}	—	40	—	40	ns	C_L = 15 pF	13
$\overline{RD}$ data output hold time	t_{MDHR1}	5	—	5	—	ns	C_L = 15 pF	13
	t_{MDHR2}	—	20	—	20	ns	C_L = 15 pF	13

Connection Example

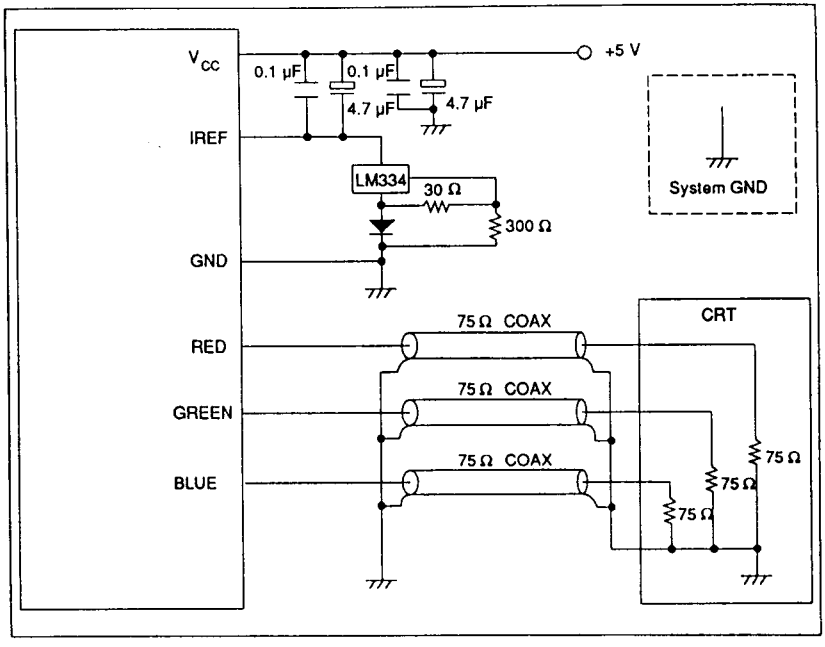


Figure 17 Connection Example