PRELIMINARY

CYP15G0101DXA

Single Channel HOTLink II™ Transceiver

Features

- 2nd generation HOTLink® technology
- Fibre Channel and Gigabit Ethernet compliant 8B/10B-coded or 10-bit unencoded
- ESCON, DVB-ASI Compliant
- SMPTE-292M, SMPTE-259M Compliant
- 8-bit encoded data transport
  - Aggregate throughput of 2.4 GBits/second
- 10-bit unencoded data transport
  - Aggregate throughput of 3 GBits/second
- Selectable parity check/generate
- Selectable input clocking options
- Selectable output clocking options
- MultiFrame™ receive Framer provides alignment to
  - Bit and byte boundaries
  - Comma or Full K28.5 detect
  - Single or Multi-byte Framer for byte alignment
  - Low-latency option
- Synchronous LVTTL parallel input interface
- Synchronous LVTTL parallel output interface
- 200-to-1500 MBaud serial signaling rate
- Internal PLLs with *no* external PLL components
- Dual differential LVPECL-compatible serial inputs
  - Internal DC-restoration
- Dual differential LVPECL-compatible serial outputs
  - Source matched for 50Ω transmission lines
  - No external bias resistors required
  - Signaling-rate controlled edge-rates
- Compatible with
  - Fiber-optic modules
  - Copper cables
  - Circuit board traces
- JTAG boundary scan
- Built-In Self-Test (BIST) for at-speed link testing
- Link Quality Indicator
  - Analog signal detect
  - Digital signal detect
  - Frequency range detect
- Low Power (0.85W typical)
  - Single +3.3V V_{CC} supply
- 100-ball BGA
- 0.25µ BiCMOS technology

Functional Description

The CYP15G0101DXA Single Channel HOTLink II™ Transceiver is a point-to-point communications building block allowing the transfer of data over a high-speed serial link (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 200-to-1500 MBaud.

The transmit channel accepts parallel characters in an Input Register, encodes each character for transport, and converts it to serial data. The receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to an Output Register. *Figure 1* illustrates typical connections between independent host systems and corresponding CYP15G0101DXA parts. As a second-generation HOTLink device, the CYP15G0101DXA extends the HOTLink II family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices.

The transmit (TX) section of the CYP15G0101DXA Single Channel HOTLink II consists of a byte-wide channel. The channel can accept either 8-bit data characters or pre-encod-

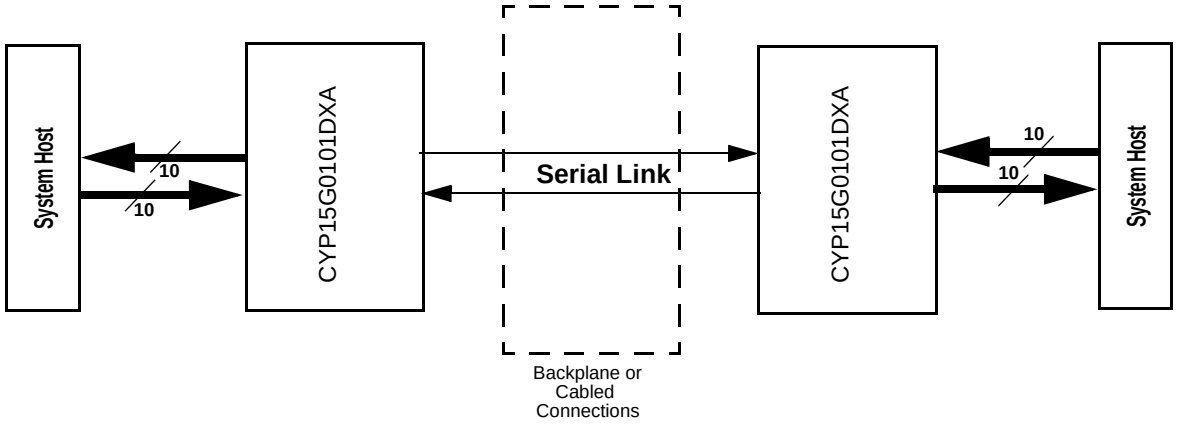


Figure 1. HOTLink II™ System Connections

ed 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10- or 20-times the input reference clock.

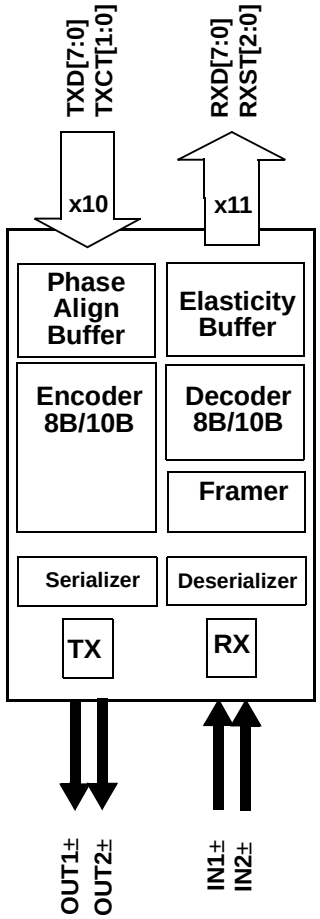
The receive (RX) section of the CYP15G0101DXA Single Channel HOTLink II consists of a byte-wide channel. The channel accepts a serial bit-stream from one of two PECL-compatible differential Line Receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The recovered bit-stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B Encoder/Decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path interfaces from one or multiple sources, the receive interface may be configured to present data relative to a recovered clock (output) or to a local reference clock (input).

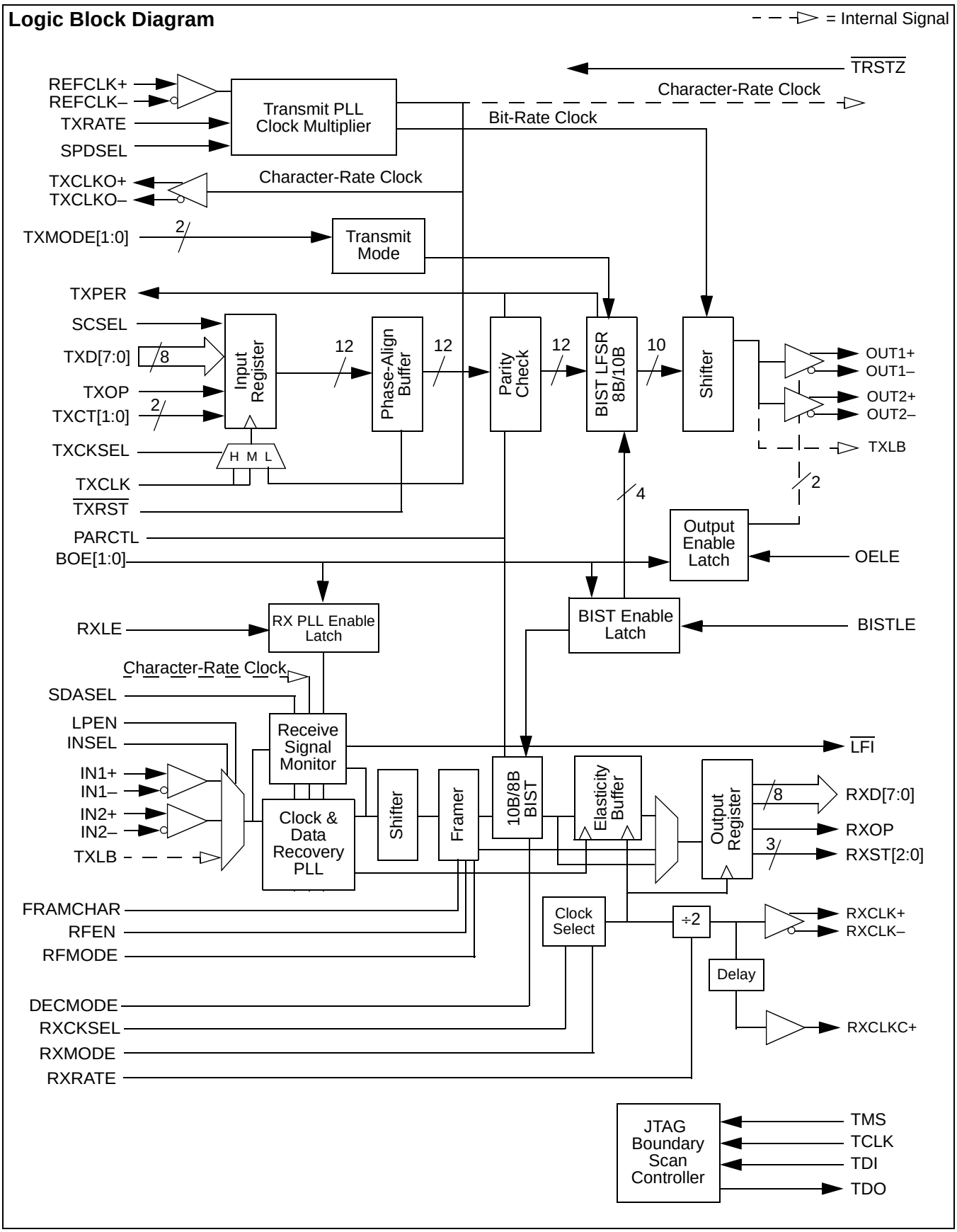
Both the transmit and the receive channels contain independent Built-In Self-Test (BIST) pattern generators and checkers. This BIST hardware allows at-speed testing of the high-speed serial data paths in both transmit and receive sections, as well as across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on basestations, switches, routers, servers and video transmission equipment.

CYP15G0101DXA Transceiver Logic Block Diagram



Logic Block Diagram



Pin Configuration

Top View

	1	2	3	4	5	6	7	8	9	10
A	V_{CC}	IN2+	V_{CC}	OUT2–	RX MODE	TX MODE [1]	IN1+	V_{CC}	OUT1–	V_{CC}
B	V_{CC}	IN2–	TDO	OUT2+	TX RATE	TX MODE [0]	IN1–	N/C	OUT1+	V_{CC}
C	RFEN	LPEN	RXLE	RX CLKC+	RX RATE	SDA SEL	SPD SEL	PAR CTL	RF MODE	INSEL
D	BOE[0]	BOE[1]	FRAM CHAR	GND	GND	GND	GND	TMS	$\overline{TRSTZ}$	TDI
E	BISTLE	DEC MODE	OELE	GND	GND	GND	GND	TCLK	RX CKSEL	TX CKSEL
F	RX ST[2]	RX ST[1]	RX ST[0]	GND	GND	GND	GND	TX PER	REF CLK–	REF CLK+
G	RXOP	RX D[1]	RX D[5]	GND	GND	GND	GND	TXOP	TX CLKO+	TX CLKO–
H	RX D[0]	RX D[2]	RX D[6]	$\overline{LFI}$	TX CT[1]	TX D[6]	TX D[3]	TX CLK	$\overline{TXRST}$	#NC
J	V_{CC}	RX D[3]	RX D[7]	RX CLK–	TX CT[0]	TX D[5]	TX D[2]	TX D[0]	#NC	V_{CC}
K	V_{CC}	RX D[4]	V_{CC}	RX CLK+	TX D[7]	TX D[4]	TX D[1]	V_{CC}	SCSEL	V_{CC}

Bottom View

10	9	8	7	6	5	4	3	2	1	
V_{CC}	OUT1–	V_{CC}	IN1+	TX MODE [1]	RX MODE	OUT2–	V_{CC}	IN2+	V_{CC}	A
V_{CC}	OUT1+	#NC	IN1–	TX MODE [0]	TX RATE	OUT2+	TDO	IN2–	V_{CC}	B
INSEL	RF MODE	PAR CTL	SPD SEL	SDA SEL	RX RATE	RX CLKC+	RXLE	LPEN	RFEN	C
TDI	$\overline{TRSTZ}$	TMS	GND	GND	GND	GND	FRAM CHAR	BOE[1]	BOE[0]	D
TX CKSEL	RX CKSEL	TCLK	GND	GND	GND	GND	OELE	DEC MODE	BISTLE	E
REF CLK+	REF CLK–	TX PER	GND	GND	GND	GND	RX ST[0]	RX ST[1]	RX ST[2]	F
TX CLKO–	TX CLKO+	TXOP	GND	GND	GND	GND	RX D[5]	RX D[1]	RXOP	G
#NC	$\overline{TXRST}$	TX CLK	TX D[3]	TX D[6]	TX CT[1]	$\overline{LFI}$	RX D[6]	RX D[2]	RX D[0]	H
V_{CC}	#NC	TX D[0]	TX D[2]	TX D[5]	TX CT[0]	RX CLK–	RX D[7]	RX D[3]	V_{CC}	J
V_{CC}	SCSEL	V_{CC}	TX D[1]	TX D[4]	TX D[7]	RX CLK+	V_{CC}	RX D[4]	V_{CC}	K

NOTE: #NC = **DO NOT CONNECT**

Pin Descriptions

CYP15G0101DXA Single Channel HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPER	LVTTL Output, changes relative to REFCLK↑ [1]	**Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected at the Encoder. This output is HIGH for one transmit character-clock period to indicate detection of a parity error in the character presented to the Encoder. If a parity error is detected, the character in error is replaced with a C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place regardless of the encoded/non-encoded state of the interface. This output provides an indication of a Phase-Align Buffer underflow/overflow condition. When the Phase-Align Buffer is enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), and an underflow/overflow condition is detected, TXPER is asserted and remains asserted until either an atomic Word Sync Sequence is transmitted or $\overline{\text{TXRST}}$ is sampled LOW to re-center the Phase-Align Buffer. When BIST is enabled (BISTLE = HIGH) for the transmit channel, BIST progress is presented on this output. Once every 511 character times (plus a 16-character Word Sync Sequence when the receive interface is clocked by REFCLK), the TXPER signal will pulse HIGH for one transmit-character clock period to indicate a complete pass through the BIST sequence.
TXCT[1:0]	LVTTL Input, synchronous, sampled by TXCLK↑ or REFCLK↑ [1]	**Transmit Control**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and are passed to the Encoder or Transmit Shifter. They identify how the TXD[7:0] characters are interpreted. When the Encoder is bypassed, these inputs are interpreted as data bits. When the Encoder is enabled, these inputs determine if the TXD[7:0] character is encoded as Data, a Special Character code, or replaced with other Special Character codes. See *Table 1* for details.
TXD[7:0]	LVTTL Input, synchronous, sampled by TXCLK↑ or REFCLK↑ [1]	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and passed to the Encoder or Transmit Shifter. When the Encoder is enabled (TXMODE[1:0] ≠ LL), TXD[7:0] specify the specific data or command character to be sent.
TXOP	LVTTL Input, synchronous, internal pull-up, sampled by TXCLK↑ or REFCLK↑ [1]	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the parity captured at this input is XORed with the data on the TXD bus to verify the integrity of the captured character.
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous, internal pull-up, sampled by TXCLK↑ or REFCLK↑ [1]	**Transmit Clock Phase Reset**. Active LOW. When sampled LOW, the transmit Phase-Align Buffer is allowed to adjust its data-transfer timing (relative to TXCLK↑) to allow clean transfer of data from the Input Register to the Encoder or Transmit Shift Register. When $\overline{\text{TXRST}}$ is deasserted (HIGH), the internal phase relationship between TXCLK↑ and the internal character-rate clock is fixed and the device operates normally. When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear Phase-Align Buffer faults caused by highly asymmetric REFCLK periods or REFCLK inputs with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from the transmit path as the Phase-Align Buffer is cleared or reset. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges of TXCLK (or one REFCLK↑) to ensure the reset operation is initiated correctly on the channel. This input is not interpreted when both TXCKSEL and TXRATE are LOW.

Note:

1. When REFCLK is configured for half-rate operation (TXRATE = HIGH), this input is sampled (or the outputs change) relative to both the rising and falling edges of REFCLK.

Pin Descriptions (continued)

CYP15G0101DXA Single Channel HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
SCSEL	LVTTL Input, synchronous, internal pull-down, sampled by TXCLK↑ or REFCLK↑ [1]	**Special Character Select**. Used in some transmit modes along with TXCT[1:0] to encode special characters or to initiate a Word Sync Sequence.
Transmit Path Clock and Clock Control		
TXCKSEL	3-Level Select [2] static control input	**Transmit Clock Select**. Selects the clock source, used to write data into the Transmit Input Register, of the transmit channel. When LOW, the Input Register is clocked by REFCLK↑ [1]. When HIGH or MID, TXCLK↑ is the Input Register clock for TXD[7:0] and TXCT[1:0].
TXCLKO±	LVTTL Output	**Transmit Clock Output**. This true and complement output clock is synthesized by the transmit PLL and operates synchronous to the internal transmit character clock. It operates at either the same frequency as REFCLK, or at twice the frequency of REFCLK (as selected by TXRATE). TXCLKO± is always equal to the transmit VCO bit-clock frequency ÷10. This output clock has no direct phase relationship to REFCLK or the recovered character clock.
TXRATE	LVTTL Input, Static Control input, internal pull-down	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiples REFCLK by 10 to generate the serial bit-rate clock. See *Table 9* for a list of operating serial rates. When REFCLK is selected to clock the receive parallel interface (RXCKSEL = LOW), the TXRATE input also determines if the clocks on the RXCLK± and RXCLKC+ outputs are full or half-rate. When TXRATE = HIGH, these output clocks are half-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE = LOW, these output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLK input.
TXCLK	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clock**. This clock must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of the input clock (relative to REFLCK or TXCLKO+) is adjusted when $\overline{\text{TXRST}}$ = LOW and locked when $\overline{\text{TXRST}}$ = HIGH.
Transmit Path Mode Control		
TXMODE[1:0]	3-Level Select [2] static control inputs	**Transmit Operating Mode**. These inputs are interpreted to select one of nine operating modes of the transmit path. See *Table 3* for a list of operating modes.
Receive Path Data Signals		
RXD[7:0]	LVTTL Output, synchronous to the RXCLK↑ output or REFCLK↑ [1] input	**Parallel Data Output**. These outputs change following the rising edge of the selected receive interface clock.
RXST[2:0]	LVTTL Output, synchronous to the RXCLK↑ output or REFCLK↑ [1] input	**Parallel Status Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is bypassed (DECMODE = LOW), RXST[1:0] become the two low-order bits of the 10-bit received character, while RXST[2] = HIGH indicates the presence of a Comma character in the Output Register. When the Decoder is enabled (DECMODE = HIGH), RXST[1:0] provide status of the received signal. See *Table 17* for a list of Receive Character status.

Note:

2. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

Pin Descriptions (continued)

CYP15G0101DXA Single Channel HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
RXOP	3-state, LVTTL Output, synchronous to the RXCLK↑ output or REFCLK↑ [1] input	**Receive Path Odd Parity**. When parity generation is enabled (PARCTL ≠ LOW), the parity output is valid for the data on the RXD bus bits. When parity generation is disabled (PARCTL = LOW) this output driver is disabled (High-Z).
Receive Path Clock and Clock Control		
RXRATE	LVTTL Input Static Control Input, internal pull-down	**Receive Clock Rate Select**. When LOW, the RXCLK± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the receive channel should be latched on either the rising edge of RXCLK+ or falling edge of RXCLK–. When HIGH, the RXCLK± recovered clock outputs are complementary clocks operating at half the character rate. Data for the receive channel should be latched alternately on the rising edge of RXCLK+ and RXCLK–. When operated with REFCLK clocking of the received parallel data outputs (RXCKSEL = LOW), RXRATE must be LOW.
RXCLK±	3-state, LVTTL Output clock	**Receive Character Clock Output or Clock Select Input**. When the receive Elasticity Buffer is disabled (RXCKSEL = MID), this true and complement clock is the Receive Interface Clock. This is used to control timing of data output transfers. This clock is output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATE. When configured such that all output data path is clocked by REFCLK instead of a recovered clock (RXCKSEL = LOW), the RXCLK± and RXCLKC+ output drivers present a buffered form of REFCLK. RXCLK± and RXCLKC+ are buffered forms of REFCLK that are slightly different in phase. This phase difference allows the user to select the optimal setup/hold timing for their specific interface.
RXCLKC+	3-state, LVTTL Output clock	**Received Character Clock Output Delayed**. When configured such that the output data path is clocked by REFCLK instead of a recovered clock (RXCKSEL = LOW), the RXCLKC+ output driver presents a buffered form of REFCLK that is slightly different in phase from RXCLK±. This phase difference allows the user to select the optimal setup/hold timing for their specific interface.
RFEN	LVTTL input, asynchronous, internal pull-down	**Reframe Enable**. Active HIGH. When HIGH, the Framer in the receive channel is enabled to frame per the presently enabled framing mode and selected framing character.
RXMODE	3-Level Select [2] static control input	**Receive Operating Mode**. This input selects one of two RXST channel status reporting modes and is only interpreted when the Decoder is enabled (DECMODE ≠ LOW). See *Table 13* for details.
RXCKSEL	3-Level Select [2] static control input	**Receive Clock Mode**. Selects the receive clock source used to transfer data to the Output Registers and configures the Elasticity Buffer in the receive path. When LOW, the Output Register is clocked by REFCLK. RXCLK± and RXCLKC+ present buffered and delayed forms of REFCLK. When MID, the RXCLK± output follows the recovered clock as selected by RXRATE and the Elasticity Buffer is bypassed. HIGH is an invalid state for this input.
FRAMCHAR	3-Level Select [2] static control input	**Framing Character Select**. Used to select the character or portion of a character used for character framing of the received data streams. When MID, the Framer looks for both positive and negative disparity versions of the 8-bit Comma character. When HIGH, the Framer looks for both positive and negative disparity versions of the K28.5 character. The LOW selection is reserved for component test.

Pin Descriptions (continued)

CYP15G0101DXA Single Channel HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
RFMODE	3-Level Select [2] static control input	**Reframe Mode Select**. Used to select the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the data stream. This signal operates in conjunction with the type of framing character selected. When LOW, the Low-Latency Framer is selected. This will frame on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode multi-byte parallel Framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phasing regardless of character offset. When HIGH, the Alternate-mode multi-byte parallel Framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received data stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phasing regardless of character offset.
DECMODE	3-Level Select [2] static control input	**Decoder Mode Select**. When LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. When MID, the Cypress Decoder table for Special Code Characters is used. When HIGH, the alternate Decoder table for Special Code Characters is used. See *Table 22* for a list of the Special Codes supported in both encoded modes.
Device Control Signals		
PARCTL	3-Level Select [2] static control input	**Parity Check/Generate Control**. Used to control the parity check and generate functions. When LOW, parity checking is disabled, and the RXOP output is disabled (High-Z). When MID, and the 8B/10B Encoder and Decoder are enabled (TXMODE[1] ≠ LOW, DECMODE ≠ LOW), TXD[7:0] inputs are checked (along with TXOP) for valid ODD parity, and ODD parity is generated for the RXD[7:0] outputs and presented on RXOP. When the 8B/10B Encoder and Decoder are disabled (TXMODE[1] = LOW, DECMODE = LOW), the TXD[7:0] and TXCT[1:0] inputs are checked (along with TXOP) for valid ODD parity, and ODD parity is generated for the RXD[7:0] and RXST[1:0] outputs and presented on RXOP. When HIGH, parity generation and checking are enabled. The TXD[7:0] and TXCT[1:0] inputs are checked (along with TXOP) for valid ODD parity, and ODD parity is generated for the RXD[7:0] and RXST[2:0] outputs and presented on RXOP.
SPDSEL	3-Level Select [2], static control input	Serial Rate Select. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 200–400 MBd, MID = 400–800 MBd, HIGH = 800–1500 MBd.
REFCLK±	Differential LVPECL or single-ended LVTTL input clock	Reference Clock. This clock input is used as the timing reference for the transmit and receive PLLs. This input clock may also be selected to clock the transmit and receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLK input, and leave the alternate REFCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface. When RXCKSEL = LOW, REFCLK is also used as the clock source for the parallel receive data (output) interface.

Pin Descriptions (continued)

CYP15G0101DXA Single Channel HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
$\overline{\text{TRSTZ}}$	LVTTL Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of REFLCK, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs will become deterministic in less than 16 REFCLK cycles. The BISTLE, OELE, and RXLE latches are reset by $\overline{\text{TRSTZ}}$. If the Elasticity Buffer or the Phase-Align Buffer are used, $\overline{\text{TRSTZ}}$ should be applied after power up to initialize the internal pointers into these memory arrays.
Analog I/O and Control		
OUT1±	CML Differential Output	**Primary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. These outputs must be AC-coupled for PECL-compatible connections.
OUT2±	CML Differential Output	**Secondary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. These outputs must be AC-coupled for PECL-compatible connections.
IN1±	LVPECL Differential Input	**Primary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The IN1± serial stream is passed to the receiver Clock and Data Recovery (CDR) circuit to extract the data content when INSEL = HIGH.
IN2±	LVPECL Differential Input	**Secondary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The IN2± serial stream is passed to the receiver Clock and Data Recovery (CDR) circuit to extract the data content when INSEL = LOW.
INSEL	LVTTL Input, asynchronous	**Receive Input Selector**. Determines which external serial bit stream is passed to the receiver Clock and Data Recovery circuit. When HIGH, the IN1± input is selected. When LOW, the IN2± input is selected.
SDASEL	3-Level Select [2], static control input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 10*.
LPEN	LVTTL Input, asynchronous, internal pull-down	**Loop-Back-Enable**. Active HIGH. When asserted (HIGH), the transmit serial data is internally routed to the receiver Clock and Data Recovery (CDR) circuit. All enabled serial drivers are forced to differential logic “1”. All serial data inputs are ignored.
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. Active HIGH. When OELE = HIGH, the signals on the BOE[1:0] inputs directly control the OUTxy± differential drivers. When the BOE[x] input is HIGH, the associated OUTx± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTx± differential driver is powered down. When OELE returns LOW, the last values present on BOE[1:0] are captured in the internal Output Enable Latch. The specific mapping of BOE[1:0] signals to transmit output enables is listed in *Table 8*. If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable both outputs.
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit and Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[1:0] inputs directly control the transmit and receive BIST enables. When the BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. When BISTLE returns LOW, the last values present on BOE[1:0] are captured in the internal BIST Enable latch. The specific mapping of BOE[1:0] signals to transmit and receive BIST enables is listed in *Table 8*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on both the transmit and receive channels.

Pin Descriptions (continued)

CYP15G0101DXA Single Channel HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-Control Latch Enable**. Active HIGH. When RXLE = HIGH, the signal on the BOE[0] input directly controls the power enable for the receive PLL and analog logic. When the BOE[0] input is HIGH, the receive channel PLL and analog logic are active. When the BOE[0] input is LOW, the receive channel PLL and analog logic are placed in a non-functional power saving mode. When RXLE returns LOW, the last value present on BOE[0] is captured in the internal RX PLL Enable latch. The specific mapping of BOE[1:0] signals to the receive channel enable is listed in *Table 8*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable the receive channel.
BOE[1:0]	LVTTL Input, asynchronous, internal pull-up	**BIST, Serial Output, and Receive Channel Enables**. These inputs are passed to and through the output enable latch when OELE = HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST enable latch when BISTLE = HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel enable latch when RXLE = HIGH, and captured in this latch when RXLE returns LOW.
$\overline{\text{LFI}}$	LVTTL Output, synchronous to the selected RXCLK↑ output or REFCLK↑ [1] input, asynchronous to receive channel enable/disable	**Link Fault Indication Output**. Active LOW. $\overline{\text{LFI}}$ is the logical OR of four internal conditions: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected 4. Receive Channel disabled
Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**
TDO	Three-State LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
TSTCLK	LVTTL Input, internal pull-up	**Test Clock Input**. For internal use. Tie HIGH for normal operation
Power		
V_{CC}		**+3.3V Power**
GND		**Signal and Power Ground for all internal circuits**

CYP15G0101DXA HOTLink II Operation

The CYP15G0101DXA is a highly configurable device designed to support reliable transfer of large quantities of data, using a high-speed serial links, from a single source to one or more destinations.

CYP15G0101DXA Transmit Data Path

Operating Modes

The transmit path of the CYP15G0101DXA supports a single-character-wide data path. This data path is used in multiple operating modes as controlled by the TXMODE[1:0] inputs.

Input Register

Within these operating modes, the bits in the Input Register support different bit assignments, based on if the character is unencoded, encoded with two control bits, or encoded with three control bits. These assignments are shown in *Table 1*.

Table 1. Input Register Bit Assignments[3]

Signal Name	Unencoded (Encoder Bypassed)	Encoded (Encoder Enabled)	
		2-bit Control	3-bit Control
TXD[0] (LSB)	DIN[0]	TXD[0]	TXD[0]
TXD[1]	DIN[1]	TXD[1]	TXD[1]
TXD[2]	DIN[2]	TXD[2]	TXD[2]
TXD[3]	DIN[3]	TXD[3]	TXD[3]
TXD[4]	DIN[4]	TXD[4]	TXD[4]
TXD5]	DIN[5]	TXD[5]	TXD[5]
TXD[6]	DIN[6]	TXD[6]	TXD[6]
TXD[7]	DIN[7]	TXD[7]	TXD[7]
TXCT[0]	DIN[8]	TXCT[0]	TXCT[0]
TXCT[1] (MSB)	DIN[9]	TXCT[1]	TXCT[1]
SCSEL	N/A	N/A	SCSEL

Note:
3. The TXOP input is also captured in the Input Register, but its interpretation is under the separate control of PARCTL.

The Input Register captures a minimum of eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the control bits are part of the pre-encoded 10-bit data character.

When the Encoder is enabled (TXMODE[1] ≠ LOW), the TXCT[1:0] bits are interpreted along with the TXD[7:0] character to generate the specific 10-bit transmission character. When TXMODE[0] ≠ HIGH, an additional special character select (SCSEL) input is also captured and interpreted. This SCSEL input is used to modify the encoding of the characters.

Phase-Align Buffer

Data from the Input Register is passed either to the Encoder or to the Phase-Align buffer. When the transmit path is operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the Phase-Align Buffer is bypassed and data is passed directly to the Parity Check and Encoder block to reduce latency.

When an Input-Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the Phase-Align Buffer is enabled. This buffer is used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of the Phase-Align Buffer takes place when the $\overline{\text{TXRST}}$ input is sampled LOW by TXCLK↑. When $\overline{\text{TXRST}}$ is returned HIGH, the present input clock phase relative to REFCLK↑ is set. $\overline{\text{TXRST}}$ is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machine. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive TXCLK↑ clocks to ensure the reset operation is initiated correctly.

Once set, the input clock is allowed to skew in time up to half a character period in either direction relative to REFCLK↑; i.e., ±180°. This time shift allows the delay path of the character clock (relative to REFLCK↑) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on the TXPER output. This output indicates a continuous error until the Phase-Align Buffer is reset. While the error remains active, the transmitter will output a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

In specific transmit modes it is also possible to reset the Phase-Align Buffer and with minimal disruption of the serial data stream. When the transmit interface is configured for generation of atomic Word Sync Sequences (TXMODE[1] = MID) and a Phase-Align Buffer error is present, the transmission of a Word Sync Sequence will re-center the Phase-Align Buffer and clear the error condition.

> **NOTE**: One or more K28.5 characters may be added or lost from the data stream during this reset operation. When used with non-Cypress devices that require a complete 16-character Word Sync Sequence for proper receive Elasticity Buffer alignment, it is recommend that the sequence be followed by a second Word Sync Sequence to ensure proper operation.

Parity Support

In addition to the ten data and control bits that are captured at the transmit Input Register, a TXOP input is also available. This allows the CYP15G0101DXA to support ODD parity checking. Parity checking is available for all operating modes (including Encoder Bypass). The specific mode of parity checking is controlled by the PARCTL input, and operates per *Table 2*.

When PARCTL = MID (open) and the Encoder is enabled (TXMODE[1] ≠ LOW), only the TXD[7:0] data bits are checked for ODD parity along with the TXOP bit. When PARCTL = HIGH with the Encoder enabled (or MID with the Encoder bypassed), the TXD[7:0] and TXCT[1:0] inputs are checked for ODD parity along with the TXOP bit. When PARCTL = LOW, parity checking is disabled.

When parity checking and the Encoder are both enabled (TXMODE[1] ≠ LOW), the detection of a parity error causes a C0.7 character of proper disparity to be passed to the Transmit Shifter. When the Encoder is bypassed (TXMODE[1] = LOW),

Table 2. Input Register Bits Checked for Parity[4]

Signal Name	Transmit Parity Check Mode (PARCTL)			
	LOW	MID		HIGH
		TXMODE[1] = LOW	TXMODE[1] ≠ LOW	
TXD[0]		X[5]	X	X
TXD[1]		X	X	X
TXD[2]		X	X	X
TXD[3]		X	X	X
TXD[4]		X	X	X
TXD[5]		X	X	X
TXD[6]		X	X	X
TXD[7]		X	X	X
TXCT[0]		X		X
TXCT[1]		X		X
TXOP		X	X	X

Note:
4. Transmit path parity errors are reported on the TXPER output.
5. Bits marked as X are XORed together. Result must be a logic-1 for parity to be valid.

detection of a parity error causes a positive disparity version of a C0.7 transmission character to be passed to the Transmit Shifter.

Encoder

The character, received from the Input Register or Phase-Align Buffer and Parity Check Logic, is then passed to the Encoder logic. This block interprets each character and any control bits, and outputs a 10-bit transmission character.

Depending on the configured operating mode, the generated transmission character may be

- the 10-bit pre-encoded character accepted in the Input Register
- the 10-bit equivalent of the 8-bit Data character accepted in the Input Register
- the 10-bit equivalent of the 8-bit Special Character code accepted in the Input Register
- the 10-bit equivalent of the C0.7 SVS character if parity checking was enabled and a parity error was detected
- the 10-bit equivalent of the C0.7 SVS character if a Phase-Align Buffer overflow or underflow error is present
- a character that is part of the 511-character BIST sequence
- a K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

The selection of the specific characters generated are controlled by the TXMODE[1:0], SCSEL, TXCT[1:0], and TXD[7:0] inputs for each character.

Data Encoding

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- a minimum transition density (to allow the serial receive PLL to extract a clock from the data stream)
- a DC-balance in the signaling (to prevent baseline wander)
- run-length limits in the serial data (to limit the bandwidth of the link)
- the remote receiver a way of determining the correct character boundaries (framing).

When the Encoder is enabled (TXMODE[1] ≠ LOW), the characters to be transmitted are converted from Data or Special Character codes to 10-bit transmission characters (as selected by the TXCT[1:0] and SCSEL inputs), using an integrated 8B/10B Encoder. When directed to encode the character as a Special Character code, it is encoded using the Special Character encoding rules listed in *Table 22*. When directed to encode the character as a Data character, it is encoded using the Data Character encoding rules in *Table 21*.

The 8B/10B Encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON™ channels, Digital Video Broadcast (DVB-ASI) and ATM Forum standards for data transport.

Many of the Special Character codes listed in *Table 22* may be generated by more than one input character. The CYP15G0101DXA is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP15G0101DXA to operate in mixed environments with other Cypress HOTLink devices using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from 8 bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Transmit Modes

The operating mode of the transmit path is set through the TXMODE[1:0] inputs. These 3-level select inputs allow one of nine transmit modes to be selected. Within each of these operating modes, the actual characters generated by the Encoder logic block are also controlled both by these and other static and dynamic control signals. The transmit modes are listed in *Table 3*.

The encoded modes (TX Modes 3 through 8) support multiple encoding tables. These encoding tables vary by the specific combinations of SCSEL, TXCT[1], and TXCT[0] that are used to control the generation of data and control characters. These multiple encoding forms allow maximum flexibility in interfacing to legacy applications, while also supporting numerous extensions in capabilities.

TX Mode 0—Encoder Bypass

When the Encoder is bypassed, the character captured from the TXD[7:0] and TXCT[1:0] inputs is passed directly to the Transmit Shifter without modification. If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character is replaced with the 1001111000 pattern (+C0.7 character) regardless of the running disparity of the previous character.

With the Encoder bypassed, the TXCT[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the

Table 3. Transmit Operating Modes

TX Mode		Operating Mode		
Mode Number	TXMODE [1:0]	Word Sync Sequence Support	SCSEL Control	TXCT Function
0	LL	None	None	Encoder Bypass
1	LM	None	None	Reserved for test
2	LH	None	None	Reserved for test
3	ML	Atomic	Special Character	Encoder Control
4	MM	Atomic	Word Sync	Encoder Control
5	MH	Atomic	None	Encoder Control
6	HL	Interruptible	Special Character	Encoder Control
7	HM	Interruptible	Word Sync	Encoder Control
8	HH	Interruptible	None	Encoder Control

TXD[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in *Table 4*.

In Encoder Bypass mode the SCSEL input is ignored. All clocking modes interpret the data in the same way.

Table 4. Encoder Bypass Mode (TXMODE[1:0] = LL)

Signal Name	Bus Weight	10B Name
TXD[0] (LSB)	2^0	a[6]
TXD[1]	2^1	b
TXD[2]	2^2	c
TXD[3]	2^3	d
TXD[4]	2^4	e
TXD[5]	2^5	i
TXD[6]	2^6	f
TXD[7]	2^7	g
TXCT[0]	2^8	h
TXCT[1] (MSB)	2^9	j

Note:
6. LSB is shifted out first.

TX Modes 1 and 2—Factory Test Modes

These modes enable specific factory test configurations. They are not considered normal operating modes of the device. Entry or configuration into these test modes will not damage the device.

TX Mode 3—Atomic Word Sync and SCSEL Control of Special Codes

When configured in TX Mode 3, the SCSEL input is captured along with the TXCT[1:0] data control inputs. These bits combine to control the interpretation of the TXD[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 5*.

When TXCKSEL = MID, the transmit channel captures data into its Input Register using the TXCLK clock.

Table 5. TX Modes 3 and 6 Encoding

SCSEL	TXCT[1]	TXCT[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
1	0	1	Special character code
X	1	1	16-character Word Sync Sequence

Word Sync Sequence

When TXCT[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the transmit channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence follow a pattern of either ++−−+−+−+−+−+−+− or −−++−+−+−+−+−+.

When TXMODE[1] = MID (open, TX modes 3, 4, and 5), the generation of this character sequence is an atomic (non-interruptible) operation. Once it has been successfully started, it cannot be stopped until all 16 characters have been generated. The content of the Input Register is ignored for the duration of this 16-character sequence. At the end of this sequence, if the TXCT[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterruptible for the following 15 character clocks.

If parity checking is enabled, the character used to start the Word Sync Sequence must also have correct ODD parity. This is true even though the contents of the TXD[7:0] bits do not directly control the generation of characters during the Word Sync Sequence. Once the sequence is started, parity is not checked on the following 15 characters in the Word Sync Sequence.

When TXMODE[1] = HIGH (TX modes 6, 7, and 8), the generation of the Word Sync Sequence becomes an interruptible operation. In TX Mode 6, this sequence is started as soon as the TXCT[1:0] = 11 condition is detected on the channel. In order for the sequence to continue, the TXCT[1:0] inputs must be sampled as 00 for the remaining 15 characters of the sequence.

If at any time a sample period exists where TXCT[1:0] ≠ 00, the Word Sync Sequence is terminated, and a character representing the data and control bits is generated by the Encoder. This resets the Word Sync Sequence state machine such that it will start at the beginning of the sequence at the next occurrence of TXCT[1:0] = 11.

When parity checking is enabled and TXMODE[1] = HIGH, all characters (including those in the middle of a Word Sync Sequence) must have correct parity. The detection of a character with incorrect parity during a Word Sync Sequence (regardless of the state of TXCT[1:0]) will interrupt that sequence and force generation of a C0.7 SVS character. Any interruption of the Word Sync Sequence causes the sequence to terminate.

When TXCKSEL = LOW, the Input Register for the transmit channel is clocked by REFCLK [1]. When TXCKSEL = HIGH, the Input Register for the transmit channel is clocked with TXCLK↑.

TX Mode 4—Atomic Word Sync and SCSEL Control of Word Sync Sequence Generation

When configured in TX Mode 4, the SCSEL input is captured along with the TXCT[1:0] data control inputs. These bits combine to control the interpretation of the TXD[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 6*.

Table 6. TX Modes 4 and 7 Encoding

SCSEL	TXCT[1]	TXCT[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
0	1	1	Special character code
1	X	1	16-character Word Sync Sequence

TX Mode 4 also supports an Atomic Word Sync Sequence. Unlike TX Mode 3, this sequence is started when both SCSEL and TXCT[0] are sampled HIGH. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this Word Sync Sequence is the same as that documented for TX Mode 3.

TX Mode 5—Atomic Word Sync, No SCSEL

When configured in TX Mode 5, the SCSEL signal is not used. The TXCT[1:0] inputs control the characters generated by the channel. The specific characters generated by these bits are listed in *Table 7*.

Table 7. TX Modes 5 and 8 Encoding

SCSEL	TXCT[1]	TXCT[0]	Characters Generated
X	0	0	Encoded data character
X	0	1	K28.5 fill character
X	1	0	Special character code
X	1	1	16-character Word Sync Sequence

TX Mode 5 also has the capability of generating an Atomic Word Sync Sequence. For the sequence to be started, the TXCT[1:0] inputs must both be sampled HIGH. The generation and operation of this Word Sync Sequence is the same as that documented for TX Mode 3.

Transmit BIST

The transmit channel contains an internal pattern generator that can be used to validate both device and link operation. This generator is enabled by the BOE[1] signal, as listed in *Table 8* (when the BISTLE latch enable input is HIGH). When enabled, a register in the transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver.

When the BISTLE signal is HIGH, if the BOE[1] input is LOW the BIST generator in the transmit channel is enabled (and if BOE[0] = LOW the BIST checker in the receive channel is enabled). When BISTLE returns LOW, the values of the BOE[1:0] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned high to open the latch again. A device reset (TRSTZ sampled LOW), also presets the BIST Enable Latch to disable BIST on both the transmit and receive channels.

All data and data-control information present at the TXD[7:0] and TXCT[1:0] inputs are ignored when BIST is active on the transmit channel. If the receive channel is configured for common clock operation (RXCKSEL = LOW) each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock-frequency variations.

Serial Output Drivers

The serial interface Output Drivers use high-performance differential CML (Current Mode Logic) to provide source-matched drivers for the transmission lines. These Serial Drivers accept data from the Transmit Shifter. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or AC-coupled transmission lines.

When configured for local loopback (LPEN = HIGH), the enabled Serial Drivers are configured to drive a static differential logic-1.

Each Serial Driver can be enabled or disabled through the BOE[1:0] inputs, as controlled by the OELE latch-enable signal. When OELE = HIGH, the signals present on the BOE[1:0] inputs are passed through the Serial Output Enable latch to control the Serial Driver. The BOE[1:0] input with OUT1± and OUT2± driver is listed in *Table 8*.

Table 8. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[1]	OUT2±	Transmit	X
BOE[0]	OUT1±	Receive	Receive

When OELE = HIGH and BOE[x] = HIGH, the associated Serial Driver is enabled to drive any attached transmission line. When OELE = HIGH and BOE[x] = LOW, the associated driver is disabled and internally configured for minimum power dissipation. If both Serial Drivers for the channel are disabled, the internal logic for the channel is also configured for lowest power operation. When OELE returns LOW, the values present on the BOE[1:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to open the latch again. A device reset (TRSTZ sampled LOW) clears this latch and disables both Serial Drivers.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiples that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit path.

This clock multiplier PLL can accept a REFCLK input between 20 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP15G0101DXA clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

SPDSEL is a 3-level select[2] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signaling-rate and allowable range of REFCLK frequencies are listed in *Table 9*.

Table 9. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	200–400
	0	20–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.4V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC-or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so it is necessary to ensure that the 0V-differential crossing point remains within the parametric range supported by the input.

CYP15G0101DXA Receive Data Path

Serial Line Receivers

Two differential Line Receivers, IN1± and IN2±, are available for accepting serial data streams. The active Serial Line Receiver is selected using the INSEL input. Both Serial Line Receivers have differential inputs, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL logic family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local loopback input (LPEN) allows the serial transmit data to be routed internally back to the Clock and Data Recovery circuit. When configured for local loopback, the transmit Serial Driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

Signal Detect / Link Fault

Each selected Line Receiver (i.e., that routed to the Clock and Data Recovery PLL) is simultaneously monitored for

- analog amplitude
- transition density
- Range Control logic report the received data stream inside normal frequency range (±200 ppm)
- receive channel enabled.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the $\overline{LFI}$ (Link Fault Indicator) output which changes synchronous to the selected receive interface clock.

Table 10. Analog Amplitude Detect Valid Signal Levels

SDASEL	Typical signal with peak amplitudes above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a 3-level select[2] (ternary) input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 10*.

The Analog Signal Detect monitor is active for the present Line Receiver, as selected by the INSEL input. When configured for local loopback (LPEN = HIGH), no Line Receiver is selected, and the $\overline{LFI}$ output reports only the receive VCO frequency out-of-range and transition density status. When local loopback is active, the Analog Signal Detect monitor is disabled.

Transition Density

The Transition Detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received (within the referenced period), the Transition Detection logic asserts $\overline{LFI}$. The $\overline{LFI}$ output remains asserted until at least one transition is detected in each of three adjacent received characters.

Range Control

The receive-VCO Range-Control Monitor tracks the frequency of the received signal relative to REFCLK. It also determines if the receive Clock/Data Recovery circuit (CDR) should align the receive-VCO clock to the data stream or to the local REFCLK input. This prevents the receive VCO from tracking an out-of-specification received signal.

When the Range-Control Monitor indicates that the signaling rate is within specification, the phase detector in the receive PLL is configured to track the transitions in the received data

stream. In this mode the $\overline{LFI}$ output is HIGH (unless one of the other status monitors indicates that the received signal is out of specification). If the Range-Control Monitor indicates that the received data stream signaling-rate is out of specification, the phase detector is configured to track the local REFCLK input, and the $\overline{LFI}$ output is asserted LOW.

The specific trip points for this compare function are listed in *Table 11*. Because the compare function operates with two asynchronous clocks, there is a small uncertainty in the measurement. The switch points are asymmetric to provide hysteresis to the operation.

Table 11. Receive Signaling Rate Range Control criteria

Current RX PLL Tracking Source	Frequency Difference Between Transmit Character Clock & RX VCO	Next RX PLL Tracking Source
Selected data stream ($\overline{LFI}$ = HIGH)	<1708 ppm	Data Stream
	1708-1953 ppm	Indeterminate
	>1953 ppm	REFCLK
REFCLK ($\overline{LFI}$ = LOW)	<488 ppm	Data Stream
	488-732 ppm	Indeterminate
	>732 ppm	REFCLK

Receive Channel Enabled

The CYP15G0101DXA receive channel can be enabled and disabled through the BOE[0] input, as controlled by the RXLE latch-enable signal. When RXLE = HIGH, the signal present on the BOE[0] inputs is passed through the Receive Channel Enable Latch to control the PLL and logic of the receive channel. The BOE[1:0] input functions are listed in *Table 8*.

When RXLE = HIGH and BOE[0] = HIGH, the receive channel is enabled to receive and decode a serial stream from the Line Receiver. When RXLE = HIGH and BOE[0] = LOW, the receive channel is disabled and internally configured for minimum power dissipation. When disabled, the channel indicates a constant $\overline{LFI}$ output. When RXLE returns LOW, the values present on the BOE[1:0] inputs are latched in the Receive Channel Enable Latch, and remain there until RXLE returns HIGH to opened the latch again.

Note: When a disabled receive channel is re-enabled, the status of the $\overline{LFI}$ output and data on the parallel outputs may be indeterminate for up to 10ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from a received serial stream is performed by a Clock/Data Recovery (CDR) block within the receive channel. The clock extraction function is performed by a high-performance embedded phase-locked loop (PLL) that tracks the frequency of the transitions in the incoming bit stream and aligns the phase of the internal bit-rate clock to the transitions in the serial data stream.

The CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to ensure that the VCO (within the CDR) is operating at the correct frequency (rather than some harmonic of the bit-rate)

- to reduce PLL acquisition time
- and to limit unlocked frequency excursions of the CDR VCO when there is no input data is present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR will attempt to recover a data bit stream from it. If the frequency of the recovered data stream is outside the limits set by the Range Control Monitor, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ±200 ppm of the frequency of the clock that drives the REFCLK input of the *remote* transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{LFI}$ output can be used to select an alternate data stream. When an $\overline{LFI}$ indication is detected, external logic can toggle selection of the IN1± and IN2± inputs through the INSEL input. When a port switch takes place, it is necessary for the receive PLL to reacquire the new serial stream and frame to the incoming character boundaries.

Deserializer/Framer

Each CDR circuit extracts bits from the serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more Comma or K28.5 characters at all possible bit positions. The location of these characters in the data stream are used to determine the character boundaries of all following characters.

Framing Character

The CYP15G0101DXA allows selection of either of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

The specific bit combinations of these framing characters are listed in *Table 12*. When the specific bit combination of the selected framing character is detected by the Framer, the boundaries of the characters present in the received data stream are known.

Table 12. Framing Character Selector

FRAMCHAR	Bits detected in Framer	
	Character Name	Bits Detected
MID (Open)	Comma+ Comma–	00111110XX[7] or 11000001XX
HIGH	–K28.5 +K28.5	0011111010 or 1100000101

Note:

7. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the 8th bit as an inversion of the 7th bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.

Framer

The Framer operates in one of three different modes, as selected by the RFMODE input. In addition, the Framer itself may be enabled or disabled through the RFEN input. When RFEN = LOW, the Framer is disabled, and no combination of bits in a received data stream will alter the character bound-

aries. When RFEN = HIGH, the Framer-mode selected by RFMODE is enabled.

When RFMODE = LOW, the Low-Latency Framer is selected. This Framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode the Framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to 14 character-clock cycles from the detection of the selected framing character.

NOTE: When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which would cause the Receiver to update its character boundaries incorrectly.

When RFMODE = MID (open) the Cypress-mode multi-byte Framer is selected. The required detection of multiple framing characters makes the link much more robust to incorrect framing due to aliased SYNC characters in the data stream. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE = HIGH, the Alternate-mode multi-byte Framer is enabled. Like the Cypress-mode multi-byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

Framing is enabled when RFEN = HIGH. If RFEN = LOW, the Framer is disabled. When the Framer is disabled, no changes are made to the recovered character boundary, regardless of the presence of framing characters in the data stream.

10B/8B Decoder Block

The Decoder logic block performs three primary functions:

- decoding the received transmission characters back into Data and Special Character codes,
- comparing generated BIST patterns with received characters to permit at-speed link and device testing,
- and generation of ODD parity on the decoded characters.

10B/8B Decoder

The framed parallel output of the Deserializer Shifter is passed to the 10B/8B Decoder where, if the Decoder is enabled (DECMODE ≠ LOW), it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the 10B/8B Decoder patterns in *Table 21* and *Table 22* of this data sheet. Valid data characters are indicated by a 000b bit-combination on the RXST[2:0] status bits, and Special Character codes are indicated by a 001b bit-combination on these same status outputs. Framing characters, invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

The 10B/8B Decoder operates in two normal modes, and can also be bypassed. The operating mode for the Decoder is controlled by the DECMODE input.

When DECMODE = LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. In this mode, the receive Elasticity Buffers are bypassed, and RXCKSEL must be MID. This clock mode generates separate RXCLK± outputs for the receive channel.

When DECMODE = MID (or open), the 10-bit transmission characters are decoded using *Table 21* and *Table 22*. Received Special Code characters are decoded using the Cypress column of *Table 22*.

When DECMODE = HIGH, the 10-bit transmission characters are decoded using *Table 21* and *Table 22*. Received Special Code characters are decoded using the Alternate column of *Table 22*.

Receive BIST Operation

The Receiver interface contains an internal pattern generator that can be used to validate both device and link operation. This generator is enabled by the BOE[0] signal as listed in *Table 8* (when the BISTLE latch enable input is HIGH). When enabled, a register in the Receive channel becomes a pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter. When synchronized with the received data stream, the Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXST[2:0] bits of the Output Register.

When the BISTLE signal is HIGH, if the BOE[0] input is LOW the BIST generator/checker in the Receive channel is enabled (and if BOE[1] = LOW the BIST generator in the transmit channel is enabled). When BISTLE returns LOW, the values of the BOE[1:0] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned high to open the latch again. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This D0.0 character is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the RXST[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXST[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the Decoder is bypassed and BIST is enabled on the Receive channel.

The specific status reported by the BIST state machine are listed in *Table 17*. These same codes are reported on the receive status outputs regardless of the state of DECMODE.

The specific patterns checked by each receiver are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence compared by the CYP15G0101DXA is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for common clock operation (RXCKSEL = LOW) each pass must be preceded by a 16-character Word Sync Sequence to allow output buffer alignment and management of clock frequency variations. This is automatically generated by the transmitter when its local RXCKSEL = LOW.

The BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low-Latency Framer is enabled (RFMODE = LOW), the Framer will misalign to an aliased SYNC character within the BIST sequence. If the Alternate-mode Multi-Byte Framer is enabled (RFMODE = HIGH) and the Receiver outputs are clocked relative to a recovered clock (RXCKSEL = MID), it is generally necessary to frame the Receiver before BIST is enabled. If the Receiver outputs are clocked relative to REFCLK (RXCKSEL = LOW), the transmitter precedes every 511 character BIST sequence with a 16-character Word Sync Sequence. This sequence will frame the Receiver regardless of the setting of RFMODE.

Receive Elasticity Buffer

The receive channel contains an Elasticity Buffer that is designed to support multiple clocking modes. This buffer allows data to be read using an Elasticity Buffer read-clock that is asynchronous in both frequency and phase from the Elasticity Buffer write clock, or to use a read clock that is frequency coherent but with uncontrolled phase relative to the Elasticity Buffer write clock.

The Elasticity Buffer is a minimum of 10-characters deep, and supports a 12-bit wide data path. It is capable of supporting a decoded character, three status bits, and a parity bit for each character present in the buffer. The write clock for this buffer is always the recovered clock for the read channel.

The read clock for the Elasticity Buffer may come from one of two selectable sources. It may be a

- character-rate REFCLK
- recovered clock from the receive channel

Receive Modes

The operating mode of the receive path is set through the RXMODE input. This RXMODE input is only interpreted when the Decoder is enabled (DECMODE ≠ LOW). These modes determine the RXST status reporting. The different receive modes are listed in *Table 13*.

When RXCKSEL = LOW, the Receive channel is clocked by REFCLK. The RXCLK± and RXCLKC+ outputs presents buffered and delayed forms of REFCLK. In this mode, the receive Elasticity Buffer is enabled. For REFCLK clocking, the Elasticity Buffer must be able to insert K28.5 characters and delete framing characters as appropriate.

Table 13. Receive Operating Modes

RX Mode		Operating Mode	
Mode Number	RXMODE	Channel Mode	RXST Status Reporting
0	L	Independent	Status A
1	M		Reserved for test
2	H	Independent	Status B

The insertion of a K28.5 or deletion of a framing character can occur at any time, however, the actual timing on these insertions and deletions is controlled in part by the how the transmitter sends its data. Insertion of a K28.5 character can only occur when the receiver has a framing character in the Elasticity Buffer. Likewise, to delete a framing character, one must also be in the Elasticity Buffer. To prevent an Elasticity Buffer overflow or underflow in the receive channel, a minimum density of framing characters must be present in the received data stream.

Prior to reception of valid data, at least one Word Sync Sequence (or that portion of one necessary to center the Elasticity Buffer) must be received to allow the receive Elasticity Buffer to be centered. The Elasticity Buffer may also be centered by a device reset operation initiated through the $\overline{\text{TRSTZ}}$ input, however, following such an event the CYP15G0101DXA will normally require a framing event before it will correctly decode characters.

When RXCKSEL = MID (or open), the received channel Output Register is clocked by the recovered clock. Since no characters may be added or deleted, the receiver Elasticity Buffer is bypassed.

Power Control

The CYP15G0101DXA supports user control of the powered up or down state of the Transmit and Receive channel. The Receive channel is controlled by the RXLE signal and the values present on the BOE[1:0] bus. The Transmit channel is controlled by the OELE signal and the values present on the BOE[1:0] bus. If either the Transmit or the Receive channel is not used, then powering down the unused channel will save power and reduce system heat generation. Controlling system power dissipation will improve the system performance.

Receive Channel

When RXLE = HIGH, the signal on the BOE[0] input directly controls the power enable for the receive PLL and the analog circuit. When BOE[0] = HIGH, the Receive channel and its analog circuits are active. When BOE[0] = LOW, the Receive channel and its analog circuits are powered down. When a disabled receive channel is re-enabled, the status of the $\overline{\text{LFI}}$ output and data on the parallel outputs for the Receive channel may be indeterminate for up to 10 ms.

Transmit Channel

When OELE = HIGH, the signals on the BOE[1:0] inputs directly control the power enables for the Serial Drivers. When a BOE[1:0] input is HIGH, the associated Serial Driver is en-

abled. When a BOE[1:0] input is LOW, the associated Serial Driver is disabled. When OELE returns LOW, the values present on the BOE[1:0] inputs are latched in the Output Enable Latch.

Device Reset State

When the CYP15G0101DXA is reset by assertion of $\overline{\text{TRSTZ}}$, both the Transmit Enable and Receive Enable Latches are cleared, and the BIST Enable Latch is preset. In this state, the Transmit and Receive channels are disabled, and BIST is disabled.

Following a device reset, it is necessary to enable the transmit and receive channels for normal operation. This can be done by sequencing the appropriate values on the BOE[1:0] inputs while the OELE and RXLE signals are raised and lowered. For systems that do not require dynamic control of power, or want the part to power up in a fixed configuration, it is also possible to strap the RXLE and OELE control signals HIGH to permanently enable their associated latches. Connection of the associated BOE[1:0] signals HIGH will then enable the Transmit and Receive channels as soon as the $\overline{\text{TRSTZ}}$ signal is deasserted.

Output Bus

The receive channel presents a 12-signal output bus consisting of

- an 8-bit data bus
- a 3-bit status bus
- a parity bit

The signals present on this output bus are modified by the present operating mode of the CYP15G0101DXA as selected by DECMODE. This mapping is shown in *Table 14*.

Table 14. Output Register Bit Assignments[8]

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXST[2] (LSB)	COMDET	RXST[2]
RXST[1]	DOUT[0]	RXST[1]
RXST[0]	DOUT[1]	RXST[0]
RXD[0]	DOUT[2]	RXD[0]
RXD[1]	DOUT[3]	RXD[1]
RXD[2]	DOUT[4]	RXD[2]
RXD[3]	DOUT[5]	RXD[3]
RXD[4]	DOUT[6]	RXD[4]
RXD[5]	DOUT[7]	RXD[5]
RXD[6]	DOUT[8]	RXD[6]
RXD[7] (MSB)	DOUT[9]	RXD[7]

Note:
8. The RXOP output is also driven from the Output Register, but its interpretation is under the separate control of PARCTL.

When the 10B/8B Decoder is bypassed (DECMODE = LOW), the framed 10-bit character and a single status bit are presented to the receiver Output Register, along with a status output indicating if the character in the Output Register is one of the selected framing characters. The bit usage and mapping of the external signals to the raw 10B transmission character is shown in *Table 15*.

Table 15. Decoder Bypass Mode (DECMODE = LOW)

Signal Name	Bus Weight	10B Name
RXST[2] (LSB)	COMDET	
RXST[1]	2^0	a
RXST[0]	2^1	b
RXD[0]	2^2	c
RXD[1]	2^3	d
RXD[2]	2^4	e
RXD[3]	2^5	i
RXD[4]	2^6	f
RXD[5]	2^7	g
RXD[6]	2^8	h
RXD[7] (MSB)	2^9	j

The COMDET status output operates the same regardless of the bit combination selected for character framing by the FRAMCHAR input. It is HIGH when the character in the Output Register contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the Low-Latency Framer and half-rate receive port clocking is also enabled (RFMODE = LOW, RXRATE = HIGH, and RXCKSEL = MID), the Framer will stretch the recovered clock to the nearest 20-bit boundary such that the rising edge of RXCLK+ occurs when COMDET = HIGH in the Output Register.

When the Cypress or Alternate-mode Framer is enabled and half-rate receive port clocking is also enabled (RFMODE ≠ LOW and RXRATE = HIGH), the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the Framer logic such that the rising edge of RXCLK+ occurs when COMDET = HIGH in the Output Register.

This adjustment only occurs when the Framer is enabled (RFEN = HIGH). When the Framer is disabled, the clock boundaries are not adjusted, and COMDET may be asserted during the rising edge of RXCLK– (if an odd number of characters were received following the initial framing).

Parity Generation

In addition to the eleven data and status bits that are presented, an RXOP parity output is also available. This allows the CYP15G0101DXA to support ODD parity generation. To handle a wide range of system environments, the CYP15G0101DXA supports multiple different forms of parity generation (in addition to no parity). When the Decoder is enabled (DECMODE ≠ LOW), parity can be generated on

- the RXD[7:0] character
- the RXD[7:0] character and RXST[2:0] status

When the Decoder is bypassed (DECMODE = LOW), parity can be generated on

- the RXD[7:0] and RXST[1:0] bits
- the RXD[7:0] and RXST[2:0] bits

These modes differ in the number bits which are included in the parity calculation. For all cases, only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 16*.

Table 16. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)			
	LOW[9]	MID		HIGH
		DECMODE = LOW	DECMODE ≠ LOW	
RXST[2]				X[10]
RXST[1]		X		X
RXST[0]		X		X
RXD[0]		X	X	X
RXD[1]		X	X	X
RXD[2]		X	X	X
RXD[3]		X	X	X
RXD[4]		X	X	X
RXD[5]		X	X	X
RXD[6]		X	X	X
RXD[7]		X	X	X

Notes:

9. Receive path parity output drivers (RXOPx) are disabled (High-Z) when PARCTL = LOW
10. When the Decoder is bypassed (DECMODE = LOW) and BIST is not enabled (Receive BIST Latch output is HIGH), RXSTx[2] is driven to a logic-0, except when the character in the output buffer is a framing character.

Parity generation is enabled through the 3-level select PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOP output is disabled (High-Z).

When PARCTL = MID (open) and the Decoder is enabled (DECMODE ≠ LOW), ODD parity is generated for the received and decoded character in the RXD[7:0] signals and is presented on the RXOP output.

When PARCTL = MID (open) and the Decoder is bypassed (DECMODE = LOW), ODD parity is generated for the received and decoded character in the RXD[7:0] and RXST[1:0] bit positions.

When PARCTL = HIGH, ODD parity is generated for the TXD[7:0] and the RXST[2:0] status bits.

When the Output Register clocking is such that the decoded character is passed through the receive Elasticity Buffer prior to the addition of the RXST[2:0] status bits, the output parity calculation becomes a two-step process. The first parity calculation takes place as soon as the character is framed and decoded. This generates proper parity for the data portion of the decoded character which is then written to the Elasticity Buffer. If the parity calculation also includes the RXST[2:0] status bits (PARCTL = HIGH), a second parity calculation is made prior to loading the data and status bits into the receive Output Register. This is necessary because the status bits with a character in the Output Register are not necessarily determined until after the character is read from the receive Elasticity Buffer.

This second parity calculation is based only on the content of the status bits, and the singular parity bit associated with the character read from the Elasticity Buffer.

Receive Status Bits

When the 10B/8B Decoder is enabled (DECMODE ≠ LOW), each character presented at the Output Register includes three associated status bits. These bits are used to identify

- if the contents of the data bus are valid,
- the type of character present,
- the state of receive BIST operations (regardless of the state of DECMODE),
- character violations.

These conditions normally overlap; e.g., a valid data character received with incorrect running disparity is not reported as a valid data character. It is instead reported as a Decoder violation of some specific type. This implies a hierarchy or priority level to the various status bit combinations. The hierarchy and value of each status is listed in *Table 17*.

Within these status decodes, there are three forms of status reporting. The two normal or data status reporting modes (Type A and Type B) are selectable through the RXMODE input. These status types allow compatibility with legacy systems, while allowing full reporting in new systems. The third status type is used for reporting receive BIST status and progress.

BIST Status State Machine

When the receive path is enabled to look for and compare the received data stream with the BIST pattern, the RXST[2:0] bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in *Figure 2* and *Table 17*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the interface for the first character (D0.0) of the next BIST sequence. Also, if the Elasticity Buffer ever hits and overflow/underflow condition, the status is forced to the BIST_START until the buffer is re-centered (approximately nine character periods).

To ensure compatibility between the source and destination systems when operating in BIST, the sending and receiving ends of the BIST sequence must use the same clock set-up (RXCKSEL = MID or RXCKSEL = LOW).

JTAG Support

The CYP15G0101DXA contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs and outputs and the REFCLK± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP15G0101DXA is ‘0C800069’x.

3-Level Select Inputs

Each 3-Level select inputs reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively.

Table 17. Receive Character Status Bits

RXST[2:0]	Priority	Description		
		Type-A Status	Type-B Status	Receive BIST Status (Receive BIST = Enabled)
000	7	**Normal Character Received.** The valid Data character on the output bus meets all the formatting requirements of Data characters listed in *Table 21*.		**BIST Data Compare.** Character compared correctly
001	7	**Special Code Detected.** The valid special character on the output bus meets all the formatting requirements of the Special Code characters listed in *Table 22*, but is not the presently selected framing character or a Decoder violation indication.		**BIST Command Compare.** Character compared correctly
010	2	**Receive Elasticity Buffer Underrun/Overrun Error.** The receive buffer was not able to add/drop a K28.5 or framing character.	**RESERVED**	**BIST Last Good.** Last Character of BIST sequence detected and valid.
011	5	**Framing Character detected.** This indicates that a character matching the patterns identified as a framing character (as selected by FRAMCHAR) was detected. The decoded value of this character is present in the output bus.		
100	4	**Codeword Violation.** The character on the output bus is a C0.7. This indicates that the received character cannot be decoded into any valid character.		**BIST Last Bad.** Last Character of BIST sequence detected invalid.
101	1	**Loss of Sync.** The character on the bus is invalid, due to an event that has caused the receive channels to lose synchronization. This indicates a PLL Out of Lock condition.	**Loss of Sync.** The character on the bus is invalid, due to an event that has caused the receive channels to lose synchronization. This indicates a loss of character framing. Also used to indicate receive Elasticity Buffer underflow/overflow errors.	**BIST Start.** Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition, and Elasticity Buffer overflow/underflow conditions.
110	6	**Running Disparity Error.** The character on the output bus is a C4.7, C1.7, or C2.7.		**BIST Error.** While comparing characters, a mismatch was found in one or more of the decoded character bits.
111	3	**RESERVED**		**BIST Wait.** The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

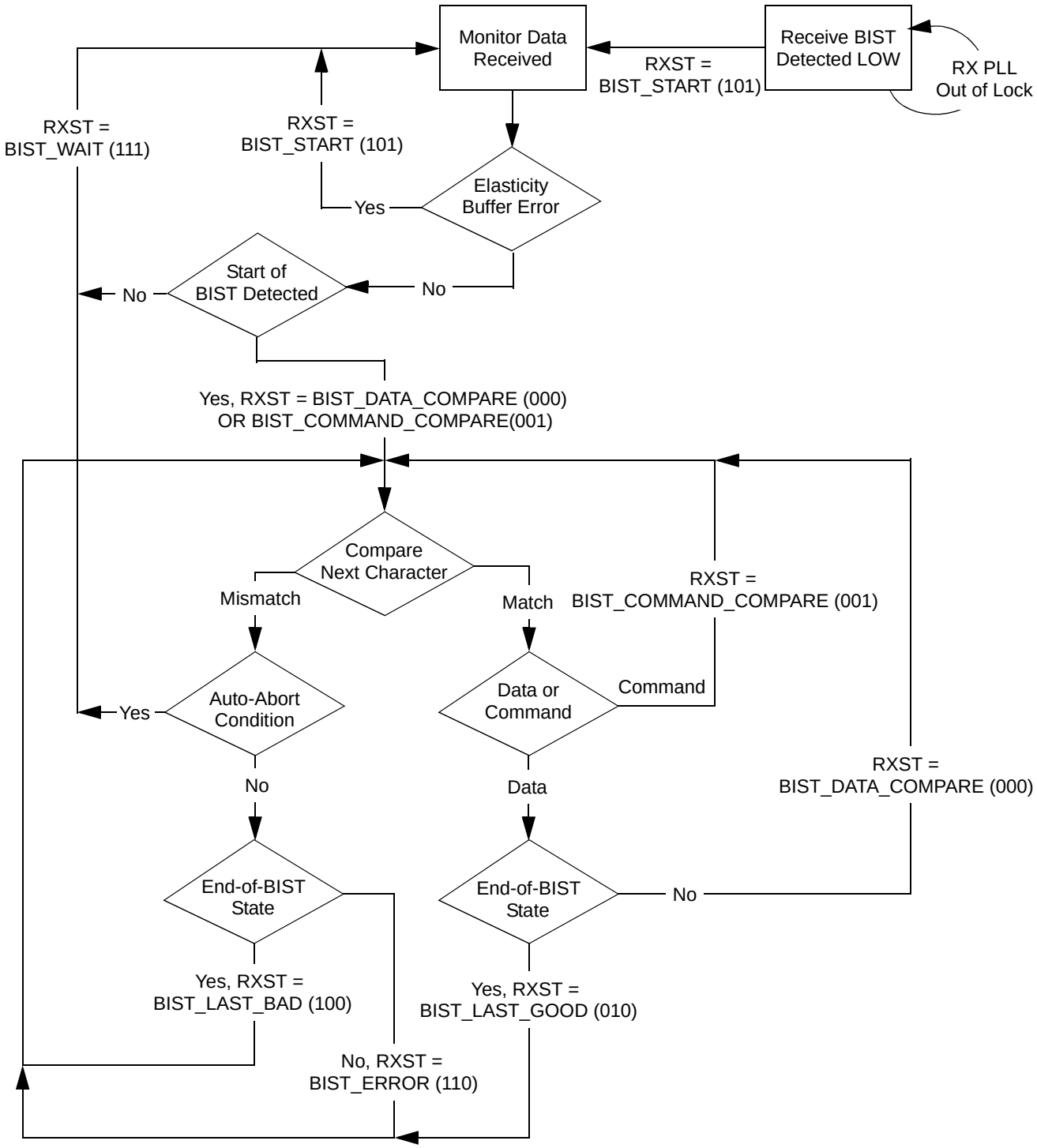


Figure 2. Receive BIST State Machine

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW)..... 60 mA

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

Static Discharge Voltage ..... > 2000 V (per MIL-STD-883, Method 3015)

Latch-Up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ± 5%
Industrial	–40°C to +85°C	+3.3V ± 5%

CYP15G0101DXA DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL Compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, V_{CC} = Min.	2.4	V_{CC}	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V [11]	–50	–15	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL Compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF} [12]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	V_{CC} / 2	V
V_{COMREF} [13]	Common Mode Range		1.0	V_{CC} – 1.2	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID current	V_{IN} = V_{CC} / 2	–50	50	µA
I_{ILL}	Input LOW current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: OUT1±, OUT2±					
V_{OHC}	Output HIGH Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
V_{OLC}	Output LOW Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V

Notes:

11. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
12. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
13. The common mode range defines the allowable range of REFCLK+ and REFCLK– when REFCLK+ = REFCLK–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

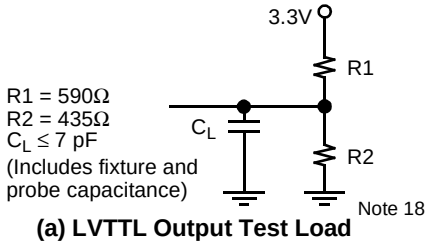
CYP15G0101DXA DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load		450	800	mV
		150Ω differential load		560	1000	mV
Differential Serial Line Receiver Inputs: IN1±, IN2±						
V_{DIFFS} [12]	Input Differential Voltage |(IN+) – (IN–)|			100	1200	mV
V_{IHE}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage			V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max.			1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min.		–700		µA
V_{COM} [14]	Common mode Input range	((VCC – 2.0) + 0.05) Min., (Min. V_{CC} – 0.05) Max.		+1.25	+3.1	V
Miscellaneous				**Typ.**	**Max.**	
I_{CC} [15]	Power Supply Current	REFCLK= Max.	Commercial		305	mA
			Industrial		TBD	mA
I_{CC} [16]	Typ Power Supply Current	REFCLK= 125 MHz		260		mA

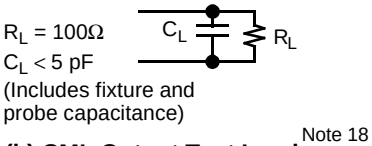
Capacitance[17]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

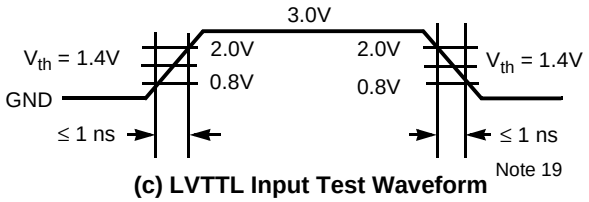
AC Test Loads and Waveforms



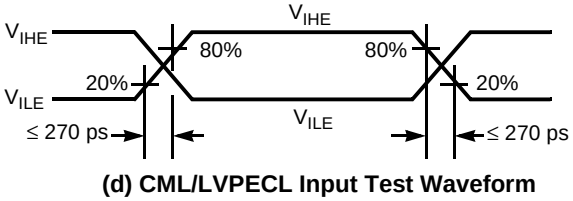
(a) LVTTL Output Test Load



(b) CML Output Test Load



(c) LVTTL Input Test Waveform



(d) CML/LVPECL Input Test Waveform

Notes:

14. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
15. Maximum I_{CC} is measured with V_{CC} = MAX, RFEN = LOW, TA = 25°C, with all Serial Line Drivers enabled, sending a constant alternating 01 pattern, and outputs unloaded.
16. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, TA = 25°C, RFEN = LOW, with one Serial Line Driver sending a continuous alternating 01 pattern and parallel outputs unloaded.
17. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
18. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
19. The LVTTL switching threshold is 1.4V. All timing references are made relative to the point where the signal edges crosses this threshold voltage.

CYP15G0101DXA Transmitter LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max	Unit
f_{TS}	TXCLK Clock Cycle Frequency	20	150	MHz
t_{TXCLK}	TXCLK Period	6.66	50	ns
t_{TXCLKH}[17]	TXCLK HIGH Time	2.2		ns
t_{TXCLKL}[17]	TXCLK LOW Time	2.2		ns
t_{TXCLKR}[17, 20, 21]	TXCLK Rise Time	0.3	1.7	ns
t_{TXCLKF}[17, 20, 21]	TXCLK Fall Time	0.3	1.7	ns
t_{TXDS}	Transmit Data Set-up Time to TXCLK↑ (TXCKSEL ≠ LOW)	1.7		ns
t_{TXDH}	Transmit Data Hold Time from TXCLK↑ (TXCKSEL ≠ LOW)	0.8		ns
f_{TOS}	TXCLKO Clock Cycle Frequency (= 1x or 2x REFCLK Frequency)	20	150	MHz
t_{TXCLKO}	TXCLKO Period	6.66	50	ns
$t_{TXCLKOD+}$	TXCLKO+ Duty Cycle with 65% HIGH time	–1.0	+0.0	ns
$t_{TXCLKOD–}$	TXCLKO– Duty Cycle with 35% HIGH time	–0.0	+1.0	ns

CYP15G0101DXA Receiver LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{RS}	RXCLK Clock Output Frequency	10	150	MHz
t_{RXCLKP}	RXCLK Period	6.66	100	ns
t_{RXCLKH}	RXCLK HIGH Time (RXRATE = LOW)	2.33[17]	26.5	ns
	RXCLK HIGH Time (RXRATE = HIGH)	5.20	51	ns
t_{RXCLKL}	RXCLK LOW Time (RXRATE = LOW)	2.33[17]	26	ns
	RXCLK LOW Time (RXRATE = HIGH)	5.66	51	ns
t_{RXCLKD}	RXCLK Duty Cycle centered at 50%	–1.0	+1.0	ns
t_{RXCLKR}[17]	RXCLK Rise Time	0.3	1.2	ns
t_{RXCLKF}[17]	RXCLK Fall Time	0.3	1.2	ns
$t_{RXDV–}$[22]	Status and Data Valid Time From RXCLK (RXCKSEL = MID)	5UI – 1.5		ns
	Status and Data Valid Time From RXCLK (HALF RATE RECOVERED CLOCK)	–1.5		ns
t_{RXDV+}[22]	Status and Data Invalid Time From RXCLK (RXCKSEL = MID)	5UI – 1.8		ns
	Status and Data Invalid Time From RXCLKx (HALF RATE RECOVERED CLOCK)	–1.5		ns

Notes:
20. The ratio of rise time to falling time must not vary by greater than 2:1.
21. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
22. Parallel data output specifications are only valid if all inputs or outputs are loaded with similar DC and AC loads.

CYP15G0101DXA REFCLK Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{REF}	REFCLK Clock Frequency	20	150	MHz
t_{REFCLK}	REFCLK Period	6.6	50	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = HIGH)	5.9		ns
	REFCLK HIGH Time (TXRATE = LOW)	2.9[17]		ns
t_{REFL}	REFCLK LOW Time (TXRATE = HIGH)	5.9		ns
	REFCLK LOW Time (TXRATE = LOW)	2.9[17]		ns
t_{REFD}[23]	REFCLK Duty Cycle	30	70	%
t_{REFR}[17, 20, 21]	REFCLK Rise Time (20%-80%)		2	ns
t_{REFF}[17, 20, 21]	REFCLK Fall Time (20%-80%)		2	ns
t_{TREFDS}	Transmit Data or $\overline{TXRST}$ Set-up Time to REFCLK (TXCKSEL = LOW)	1.7		ns
t_{TREFDH}	Transmit Data or $\overline{TXRST}$ Hold Time from REFCLK (TXCKSEL = LOW)	0.8		ns
t_{RREFDA}	Receive Data Access Time from REFCLK (RXCKSEL = LOW)		9.5	ns
t_{RREFDV}	Receive Data Valid Time from REFCLK (RXCKSEL = LOW)	4.0		ns
$t_{RREFADV-}$	Receive Data Access Time from RXCLK (RXCKSEL = LOW)	10UI – 4.7		ns
$t_{RREFADV+}$	Receive Data Valid Time from RXCLK (RXCKSEL = LOW)	1.0		ns
$t_{RREFCDV-}$	Receive Data Access Time from RXCLK (RXCKSEL = LOW)	10UI – 4.3		ns
$t_{RREFCDV+}$	Receive Data Valid Time from RXCLK (RXCKSEL = LOW)	0.2		ns
t_{REFRX}	REFCLK Frequency Referenced to Received Clock Period[24]	–0.02	+0.02	%

CYP15G0101DXA Transmit Serial Outputs and TX PLL Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		5000	660	ps
t_{RISE}[17]	CML Output Rise Time 20%-80% (CML Test Load)	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	200	1000	ps
t_{FALL}[17]	CML Output Fall Time 80%-20% (CML Test Load)	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	200	1000	ps
t_{DJ}[17, 25, 27]	Deterministic Jitter (peak-peak)	0.2–1.5 Gbps		TBD	UI
t_{RJ}[17, 26, 27]	Random Jitter (σ)	0.2–1.5 Gbps		TBD	ps
t_{TXLOCK}	Transmit PLL Lock to REFCLK		TBD	TBD	ns

Notes:

23. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLK duty cycle cannot be as large as 30%-70%,
24. REFCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±200 PPM (±0.02%) of the transmitter PLL reference (REFCLK) frequency, necessitating a ±100-PPM crystal.
25. While sending continuous K28.5s, outputs loaded to a balanced 100Ω load, measured at the crosspoint of the differential outputs over the operating range.
26. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.
27. Total jitter is calculated at an assumed BER of 1E –12. Hence: Total Jitter (t_J) = (t_{RJ} * 14) + t_{DJ}.

CYP15G0101DXA Receive Serial Inputs and CDR PLL Characteristics Over the Operating Range

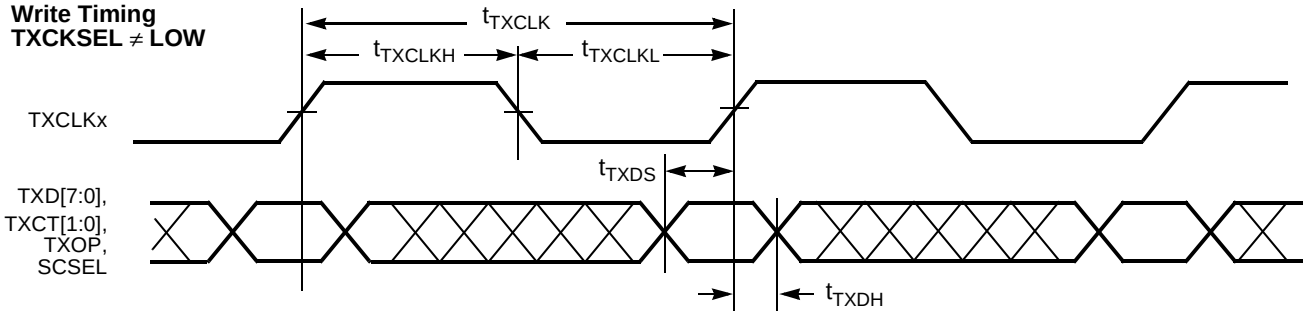
Parameter	Description	Min.	Max.	Unit
t_{RXLOCK}	Receive PLL lock to input data stream (cold start)		10	ms
	Receive PLL lock to input data stream		2500	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate	TBD	TBD	ns
t_{SA}	Static Alignment[17, 28]	TBD	TBD	ps
t_{jtol}	Jitter Tolerance[17, 29, 30, 31]	TBD	TBD	UI

Notes:

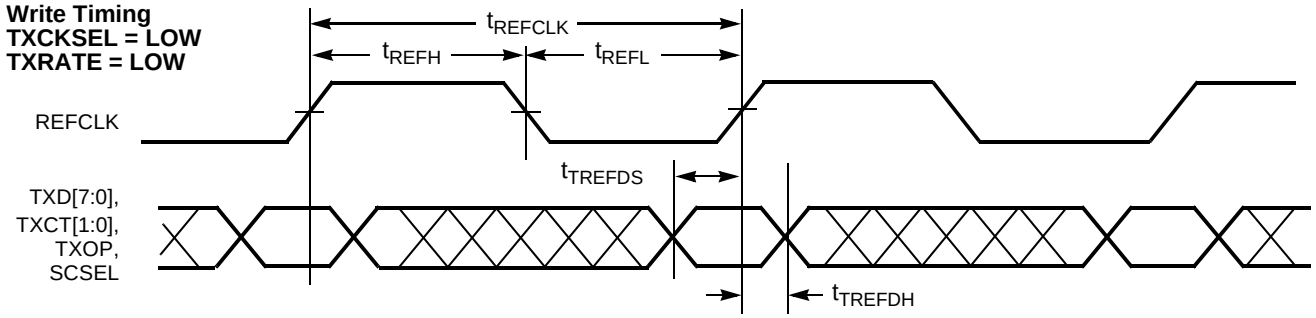
28. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a character error occurs.
29. Receiver UI (Unit Interval) is calculated as $1/(f_{REF} * 20)$ (when RXRATE = HIGH) or $1/(f_{REF} * 10)$ (when RXRATE = LOW) if no data is being received, or $1/(f_{REF} * 20)$ (when RXRATE = HIGH) or $1/(f_{REF} * 10)$ (when RXRATE = LOW) of the remote transmitter if data is being received. In an operating link this is equivalent to t_B.
30. All measurements were done using a CJTPAT.
31. Measured at a datarate of 1.25Gbps.

CYP15G0101DXA HOTLink II Transmitter Switching Waveforms

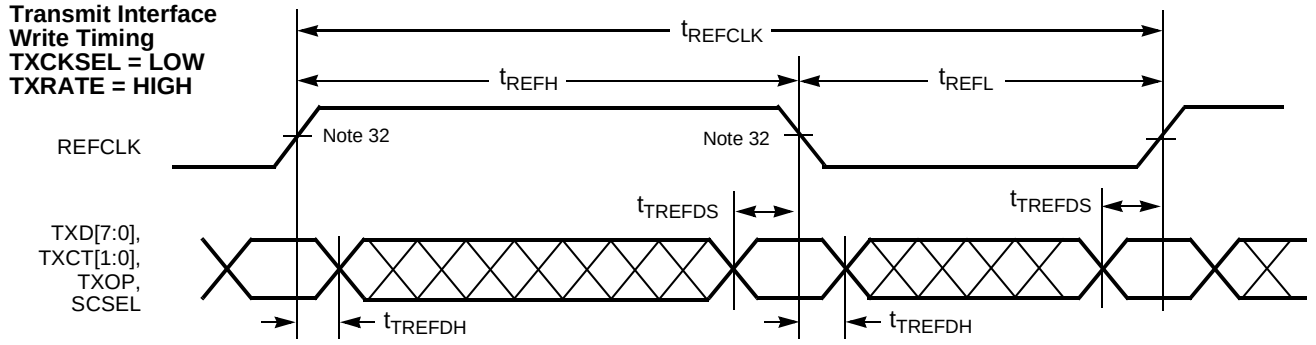
Transmit Interface Write Timing TXCKSEL ≠ LOW



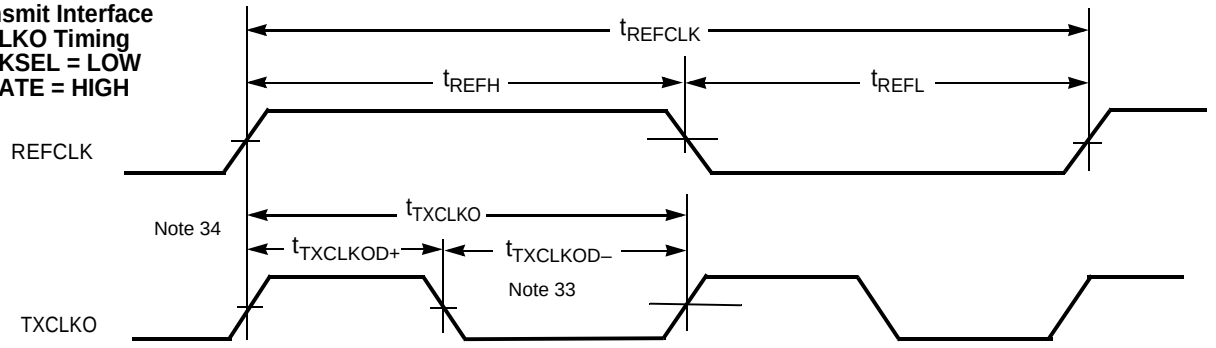
Transmit Interface Write Timing TXCKSEL = LOW TXRATE = LOW



Transmit Interface Write Timing TXCKSEL = LOW TXRATE = HIGH



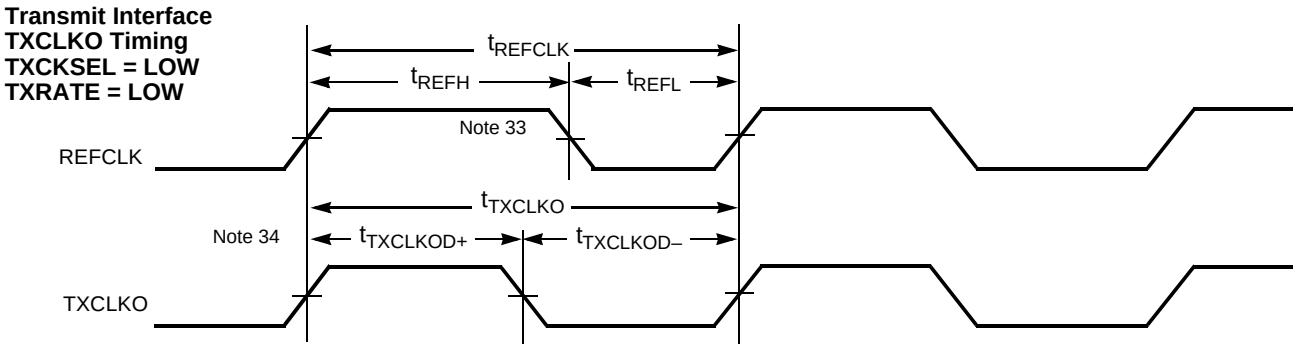
Transmit Interface TXCLKO Timing TXCKSEL = LOW TXRATE = HIGH



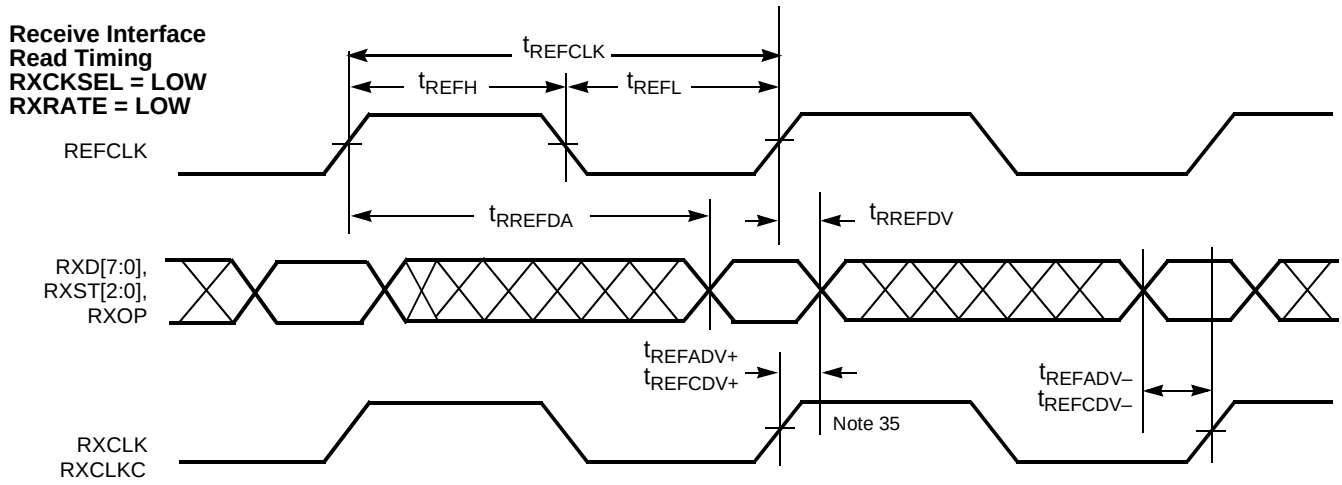
Note:

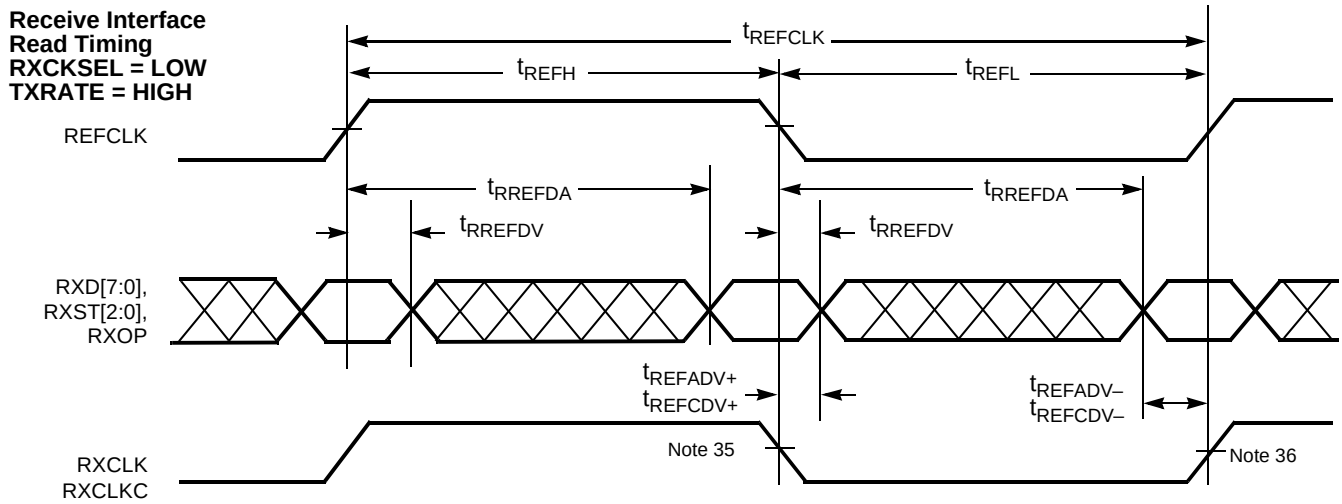
32. When REFCLK is configured for half-rate operation (TXRATE = HIGH) and data is captured using REFCLK instead of TXCLK clock (TXCKSEL = LOW), data is captured using both the rising and falling edges of REFCLK.
33. The TXCLKO output remains at the character rate regardless of the state of TXRATE and does not follow the duty cycle of REFCLK.
34. The rising edge of TXCLKO output has no direct phase relationship to the REFCLK input.

CYP15G0101DXA HOTLink II Transmitter Switching Waveforms (continued)



Switching Waveforms for the CYP15G0101DXA HOTLink II Receiver



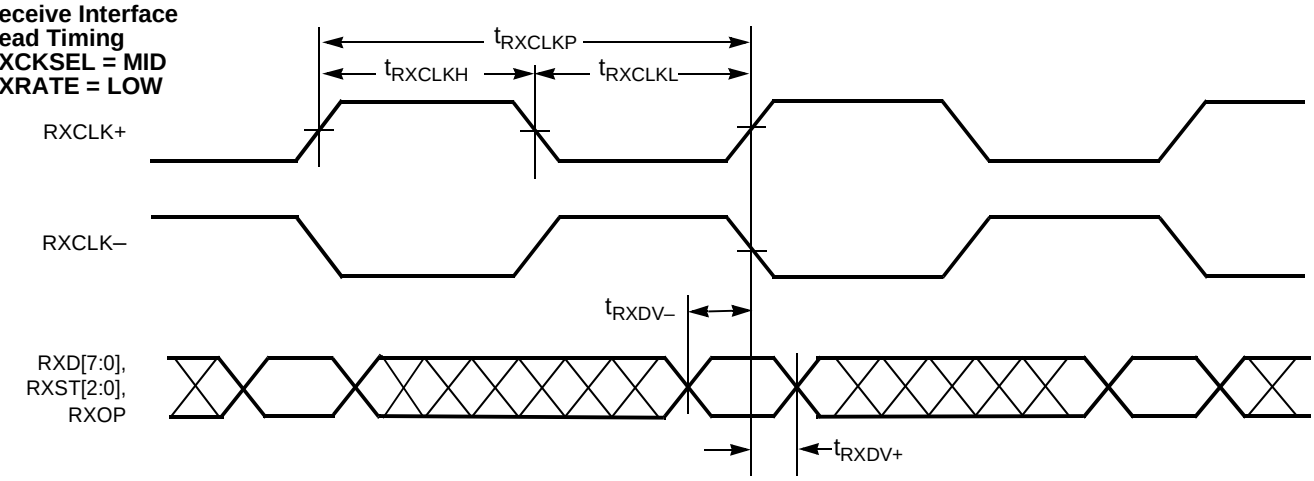


Note:

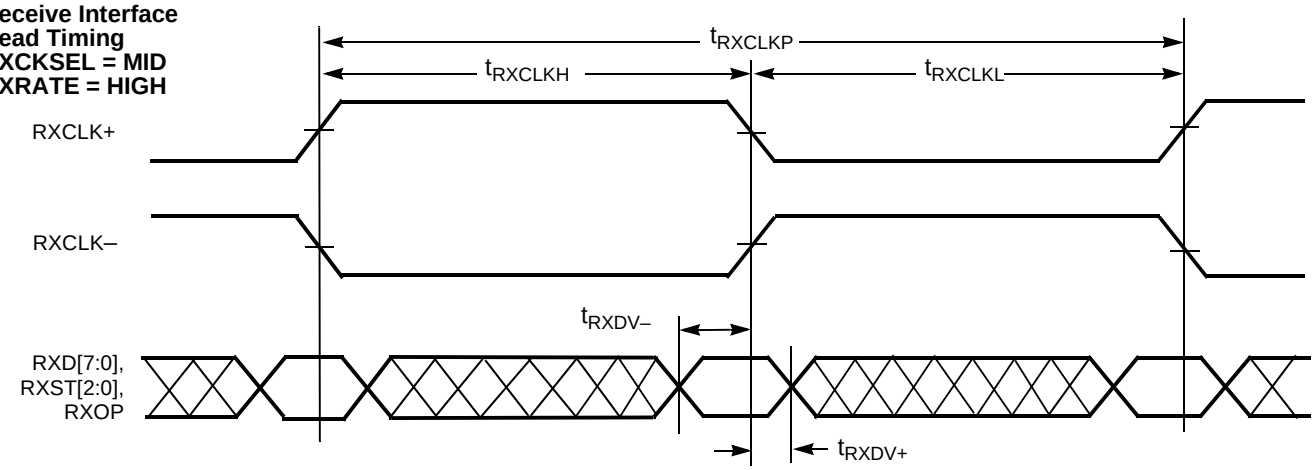
35. RXCLK and RXCLKC are a delayed in phase from REFCLK, and are different in phase from each other.
36. When operated with a half-rate REFCLK, the setup and hold specifications for data relative to RXCLK and RXCLKC are relative to both rising and falling edges of the clock output

Switching Waveforms for the CYP15G0101DXA HOTLink II Receiver (continued)

Receive Interface Read Timing RXCKSEL = MID RXRATE = LOW



Receive Interface Read Timing RXCKSEL = MID RXRATE = HIGH



Static Alignment

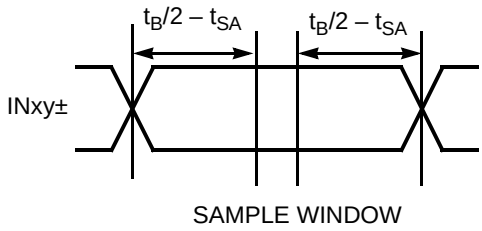


Table 18. Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A1	VCC	POWER	D5	GND	GROUND	G9	TXCLKO+	LVTTL OUT
A2	IN2+	CML IN	D6	GND	GROUND	G10	TXCLKO–	LVTTL OUT
A3	VCC	POWER	D7	GND	GROUND	H1	RXD[0]	LVTTL OUT
A4	OUT2–	CML OUT	D8	TMS	LVTTL IN PU	H2	RXD[2]	LVTTL OUT
A5	RXMODE	3-LEVEL SEL	D9	TRSTZ	LVTTL IN PU	H3	RXD[6]	LVTTL OUT
A6	TXMODE[1]	3-LEVEL SEL	D10	TDI	LVTTL IN PU	H4	$\overline{\text{LFI}}$	LVTTL OUT
A7	IN1+	CML IN	E1	BISTLE	LVTTL IN PU	H5	TXCT[1]	LVTTL IN
A8	VCC	POWER	E2	DECMODE	3-LEVEL SEL	H6	TXD[6]	LVTTL IN
A9	OUT1–	CML OUT	E3	OELE	LVTTL IN PU	H7	TXD[3]	LVTTL IN
A10	VCC	POWER	E4	GND	GROUND	H8	TXCLK	LVTTL IN PD
B1	VCC	POWER	E5	GND	GROUND	H9	$\overline{\text{TXRST}}$	LVTTL IN PU
B2	IN2–	CML IN	E6	GND	GROUND	H10	#NC	NO CONNECT
B3	TDO	LVTTL 3-S OUT	E7	GND	GROUND	J1	VCC	POWER
B4	OUT2+	CML OUT	E8	TCLK	LVTTL IN PD	J2	RXD[3]	LVTTL OUT
B5	TXRATE	LVTTL IN PD	E9	RXCKSEL	3-LEVEL SEL	J3	RXD[7]	LVTTL OUT
B6	TXMODE[0]	3-LEVEL SEL	E10	TXCKSEL	3-LEVEL SEL	J4	RXCLK–	LVTTL OUT
B7	IN1–	CML IN	F1	RXST[2]	LVTTL OUT	J5	TXCT[0]	LVTTL IN
B8	#NC	NO CONNECT	F2	RXST[1]	LVTTL OUT	J6	TXD[5]	LVTTL IN
B9	OUT1+	CML OUT	F3	RXST[0]	LVTTL OUT	J7	TXD[2]	LVTTL IN
B10	VCC	POWER	F4	GND	GROUND	J8	TXD[0]	LVTTL IN
C1	RFEN	LVTTL IN PD	F5	GND	GROUND	J9	#NC	NO CONNECT
C2	LPEN	LVTTL IN PD	F6	GND	GROUND	J10	VCC	POWER
C3	RXLE	LVTTL IN PU	F7	GND	GROUND	K1	VCC	POWER
C4	RXCLKC+	LVTTL OUT	F8	TXPER	LVTTL OUT	K2	RXD[4]	LVTTL OUT
C5	RXRATE	LVTTL IN PD	F9	REFCLK–	PECL IN	K3	VCC	POWER
C6	SDASEL	3-LEVEL SEL	F10	REFCLK+	PECL IN	K4	RXCLK+	LVTTL OUT
C7	SPDSEL	3-LEVEL SEL	G1	RXOP	LVTTL 3-S OUT	K5	TXD[7]	LVTTL IN
C8	PARCTL	3-LEVEL SEL	G2	RXD[1]	LVTTL OUT	K6	TXD[4]	LVTTL IN
C9	RFMODE	3-LEVEL SEL	G3	RXD[5]	LVTTL OUT	K7	TXD[1]	LVTTL IN
C10	INSEL	LVTTL IN	G4	GND	GROUND	K8	VCC	POWER
D1	BOE[0]	LVTTL IN PU	G5	GND	GROUND	K9	SCSEL	LVTTL IN PD
D2	BOE[1]	LVTTL IN PU	G6	GND	GROUND	K10	VCC	POWER
D3	FRAMCHAR	3-LEVEL SEL	G7	GND	GROUND			
D4	GND	GROUND	G8	TXOP	LVTTL IN PU			

NOTE: #NC = **DO NOT CONNECT**

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data characters are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard contain a distinct and easily recognizable bit pattern that assists the receiver in achieving character alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character.

```
FC-2  45H
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation, note that the order of bits has been reversed):

```
Data Byte Name  D5.2
                Bits: ABCDE FGH
                      10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
                Bits: abcdei fghj
                      101001 0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and SC/D = LOW) or a Special Character (c is set to K, and SC/D = HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

NOTE: This definition of the 10-bit Transmission Code is based on the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code” IBM Journal of Research and Development, 27, No. 5: 440-451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. “Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code” (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANS X3.230-1994 ANSI FC-PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22-7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within any higher-level constructs specified by a standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit “a” is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order.

Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters and checking the validity of received Transmission Characters. In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two Transmission Characters. The two columns correspond to the current value of the running disparity. Running disparity is a binary parameter with either a negative (–) or positive (+) value.

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter calculates a new value for its running disparity based on the contents of the transmitted character. Special Character

codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character is calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in the table is found for the Valid Data byte or the Special Character byte for which a Transmission Character is to be generated (encoded). The current value of the Transmitter's running disparity is used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity is calculated. This new value is used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 19* shows naming notations and examples of valid transmission characters.

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character.

Table 19. Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	00101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 20* shows an example of this behavior.

Table 20. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Table 21. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001

Table 21. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100

Table 21. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010

Table 21. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 22. Valid Special Character Codes and Sequences (TXCTx = special character code or RXSTx[2:0] = 001)[37, 38]

S.C. Code Name	S.C. Byte Name			S.C. Byte Name			Current RD– abcdei fghj	Current RD+ abcdei fghj
	Cypress			Alternate				
	S.C. Byte Name[39]		Bits HGF EDCBA	S.C. Byte Name[39]		Bits HGF EDCBA		
K28.0	C0.0	(C00)	000 00000	C28.0	(C1C)	000 11100	001111 0100	110000 1011
K28.1[40]	C1.0	(C01)	000 00001	C28.1	(C3C)	001 11100	001111 1001	110000 0110
K28.2[40]	C2.0	(C02)	000 00010	C28.2	(C5C)	010 11100	001111 0101	110000 1010
K28.3	C3.0	(C03)	000 00011	C28.3	(C7C)	011 11100	001111 0011	110000 1100
K28.4[40]	C4.0	(C04)	000 00100	C28.4	(C9C)	100 11100	001111 0010	110000 1101
K28.5[40, 41]	C5.0	(C05)	000 00101	C28.5	(CBC)	101 11100	001111 1010	110000 0101
K28.6[40]	C6.0	(C06)	000 00110	C28.6	(CDC)	110 11100	001111 0110	110000 1001
K28.7[40, 42]	C7.0	(C07)	000 00111	C28.7	(CFC)	111 11100	001111 1000	110000 0111
K23.7	C8.0	(C08)	000 01000	C23.7	(CF7)	111 10111	111010 1000	000101 0111
K27.7	C9.0	(C09)	000 01001	C27.7	(CFB)	111 11011	110110 1000	001001 0111
K29.7	C10.0	(C0A)	000 01010	C29.7	(CFD)	111 11101	101110 1000	010001 0111
K30.7	C11.0	(C0B)	000 01011	C30.7	(CFE)	111 11110	011110 1000	100001 0111
End of Frame Sequence								
EOFxx[43]	C2.1	(C22)	001 00010	C2.1	(C22)	001 00010	–K28.5,Dn.xxx0	+K28.5,Dn.xxx1
Code Rule Violation and SVS Tx Pattern								
Exception[42, 44]	C0.7	(CE0)	111 00000	C0.7	(CE0)	111 00000[48]	100111 1000	011000 0111
–K28.5[45]	C1.7	(CE1)	111 00001	C1.7	(CE1)	111 00001[48]	001111 1010	001111 1010
+K28.5[46]	C2.7	(CE2)	111 00010	C2.7	(CE2)	111 00010[48]	110000 0101	110000 0101
Running Disparity Violation Pattern								
Exception[47]	C4.7	(CE4)	111 00100	C4.7	(CE4)	111 00100 [48]	110111 0101	001000 1010

Notes:

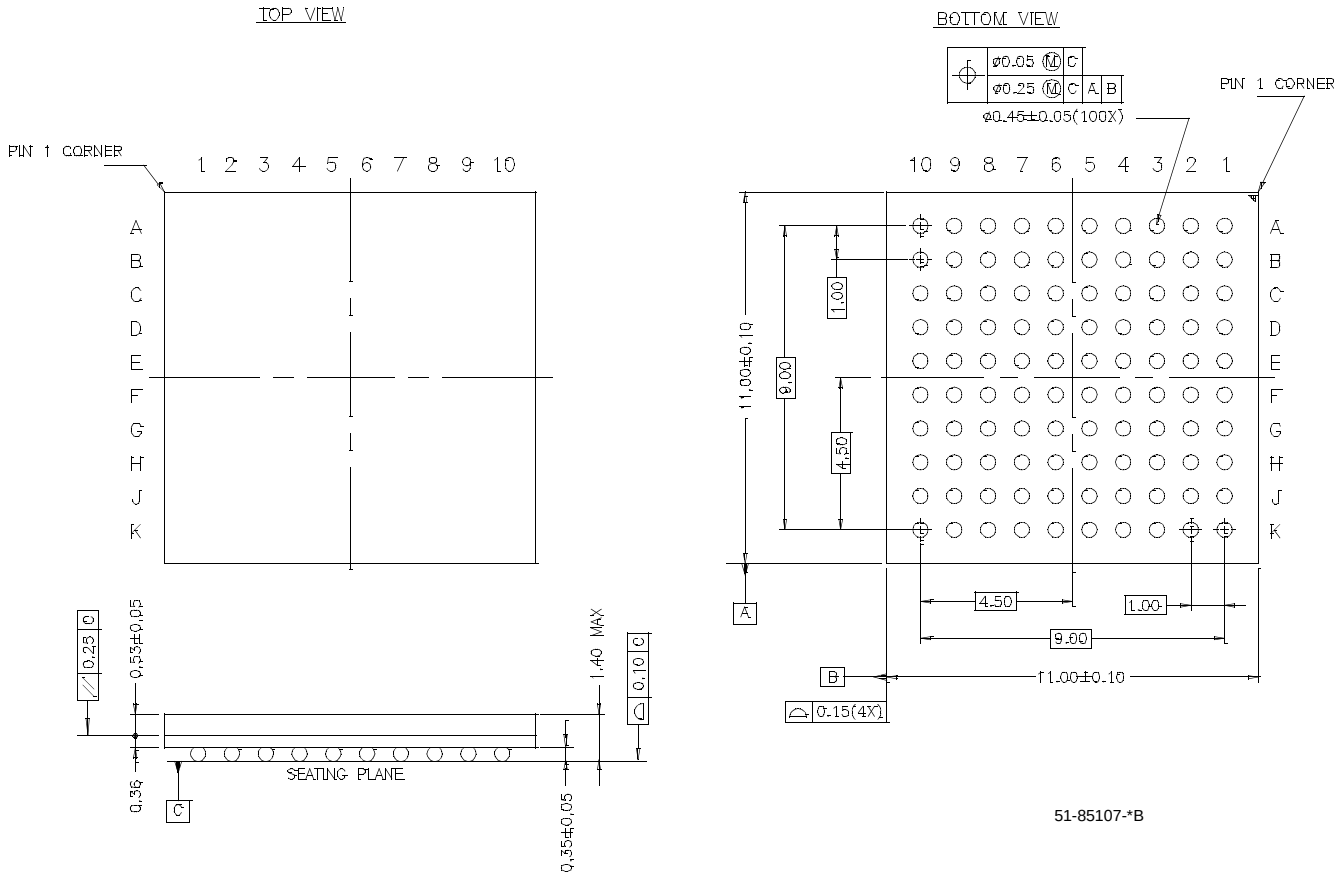
37. All codes not shown are reserved.
38. Notation for Special Character Code Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn = the specified value between 00 and FF).
39. Both the Cypress and alternate encodings may be used for data transmission to generate specific Special Character Codes. The decoding process for received characters generates Cypress codes or Alternate codes as selected by the DECMODE configuration input.
40. These characters are used for control of ESCON interfaces. They can be sent as embedded commands or other markers when not operating using ESCON protocols.
41. The K28.5 character is used for framing operations by the receiver. It is also the pad or fill character transmitted to maintain the serial link when no user data is available.
42. Care must be taken when using this Special Character code. When a C7.0 is followed by a D11.x or D20.x, or when an SVS (C0.7) is followed by a D11.x, an alias K28.5 sync character is created. These sequences can cause erroneous framing and should be avoided while RFEN = HIGH.
43. C2.1 = Transmit either –K28.5+ or +K28.5– as determined by Current RD and modify the Transmission Character that follows, by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (–) the LSB becomes 1. This modification allows construction of X3.230 “EOF” frame delimiters wherein the second data byte is determined by the Current RD.
For example, to send “EOFdt” the controller could issue the sequence C2.1–D21.4– D21.4–D21.4, and the HOTLink Transmitter will send either K28.5–D21.4– D21.4–D21.4 or K28.5–D21.5– D21.4–D21.4 based on Current RD. Likewise to send “EOFdti” the controller could issue the sequence C2.1–D10.4–D21.4– D21.4, and the HOTLink Transmitter will send either K28.5–D10.4–D21.4– D21.4 or K28.5–D10.5–D21.4– D21.4 based on Current RD. The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.
44. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. The receiver will only output this Special Character if the Transmission Character being decoded is not found in the tables.
45. C1.7 = Transmit Negative K28.5 (–K28.5+) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if –K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.
46. C2.7 = Transmit Positive K28.5 (+K28.5–) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD–, otherwise K28.5 is decoded as C5.0 or C1.7.
47. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation. The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This might indicate that an error occurred in a prior byte.
48. Supported only for data transmission. The receive status for these conditions will be reported by specific combinations of receive status bits.

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP15G0101DXA-BBC	BB100	100-Ball Grid Array	Commercial
Standard	CYP15G0101DXA-BBI	BB100	100-Ball Grid Array	Industrial

Package Diagram

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



Revision History

Document Title: CYP15G0101DXA Single Channel HOTLink II™ Transceiver (Preliminary) Document Number: 38-02061				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	117226	08/21/02	AMV	New Data Sheet