

April 1983 Revised October 2000

74F564

Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 74F564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable $\overline{(\text{OE})}$. The information presented to the D inputs is sorted in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 74F574, but has inverted outputs.

Features

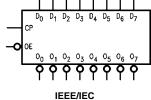
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74F574
- 3-STATE outputs for bus-oriented applications

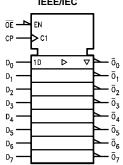
Ordering Code:

Order Number	Package Number	Package Description				
74F564SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide				
74F564PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide				

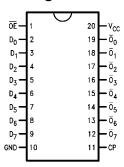
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols





Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I _{IH} /I _{IL}	
	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
D ₀ -D ₇	Data Inputs	1.0/1.0	20 μA/–0.6 mA	
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/–0.6 mA	
OE	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA	
$\overline{O}_0 - \overline{O}_7$	3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)	

Functional Description

The 74F564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable $(\overline{\text{OE}})$ LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops.

Function Table

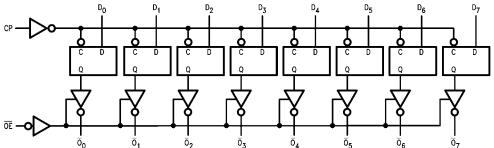
Inputs			Internal	Outputs	Function		
OE	СР	D	Q	0	Function		
Н	Н	L	NC	Z	Hold		
Н	Н	Н	NC	Z	Hold		
Н	~	L	Н	Z	Load		
Н	~	Н	L	Z	Load		
L	~	L	Н	Н	Data Available		
L	~	Н	L	L	Data Available		
L	Н	L	NC	NC	No Change in Data		
L	Н	Н	NC	NC	No Change in Data		

- H = HIGH Voltage Level L = LOW Voltage Level
- Z = High Impedance

 = LOW-to-HIGH Transition

 NC = No Change
- X = Immaterial NC = No Chang

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

-65°C to +150°C Storage Temperature Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias $-55^{\circ}C$ to $+150^{\circ}C$ V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V-0.5V to +7.0V

Input Voltage (Note 2) Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC}

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Parameter M		Min Typ		Max	Units	v _{cc}	Conditions		
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal				
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal				
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA				
V _{OH}	Output HIGH 10% V _{CC}		2.5				I _{OH} = -1 mA					
	Voltage	10% V _{CC}	2.4			V	Min	$I_{OH} = -3 \text{ mA}$				
		$5\% V_{CC}$	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$				
		5% V _{CC}	2.7					$I_{OH} = -3 \text{ mA}$				
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 24 mA				
I _{IH}	Input HIGH Current				5.0	μА	Max	V _{IN} = 2.7V				
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V				
I _{CEX}	Output HIGH Leakage Current				50	μА	Max	V _{OUT} = V _{CC}				
V _{ID}	Input Leakage Test		4.75			٧	0.0	I _{ID} = 1.9 μA All Other Pins Grounded				
I _{OD}	Output Leakage Circuit Current				3.75	μА	0.0	V _{IOD} = 150 mV All Other Pins Grounded				
I _{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$				
I _{OZH}	Output Leakage Current				50	μΑ	Max	V _{OUT} = 2.7V				
l _{OZL}	Output Leakage Current				-50	μΑ	Max	V _{OUT} = 0.5V				
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V				
I _{ZZ}	Bus Drainage Test				500	μА	0.0V	V _{OUT} = 5.25V				
I _{CCZ}	Power Supply Current			55	86	mA	Max	V _O = HIGH Z				

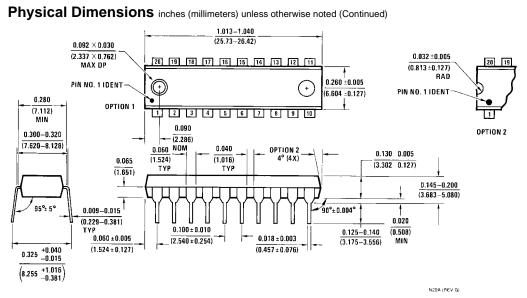
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			T _A = 0°C V _{CC} = C _L =	Units	
		Min	Тур	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100			70		MHz
t _{PLH}	Propagation Delay	2.5	5.2	8.5	2.5	8.5	
t _{PHL}	CP to \overline{O}_n	2.5	5.9	8.5	2.5	8.5	ns
t _{PZH}	Output Enable Time	3.0	5.6	9.0	2.5	10.0	
t _{PZL}		3.0	6.2	9.0	2.5	10.0	ns
t _{PHZ}	Output Disable Time	1.5	3.4	5.5	1.5	6.5	115
t_{PLZ}		1.5	2.7	5.5	1.5	6.5	

AC Operating Requirements

Symbol	Parameter		+25°C +5.0V	$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$		Units
- Cymbei	, a.a		Max	Min	Max	O.I.I.S
t _S (H)	Setup Time, HIGH or LOW	2.0		2.0		
t _S (L)	D _n to CP	2.5		2.5		ns
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		115
t _H (L)	D _n to CP	2.0		2.0		
t _W (H)	CP Pulse Width	5.0		5.0		ns
t _W (L)	HIGH or LOW	5.0		5.0		115

Physical Dimensions inches (millimeters) unless otherwise noted 12.6±0.10 -A-5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT.-0.6 TYP 1.27 TYP LAND PATTERN RECOMMENDATION ALL LEAD TIPS SEE DETAIL A 0.1 C 2.1 MAX. 1.8±0.1 0.15-0.25 0.15±0.05 1.27 TYP DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES: A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60±0.15 SEATING PLANE 1.25 -M20DRevB1 DETAIL A 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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