# VLSI TECHNOLOGY, INC.

FEATURES

- High-speed access and cycle times: 35 and 45 ns (max)
- 1.2 μ CMOS process
- Fully static operation
- Chip enable input, automatic power-down when disabled
- CMOS process for low power
  — 300 mW (typical) active
  — 100 μW (typical) standby
  — 10 μW (typical) CMOS standby
- Single 5 V ± 10% power supply
- Fully TTL compatible
- Battery back-up operation (VT6208L)
- 24-lead, 300 mil plastic DIP

DESCRIPTION

The VT6208 and VT6208L are high-speed static RAMs (SRAMs) organized as 65,536 words by four bits. These devices are fabricated using an advanced 1.2 μ CMOS process. They offer high performance 35 and 45 ns access times as well as high reliability and low power.

The VT6208L offers typical standby current of 10 μW, and is ideal in systems where power dissipation is a major consideration. This includes battery-operated systems and systems employing battery back-up. Both the VT6208 and the VT6208L are offered in a 300 mil plastic DIP.

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PIN DIAGRAM
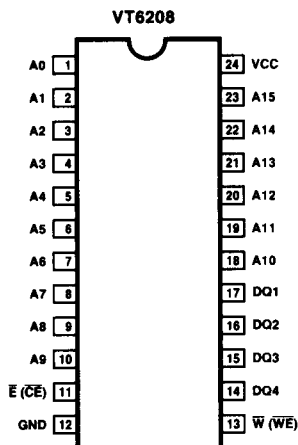
BLOCK DIAGRAM

PIN NAMES

A0–A15	Address Inputs
DQ1–DQ4	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)	Chip Enable
$\overline{W}$ ($\overline{WE}$)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)
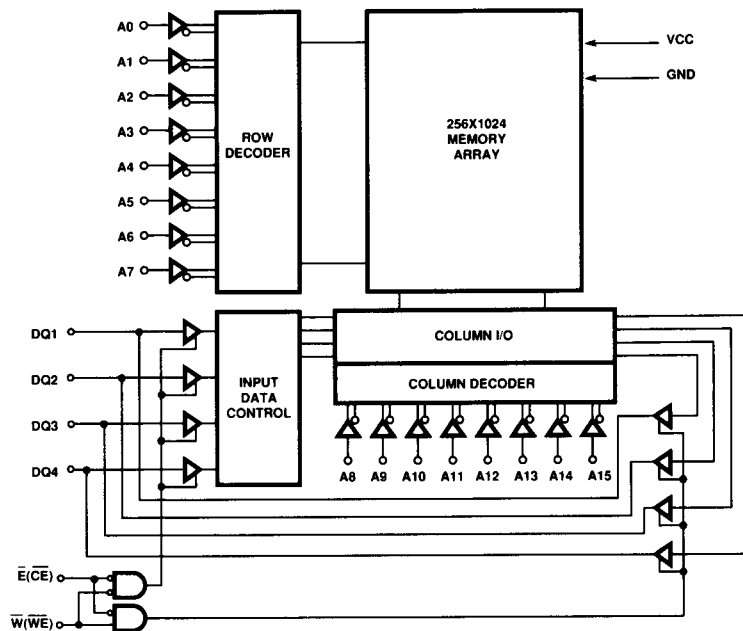
ABSOLUTE MAXIMUM RATINGS

Voltage on VCC
Relative to GND   –0.5 V to +7 V
Voltage on Any Pin
Relative to GND   –0.5 V to VCC +1
Storage
Temperature   –55°C to +125°C
Storage
Temperature
under Bias   –10°C to +85°C
Power Dissipation   1.0 W

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of this device under these or any conditions

above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
VIL	Input LOW Voltage		–0.5		0.8	V	Note 2
VIH	Input HIGH Voltage		2.2		6.0	V	
VOL	Output LOW Voltage				0.4	V	IOL = 8 mA
VOH	Output HIGH Voltage		2.4			V	IOH = –4.0 mA
ILI	Input Leakage Current		–2.0		2.0	µA	VCC = max, VIN = GND to VCC
IOL	Output Leakage Current		–10.0		10.0	µA	$\overline{E}$ = VIH, VI/O = GND to VCC
ICC	VCC Current, Active			60	100	mA	$\overline{E}$ = VIL, outputs are open-load
ISB1	VCC Current, Standby			15	30	mA	$\overline{E}$ = VIH
ISB2	VCC Current, CMOS Standby	VT6208		0.02	2.0	mA	$\overline{E} \geq$ VCC –0.2 V, VIN $\leq$ 0.2 V or VIN $\geq$ VCC –0.2 V
		VT6208L		0.002	0.1	mA	

CAPACITANCE TA = 25°C, f = 1 MHz, Note 3

Symbol	Parameter	Min	Max	Unit	Conditions
CIN	Input Capacitance		6	pF	VIN = 0 V
CI/O	Input/Output Capacitance		10	pF	VI/O = 0 V

AC TEST CONDITIONS

Input Voltage Levels   0 V to 3.0 V
Input Rise and Fall Times   5 ns
Input and Output
Reference Levels   1.5 V
Output Load   Figures 1a and 1b

AC TESTING LOAD CIRCUIT

FIGURE 1a. OUTPUT LOAD CIRCUIT A
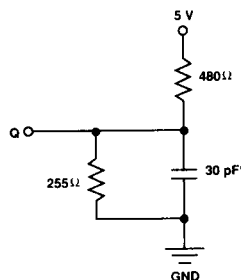
* INCLUDES JIG CAPACITANCE.

FIGURE 1b. OUTPUT LOAD CIRCUIT B, Note 4
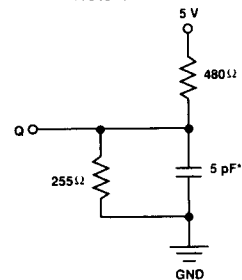
* INCLUDES JIG CAPACITANCE.

Notes:
1. Typical limits are at VCC = 5.0 V, TA = +25°C and specified loading.
2. VIL min = –2.0 V for pulse width ≤ 10 ns.
3. This parameter is sampled and not 100% tested.
4. Transition is measured ±200 mV from steady state voltage with output load Figure 1b. This parameter is sampled and not 100% tested.
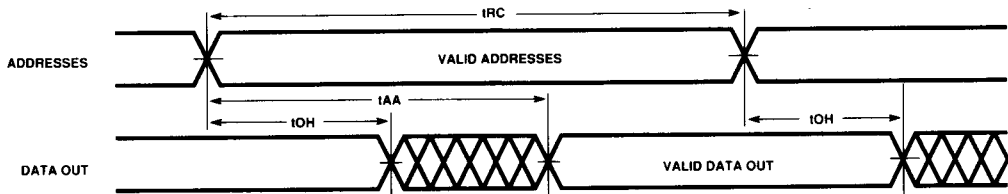
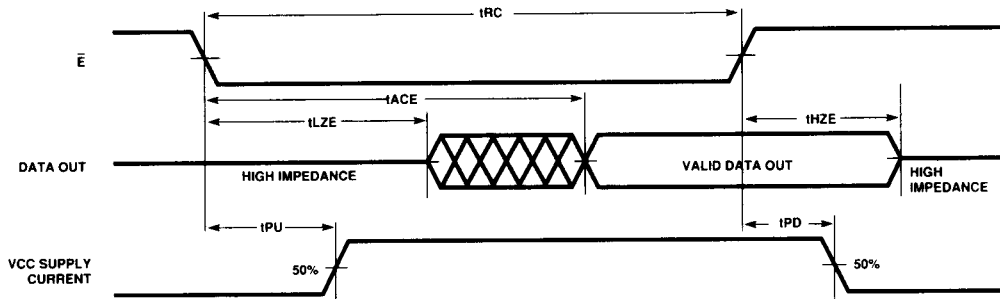## TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

READ CYCLE

Symbol	Parameter	VT6208/6208L-35		VT6208/6208L-45		Unit
		Min	Max	Min	Max	
tRC	Read Cycle Time	35		45		ns
tAA	Address Access Time		35		45	ns
tACE	Chip Enable Access Time		35		45	ns
tOH	Output Hold Time from Address Change	5		5		ns
tLZE	E̅ LOW to Output Low Z (Figure 1b)	5		5		ns
tHZE	E̅ HIGH to Output High Z (Figure 1b)	0	20	0	20	ns
tPU	E̅ LOW to Power-Up	0		0		ns
tPD	E̅ HIGH to Power-Down		30		30	ns

TIMING DIAGRAMS

READ CYCLE NO. 1, Notes 2 and 3


READ CYCLE NO. 2, Notes 2 and 4

Notes:
1. All timing parameters were measured with output load Figure 1a unless otherwise noted.
2. W̅ is HIGH for read cycle.
3. Device is continuously selected, E̅ = VIL.
4. Address valid prior to or coincident with E̅ transition to LOW.

TIMING CHARACTERISTICS TA=0°C to +70°C, VCC=5 V ±10%

WRITE CYCLE

Symbol	Parameter	VT6208/6208L-35		VT6208/6208L-45		Unit
		Min	Max	Min	Max	
tWC	Write Cycle Time	35		45		ns
tEW	$\overline{E}$ LOW to Write End	30		40		ns
tAW	Address Set-Up Time to Write End	30		40		ns
tAS	Address Set-Up to Write Start	0		0		ns
tWP	Write Pulse Width	30		35		ns
tWR	Address Hold Time from Write End (Write Recovery)	3		3		ns
tDS	Data In Set-Up Time to Write End	20		20		ns
tDH	Data In Hold Time after Write End	0		0		ns
tHZW	$\overline{W}$ LOW to Output High Z (Figure 1b)	0	10	0	15	ns
tLZW	$\overline{W}$ HIGH to Output Low Z (Figure 1b)	0		0		ns

TIMING DIAGRAMS

WRITE CYCLE NO. 1 ($\overline{W}$ CONTROLLED)
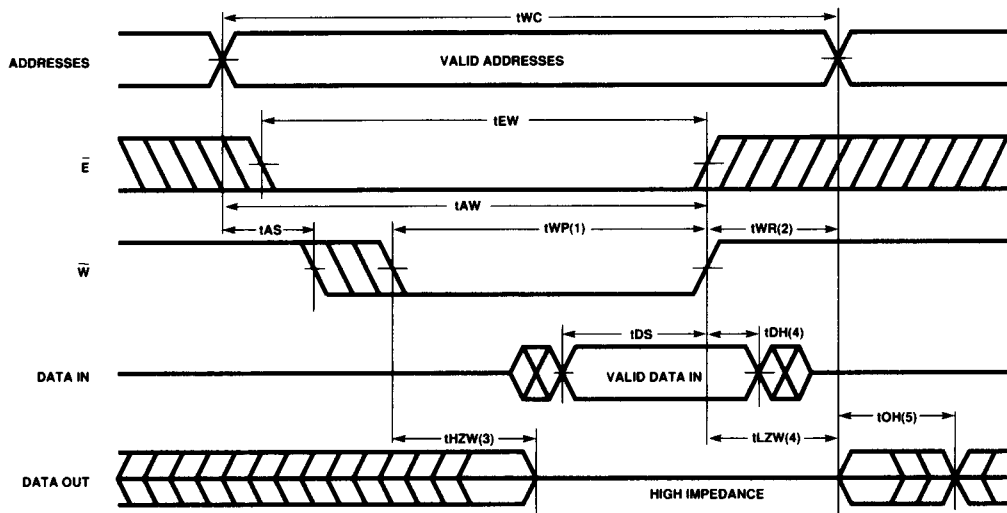
Notes:
1. A write occurs during the overlap (tWP) of a low $\overline{E}$ and a low $\overline{W}$.
2. tWR is measured from the earlier of $\overline{E}$ or $\overline{W}$ going HIGH to end of write cycle.
3. During this period, I/O pins are in the output state, and input signals of opposite phase must not be applied.
4. If $\overline{E}$ is low during this period, I/O pins are in the the output state, and input signals out of phase must not be applied to I/O pins.
5. Dout is in the same phase as written data in this write cycle.

TIMING DIAGRAMS (Cont.)

WRITE CYCLE NO. 2 (E̅ CONTROLLED), Note 3
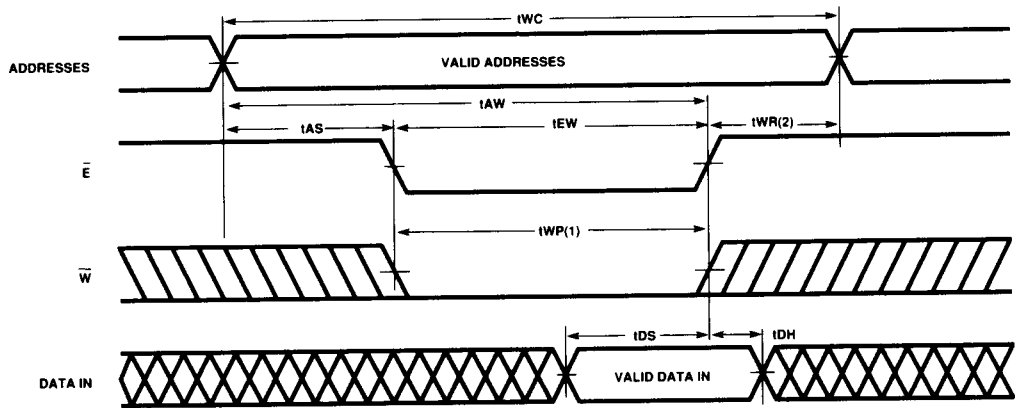
LOW VCC DATA RETENTION CHARACTERISTICS (VT6208L only) TA = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VDR	VCC for Data Retention	2.0			V	E̅ ≥ VCC –0.2 V, VIN ≥ VCC –0.2 V or 0 V ≤ VIN ≤ 0.2 V
ICCDR	Data Retention Current (VCC = 3.0 V)		1	50	μA	
tCDR	Chip Disable to Data Retention Time	0			ns	
tR	Operation Recovery Time	tRC			ns	

LOW VCC DATA RETENTION WAVEFORM (VT6208L only)
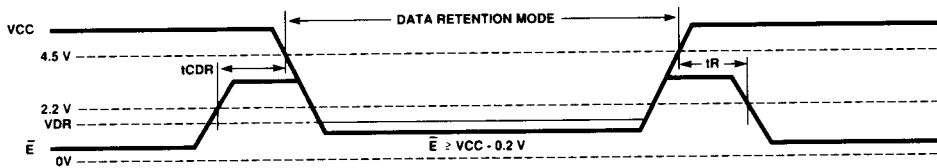
Notes:
1. A write occurs during the overlap (tWP) of a low E̅ and a low W̅.
2. tWR is measured from the earlier of E̅ or W̅ going HIGH to end of write cycle.
3. If the E̅ low transition occurs simultaneously with W̅ low transition or after the W̅ low transition, the outputs remain in a high impedance state.