VT6103

Fast Ethernet
10 / 100
1-Port PHY / Transceiver

Revision 1.1
April 15, 2002

VIA TECHNOLOGIES, INC.

Copyright Notice:

VT6103 may only be used to identify products of VIA Technologies, Inc.

Disclaimer Notice:

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable to the publication date of this document. However, VIA Technologies assumes no responsibility for any errors in this document. Furthermore, VIA Technologies assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

Offices:

USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Web: http://www.viatech.com

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Web: http://www.via.com.tw

REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	4/9/02	Initial Public Release – same as internal release 0.4 except for update of legal page, fix of miscellaneous document formatting errors, update of document title, addition of typical system block diagram, fix of RXER and TXER pin descriptions, update of application schematics, and addition of marking spec	DH
1.1	4/15/02	Revised document title and page headers Fixed Taiwan office fax number on legal page Cleaned up schematics and added as figures	DH

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VT6103

FAST ETHERNET 10 / 100
1-PORT PHY / TRANSCEIVER

PRODUCT FEATURES

- **Single Chip 100Base-TX / 10Base-T Physical Layer Solution**
- **Dual Speed – 100 / 10 Mbps**
- **Half and Full Duplex**
- **MII Interface to Ethernet Controller**
- **MII Interface to Configuration & Status**
- **Optional Repeater Interface**
- **Auto Negotiation: 10 / 100, Full / Half Duplex**
- **Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards**
- **On Chip Wave Shaping – No External Filters Required**
- **Adaptive Equalizer**
- **Baseline Wander Correction**
- **LED Outputs**
  - Link Status
  - Duplex status
  - Speed Status
  - Collision
- **48 Pin SSOP Package**

OVERVIEW

The VT6103 is a Physical Layer device for Ethernet 10Base-T and 100Base-TX using category 5 Unshielded, Type 1 Shielded, and Fiber Optic cables. This VLSI device is designed for easy implementation of 10 / 100 Mb/s Fast Etherent LANs. It interfaces to a MAC through an MII interface ensuring interoperability between products from different vendors.

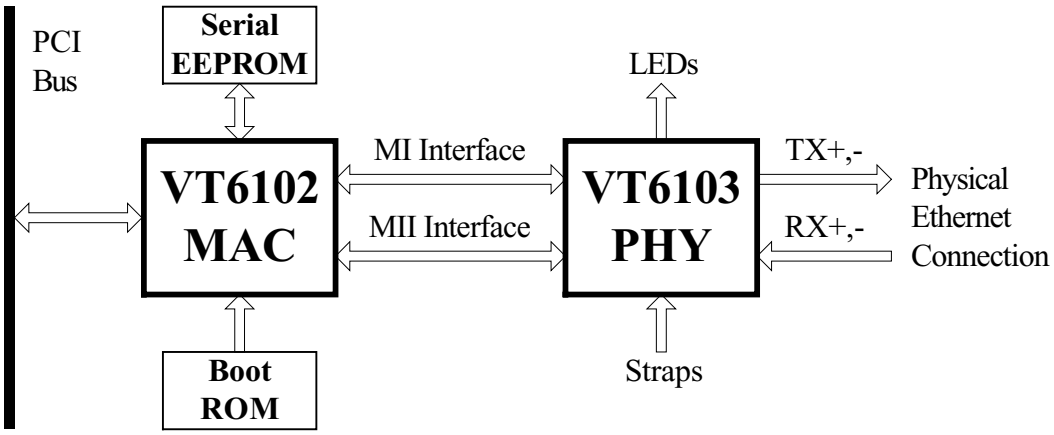


Figure 1. Typical System Block Diagram

PINOUTS

Pin Diagram

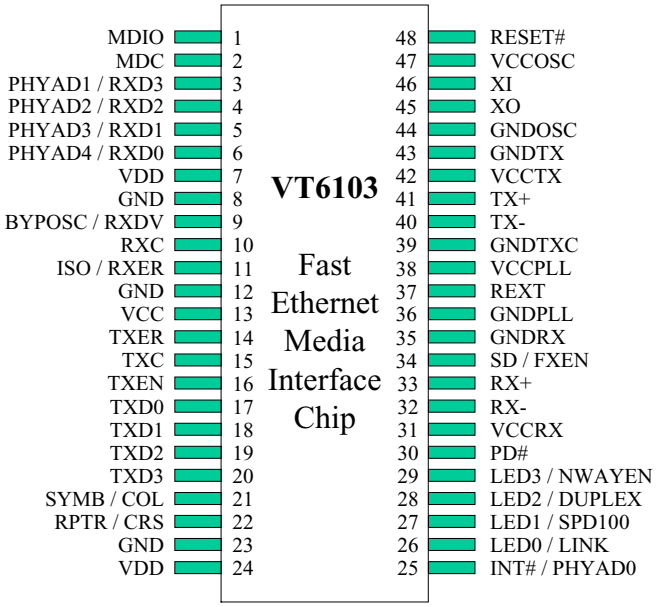


Figure 2. Pin Diagram

Pin List

Table 1. Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name
21	O / I	COL / SYMB	5	IO / I	RXD1 / PHYAD3
22	O / I	CRS / RPTR	4	IO / I	RXD2 / PHYAD2
8	**P**	**GND**	3	IO / I	RXD3 / PHYAD1
12	**P**	**GND**	9	IO / I	RXDV / BYPOSC
23	**P**	**GND**	11	O / I	RXER / ISO
44	**P**	**GNDOSC**	34	I / I	SD / FXEN
36	**P**	**GNDPLL**	40	O	TX–
35	**P**	**GNDRX**	41	O	TX+
43	**P**	**GNDTX**	15	O	TXC
39	**P**	**GNDTXC**	17	I	TXD0
25	O / I	INT# / PHYAD0	18	I	TXD1
26	O / I	LED0 / LINK	19	I	TXD2
27	O / I	LED1 / SPD100	20	I	TXD3
28	O / I	LED2 / DUPLEX	16	I	TXEN
29	O / I	LED3 / NWAYEN	14	I	TXER
2	I	MDC	**13**	**P**	**VCC**
1	IO	MDIO	**47**	**P**	**VCCOSC**
30	I	PD#	**38**	**P**	**VCCPLL**
48	I	RESET#	**31**	**P**	**VCCRX**
37	A	REXT	**42**	**P**	**VCCTX**
32	I	RX–	**7**	**P**	**VDD**
33	I	RX+	**24**	**P**	**VDD**
10	O	RXC	46	I	XI
6	IO / I	RXD0 / PHYAD4	45	O	XO

Pin Descriptions

Table 2. Pin Descriptions

Management Interface (MI)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MDIO	1	IO	**Management Interface (MI) Data I/O.** Received from the external MAC.
MDC	2	I	**Management Interface (MI) Clock.** Received from the external MAC as a timing reference for MDIO
INT# / PHYAD0	25	O	**Management Interface (MI) Interrupt Out.** Active low.

Media Independent Interface (MII)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RXC	10	O	**Receive Clock.** Timing reference for transfer of RXD and RXDV. 25 MHz when operating at 100 Mbps and 2.5 MHz when operating at 10 Mbps (always active).
RXD3 / PHYAD1, **RXD2** / PHYAD2, **RXD1** / PHYAD3, **RXD0** / PHYAD4	3 4 5 6	O	**Receive Data.** These bits transition with RXC. RXD[3:0] should accepted by the external MAC for each RXC period in which RXDV is asserted. RXD0 is the least significant bit. While RXDV is de-asserted, RXD[3:0] have no effect upon the switch's MAC and the value of RXD[3:0] is unspecified.
RXDV / BYPOSC	9	O	**Receive Data Valid.** RXDV is driven to indicate that nibbles are being presented on the MII for receiving. RXDV transitions synchronous to RXC. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be received are presented to the MII.
RXER / ISO	11	O	**Receive Error.** The VT6103 asserts this output when it receives invalid symbols from the network
TXC	15	O	**Transmit Clock.** Timing reference for transfer of TXD and TXEN. 25MHz when operating at 100 Mbps and 2.5 MHz when operating at 10 Mbps (always active).
TXD[3-0]	20, 19, 18, 17	I	**Transmit Data.** These bits transition relative to TXC. TXD[3:0] are accepted from the external MAC for each TXC period in which TXEN is asserted. TXD0 is the least significant bit. While TXEN is de-asserted, TXD[3:0] have no effect and the value of TXD[3:0] is unspecified.
TXEN	16	I	**Transmit Enable.** Indicates transmit active from the MII port. TXEN transitions synchronous to TXC. TXEN indicates that the nibbles presented on TXD[3-0] are valid for transmission. TXEN is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented to the MII interface.
TXER	14	I	**Transmit Error.** The MAC asserts this input when an error has occurred in the input stream.
COL / SYMB	21	O	**Collision Detect.** Asserted asynchronously upon detection of a collision on the medium and remains asserted while the collision condition persists.
CRS / RPTR	22	O	**Carrier Sense.** Asserted asynchronously upon detection of a non-idle medium or while TXEN is asserted. Deasserted asynchronously upon detection of idle conditions on both transmit and receive media. Remains asserted throughout the duration of a collision condition.

Physical Cable Connection			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TX+	41	O	**Transmit Plus.** Differential outputs for FX, 100BaseTx, or 10BaseT transmission.
TX–	40	O	**Transmit Minus.** Differential outputs for FX, 100BaseTx, or 10BaseT transmission.
RX+	33	I	**Receive Plus.** Differential inputs for FX, 100BaseTx, or 10BaseT reception.
RX–	32	I	**Receive Minus.** Differential inputs for FX, 100BaseTx, or 10BaseT reception.

Strap Options			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SYMB / COL	21	I	**Symbol Mode.** Latched into register 16 (register 10h) bit-2 at power-up / reset. Internally pulled low for default disabled.
RPTR / CRS	22	I	**Repeater Mode.** Latched into register 16 (register 10h) bit-4 at power-up / reset. Internally pulled low for default disabled.
ISO / RXER	11	I	**Isolate.** Latched into register 0 bit-10 at power-up / reset. Internally pulled low for default disabled.
PHYAD[4:0] / RXD[0:3], INT#	6, 5, 4, 3, 25	I	**PHY Address.** Latched into register 16 (register 10h) bits 15-11 at power-up / reset. Internally pulled low, low, low, low, and high for default 00001b.
LINK / LED0	26	I	**Test Mode Enable.** 0=Enable, 1=Disable. Do not leave floating. Pull high with 10K ohms if not used.
SPD100 / LED1	27	I	**Speed Select.** Latched into register 0 bit-13 at power-up / reset (0=Speed 10, 1=Speed100). If NWAYEN is not pulled down at power-up / reset, this pin is also latched as Speed support in register 4 (Auto-Negotiation Advertisement Base Page). Do not leave floating. Pull high or low with 10K ohms.
DUPLEX / LED2	28	I	**Duplex Mode Select.** Latched into register 0 bit-8 at power-up / reset (0=Half, 1=Full). If NWAYEN is not pulled down at power-up / reset, this pin is also latched as Duplex support in register 4 (Auto-Negotiation Advertisement Base Page). Do not leave floating. Pull high or low with 10K ohms.
NWAYEN / LED3	29	I	**N-Way Enable.** Latched into register 0 bit-12 (Auto-Negotiation Enable) at power-up / reset (0=Disable, 1=Enable). Do not leave floating. Pull low with 10K ohms if not used.
FXEN / SD	34	I	**Fiber Mode Enable.** Latched into register 16 (register 10h) bit-10 at power-up / reset (0=Disable, 1=Enable). Do not leave floating. Pull low with 10K ohms if not used.

Note: For the pins listed above, pullup / pulldown status is latched during powerup / reset. External strap option values may be set by connecting the indicated pin to a 10K ohm pull down for 0 (L) or to a 10K pull up for 1 (H).

LED Outputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
LED0 / LINK	26	IO	**LED Output 0.** See Register 16 (10h) bits 5-6 & Table 6 for LED function.
LED1 / SPD100	27	IO	**LED Output 1.** See Register 16 (10h) bits 5-6 & Table 6 for LED function.
LED2 / DUPLEX	28	IO	**LED Output 2.** See Register 16 (10h) bits 5-6 & Table 6 for LED function.
LED3 / NWAYEN	29	IO	**LED Output 3.** See Register 16 (10h) bits 5-6 & Table 6 for LED function.

Resets, Clocks, Control and Status			
Signal Name	**Pin #**	**I/O**	**Signal Description**
XI	46	I	**Crystal In.** Connect to 25 MHz crystal and to 22pF 5% to GNDOSC. Can alternately be driven by an external clock source (3.3V voltage swing) with XO unconnected.
XO	45	O	**Crystal Feedback.** Connect to other side of 25 MHz crystal and to 22pF 5% to GNDOSC
BYPOSC / RXDV	9	I	**Bypass Oscillator.** Connect to pullup to use an external oscillator instead of a crystal.
REXT	37	A	**External Resistor.** Connect 6.49K 1% resistor to GNDOSC.
SD / FXEN	34	I	**Signal Detect.** Used in fiber mode.
PD#	30	I	**Power Down.** Active low.
RESET#	48	I	**Reset.** Active low. Schmitt input for improved noise immunity..

Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VDD	7, 24	P	**Digital I/O Power.** 3.3V nominal (3.15V to 3.45V). For digital I/O
GND	8, 23	P	**Ground.** Connect to primary motherboard ground plane.
VCC	13	P	**Core Power.** 3.3V nominal (3.15V to 3.45V). For internal digital logic.
GND	12	P	**Core Ground.** Connect to primary motherboard ground plane.
VCCOSC	47	P	**Oscillator Power.** 3.3V. Isolate from digital supply voltage with a ferrite bead
GNDOSC	44	P	**Oscillator Ground.** Connect to primary motherboard ground plane.
VCCRX	31	P	**Receiver Power.** 3.3V. Isolate from digital supply voltage with a ferrite bead
GNDRX	35	P	**Receiver Ground.** Connect to primary motherboard ground plane.
VCCTX	42	P	**Transmitter Power.** 3.3V. Isolate from digital supply voltage with a ferrite bead
GNDTX	43	P	**Transmitter Ground.** Connect to primary motherboard ground plane.
GNDTXC	39	P	**Transmit Clock Ground.** Connect to primary motherboard ground plane.
VCCPLL	38	P	**PLL Power.** 3.3V. Isolate from digital supply voltage with a ferrite bead
GNDPLL	36	P	**PLL Ground.** Connect to primary motherboard ground plane.

REGISTERS

Register Overview

The VT6103 internal register set consists of thirty-two 16-bit MI (Management Interface) registers (of which 9 registers are currently undefined / reserved).

The bits of PHY registers 0-8 are defined by the IEEE 802.3u standard. The remaining PHY registers have vendor specific bit definitions. All register bits implemented by the VT6103 are described in this data sheet (see register summary table below, bit summary table on the next page, and detailed register descriptions on following pages).

PHY registers are addressed by the MAC by sending register address pointer information via the MI interface (serially over the MDIO pin clocked by MDC) with register read / write data transfer via the same pins. For more information on this mechanism, refer to IEEE 802.3 section 22.2.4.

In the register descriptions that follow, the following abbreviations are used:

RW = Read / Write
RO = Read Only
SC = Self Clearing
LH = Latch High
LL = Latch Low

"Self Clearing" bits are normally 0. If set to 1 they will perform the indicated function then automatically be cleared back to 0 by the chip. "Latch High" and "Latch Low" bits are used to record that an event (level) occurred. For Latch High bits, if the bit ever goes high, it will latch at that high level until read (the read will clear the bit). For "Latch Low" bits, if the bit goes low, it will stay at a low level until read (the read will set the bit high).

Table 3. Register Summary

Offset	Offset	Management Interface Registers	Bits	Default	Acc	Page
00	00h	Management Interface Control	16	3100h	RW	9
01	00h	Management Interface Status	16	7849h	**RO**	9
02	01h	PHY Identifier 0	16	0101h	**RO**	9
03	02h	PHY Identifier 1	16	8F20h	**RO**	9
04	03h	Auto-Negotiation Advertisement Base	16	05E1h	RW	10
05	04h	Link Partner Advertisement Base	16	0000h	**RO**	10
06	05h	Auto-Negotiation Expansion	16	0004h	**RO**	10
07	06h	Auto-Negotiation Advertisement Next	16	2001h	RW	10
08	07h	Link Partner Advertisement Next	16	0000h	**RO**	10
9-15	09-0Fh	-reserved-	—	—	—	
16	10h	PHY Configuration 1	16	0800h	RW	11
17	11h	PHY Configuration 2	16	F7FFh	RW	11
18	12h	PHY Configuration 3	16	0800h	RW	11
19	13h	PHY Configuration 4	16	FFFCh	RW	12
20	14h	PHY Status	16	0000h	**RO**	12
21	15h	Link Fail Counter	16	0000h	**RO**	13
22	16h	Invalid Symbol / Jabber Error Counter	16	0000h	**RO**	13
23	17h	False Carrier / SQE Counter	16	0000h	**RO**	13
24-25	18-19h	-reserved-	—	—	—	
26	1Ah	PHY Test Configuration 1	16	0012h	RW	14
27	1Bh	PHY Test Configuration 2	16	C500h	RW	14
28	1Ch	PHY Test Configuration 3	16	0208h	RW	15
29	1Dh	PHY Test Configuration 4	16	0030h	RW	15
30	1Eh	PHY Test Configuration 5	16	001Bh	RW	15
31	1Fh	PHY Test Configuration 6	16	0000h	RW	15

Table 4. Register Bit Summary – Registers Defined by 802.3u

Bit	Register 0	Register 1	Register 2	Register3	Register4	Register 5	Register 6	Register 7	Register 8
15	Reset	Cap 100T4	OUI (msb)	OUI (lsb)	Next Pg	LP Next Pg	–	Next Page	LP NxtPg
14	Loop Back	Cap Tx100F			Ack	LP Ack		Ack1	LP Ack1
13	Speed	Cap Tx100H			Rem Flt	LP Rem Flt		Msg Page	LP MP
12	Aneg Ena	Cap Tx10F			–	–		Ack2	LP Ack2
11	Power Down	Cap Tx10H			–	–		Toggle	LP Toggle
10	Isolate	Cap 100T2F			Pause	LP Pause		Message Code Field or Unformatted Code Field	Link Partner Message Code Field or Unformatted Code Field
9	Aneg Restart	Cap 100T2H		Part Number	100T4	LP 100T4			
8	Duplex	Extd Status			Tx100F	LP Tx100F			
7	COL Test	–			Tx100H	LP Tx100H			
6	–	Cap Supr			Tx10F	LP Tx10F			
5		Aneg Complete			Tx10H	LP Tx10H			
4		Remote Fault			Selector Field	Link Partner Selector Field	Parallel Fault Det		
3		Cap Aneg		Revision Number			LP Cap Next Pg		
2		Link Status					Cap Next Page		
1		Jabber Detect					Aneg Page Rcvd		
0		Extd Reg					LP Cap Aneg		

Table 5. Register Bit Summary - Vendor Defined Registers

Bit	Register 16	Register 17	Register 18	Register 19	Register 20	Rx21	Rx22	Rx23	26-31
15	PHY Address	Jabber Det	Byp Scram	Mask Interrupt	Polarity Invert	Link Fail Count	Receive Error Count	False Carrier Count	Used For Test
14		SQE Detect	Byp 4B5B	Mask Link Up Int	Link Up Status				
13		Pol Correct	Byp Align	Mask Link Fail Int	Link Fail Status				
12		FarEndFault	Byp NRZI	Mask Link Change Int	Link Status				
11		ChangeSeed	LostSyncEna	Mask Aneg Compete Int	Aneg Comp Status				
10	Fiber Mode	Seed	LostSyncSel	Mask Page Rcvd Int	Page Rcvd Status				
9	Cable Type		–	Mask Jabber Int	Jabber Status				
8	Force Link			Mask Rcvd Code Err Int	Rcvd Code Err Status				
7	10LoSquSel			Mask Bad SSD Int	Bad SSD Status				
6	Repeater			Mask Bad ESD Int	Bad ESD Status				
5	LED Select			Mask SQE Err Int	SQE Err Status				
4				Mask LnkFail MaxCnt Int	LnkFail MaxCnt Status				
3	Int Select			Mask Rx Err MaxCnt Int	Rx Err MaxCnt Status				
2	Symbol			Mask FalCarr MaxCnt Int	FalseCarr MaxCnt Stat				
1	–			–	Speed				
0	–			–	Duplex				

Register Descriptions

Offset 0 (00h) – MI Control (3100h)..... RW

15 **PHY Reset** .....default = 0, SC
14 **Loopback Mode**
0 Disable .....default
1 Enable
13 **Speed Select LSB**
0 10
1 100 **.....default**
12 **Auto-Negotiation Process**
0 Disable
1 Enable **.....default**
11 **Power Down**
0 Disable .....default
1 Enable
10 **Electrically Isolate PHY from MII**
0 Disable .....default
1 Enable
9 **Auto-Negotiation Restart**.....default = 0, SC
8 **Duplex Mode Select**
0 Half
1 Full **.....default**
7 **COL Test**
0 Disable .....default
1 Enable
6 **Speed Select MSB** .....reserved, always reads 0
5-0 **Reserved** ..... always reads 0

Offset 1 (01h) – MI Status (7849h)..... RO

15 **Capable of 100 Base-T4 Operation**..... def=0
14 **Capable of 100 Base-TX Full Duplex** ..... def=1
13 **Capable of 100 Base-TX Half Duplex** ..... def=1
12 **Capable of 10 Base-TX Full Duplex** ..... def=1
11 **Capable of 10 Base-TX Half Duplex** ..... def=1
10 **Capable of 100 Base-T2 Full Duplex** ..... def=0
9 **Capable of 100 Base-T2 Half Duplex** ..... def=0
8 **Extended Status Information in Rx15**..... def=0
7 **Reserved** .....always reads 0
6 **Capable of Accepting MI Frames with MI Preamble Suppressed**..... def=1
5 **Auto-Negotiation Process Completed**..... def=0
4 **Remote Fault Condition Detected** .....LH, def=0
3 **Capable of Auto-Negotiation Operation** ..... def=1
2 **Link Status** ..... LL, def=0
1 **Jabber Condition Detected**.....LH, def=0
0 **Capable of Extended Register**..... def=1

Offset 2 (02h) – PHY Identifier 0 (0101h) ..... RO

15-0 **Company ID MSBs** .....always reads 0101h

Offset 3 (03h) – PHY Identifier 1 (8F20h)..... RO

15-10 **Company ID LSBs** .....always reads 23h
9-4 **Manufacturer's Part number** .....always reads 32h
3-0 **Manufacturer's Revision Number**....always reads 0

Offset 4 (04h) – AutoNegotiation Advertisement Base Page (05E1h) ..... RW

15	**Next Page**	default = 0
14	**Received Code Word Recognized**	RO, default = 0
13	**Remote Fault**	default = 0
12-11	**Reserved**	always reads 0
10	**Pause Operation for Full Duplex Link**	default = 1
9	**100 Base-T4 Capable**	default = 0
8	**100 Base-TX Full DuplexCapable**	default = 1
7	**100 Base-TX Half Duplex Capable**	default = 1
6	**10 Base-TX Full Duplex Capable**	default = 1
5	**10 Base-TX Half Duplex Capable**	default = 1
4-0	**Selector Field**	default = 00001b

Offset 5 (05h) – Link Partner Advertisement Base Page (0000h) ..... RO

15	**Next Page**	default = 0
14	**Received Code Word Recognized**	default = 0
13	**Remote Fault**	default = 0
12-11	**Reserved**	always reads 0
10	**Pause Operation for Full Duplex Link**	default = 0
9	**100 Base-T4 Capable**	default = 0
8	**100 Base-TX Full DuplexCapable**	default = 0
7	**100 Base-TX Half Duplex Capable**	default = 0
6	**10 Base-TX Full Duplex Capable**	default = 0
5	**10 Base-TX Half Duplex Capable**	default = 0
4-0	**Selector Field**	default = 0

Offset 6 (06h) – Auto-Negotiation Expansion (0004h) .... RO

15-5	**Reserved**	always reads 0
4	**Parallel Fault Detect in Auto-Negotiation Process**	LH, default = 0
3	**Link Partner Capable of Next Page Process**	default = 0
2	**Capable of Next Page Process**	default = 0
1	**Page Received in Auto-Negotiation Process**	LH, default = 0
0	**Link Partner Capable of Auto-Negotiation Process**	default = 0

Offset 7 (07h) – AutoNegotiation Advertisement Next Page (2001h) ..... RW

15	**Next Page**	default = 0
14	**Received Code Word Recognized**	RO, default = 0
13	**Message Page**	default = 1
12	**Capable of Complying with Message**	default = 0
11	**Toggle Bit**	RO, default = 0
10-0	**Message Code Field or Unformatted Code Field**	default = 001h

Offset 8 (08h) – Link Partner Advertisement Next Page (0000h) ..... RO

15	**Next Page**	default = 0
14	**Received Code Word Recognized**	default = 0
13	**Message Page**	default = 0
12	**Capable of Complying with Message**	default = 0
11	**Toggle Bit**	default = 0
10-0	**Message Code Field or Unformatted Code Field**	default = 0

Offset 16 (10h) – PHY Configuration 1 (0800h).....RW

15-11 PHY Address..... default = 01h

10 Fiber Mode
- 0 Disable .....default
- 1 Enable

9 Cable Type
- 0 UTP5 and STP (100 ohm) cable .....default
- 1 STP 150 ohm cable

8 Force PHY in Link Good Status
- 0 Disable .....default
- 1 Enable

7 Base10Tx Low Squelch Level Select
- 0 Regular Cable Length .....default
- 1 Long Cable (> 100 meters)

6-5 Programmable LED Output Select

	LED0	LED1	LED2	LED3
00	Link/Act	Speed	Duplex	COL ....def
01	Pwr/TxAct	Link/RxAct	Speed	Duplex
10	Speed100	Speed10	Act	Duplex
11	Pwr/TxAct	Link/RxAct	Speed	COL

4 Repeater Mode
- 0 Disable .....default
- 1 Enable

3 Interrupt Select
- 0 Assert interrupt on INT#.....default
- 1 Assert interrupt on MDIO

2 Symbol Mode .....RO
- 0 Disable .....default
- 1 Enable

Offset 17 (11h) – PHY Configuration 2 (F7FFh)..... RW

15 Jabber Detect
- 0 Disable
- 1 Enable..... **default**

14 Signal Quality Error Detect
- 0 Disable
- 1 Enable..... **default**

13 Auto-Polarity Correction
- 0 Disable
- 1 Enable..... **default**

12 Far End Fault Detect
- 0 Disable
- 1 Enable..... **default**

11 Change Seed ..... Self Clearing
- 0 Disable..... default
- 1 Enable

10-0 Seed .....default = 7FFh

Offset 18 (12h) – PHY Configuration 3 (0800h) ..... RW

15 Bypass Scrambler and Descrambler Functions
- 0 Disable..... default
- 1 Enable

14 Bypass 4B5B Encoding and Decoding Functions
- 0 Disable..... default
- 1 Enable

13 Bypass Symbol Alignment Function
- 0 Disable..... default
- 1 Enable

12 Bypass NRZI Encoding and Decoding Functions
- 0 Disable..... default
- 1 Enable

11 Loss Sync Function ..... Self Clearing
- 0 Disable
- 1 Enable..... **default**

10 Lost Sync Timer Select
- 0 722 usec..... default
- 1 2 msec

9-0 Reserved .....always reads 0

Offset 19 (13h) – PHY Configuration 4 (FFFCh) .....RW

15 Mask Interrupt Function
0 Disable
1 Enable .....**default**

14 Mask Interrupt on Link-Up Status
0 Disable
1 Enable .....**default**

13 Mask Interrupt on Link-Fail Status
0 Disable
1 Enable .....**default**

12 Mask Interrupt on Link Status Change
0 Disable
1 Enable .....**default**

11 Mask Interrupt on Auto-Negotiation Process Complete
0 Disable
1 Enable .....**default**

10 Mask Interrupt on Page Received in Auto-Negotiation Process
0 Disable
1 Enable .....**default**

9 Mask Interrupt on Jabber Condition Detect
0 Disable
1 Enable .....**default**

8 Mask Interrupt on Invalid Symbol Received
0 Disable
1 Enable .....**default**

7 Mask Interrupt on SSD Delimiter Error Detected
0 Disable
1 Enable .....**default**

6 Mask Interrupt on ESD Delimiter Error Detected
0 Disable
1 Enable .....**default**

5 Mask Interrupt on Signal Quality Error Detected
0 Disable
1 Enable .....**default**

4 Mask Interrupt on Link Fail Counter in Rx15 Count to Max
0 Disable
1 Enable .....**default**

3 Mask Interrupt on Invalid Symbol Received Counter in Rx16 Count to Max
0 Disable
1 Enable .....**default**

2 Mask Interrupt on False Carrier Counter in Rx17 Count to Max
0 Disable
1 Enable .....**default**

1-0 Reserved ..... always reads 0

Offset 20 (14h) – PHY Status (0000h)..... RO

15 Polarity Inversion Base10-Tx
0 Disable..... default
1 Enable

14 Link Up Status.....LH, default = 0

13 Link Fail Status ..... LL, default = 0

12 Link Status ..... default = 0

11 Auto-Negotiation Process Complete..... default = 0

10 Page Received in Auto-Negotiation Process
.....LH, default = 0

9 Jabber Condition Detect.....LH, default = 0

8 Error Code Symbol Received.....LH, default = 0

7 Start of Stream Delimiter Error .....LH, default = 0

6 End of Stream Delimiter Error.....LH, default = 0

5 Signal Quality Error Detected .....LH, default = 0

4 Link Fail Counter in Rx15 Count to Max
.....LH, default = 0

3 Invalid Symbol Received Counter in Rx16 Count to Max .....LH, default = 0

2 False Carrier Counter in Rx17 Count to Max
.....LH, default = 0

1 PHY Speed Status ..... default = 0
0 PHY Duplex Status ..... default = 0

Offset 21 (15h) – Link Fail Counter (0000h) .....RO

15-0 Link Fail Count..... default = 0

Offset 22 (16h) – Invalid Symbol / Jabber Error Counter (0000h) .....RO

Speed 100

15-0 Count of Invalid Symbols Received ..... default = 0

Speed 10

15-0 Jabber Detect Count..... default = 0

Offset 23 (17h) – False Carrier / SQE Counter (0000h). RO

Speed 100

15-0 False Carrier Count..... default = 0

Speed 10

15-0 SQE Detect Count..... default = 0

Offset 26 (1Ah) – PHY Test Configuration 1 (0012h) ...RW

15 PHY Capability to Set Baseline Wander Correction Circuit Correction Amount
- 0 Disable .....default
- 1 Enable

14-9 Baseline Wander Correction Circuit Value

8 PHY Capability to Read Baseline Wander Correction Circuit Correction Amount
- 0 Disable .....default
- 1 Enable

7 Baseline Wander Upper Limit Overflow Indication .....LH
- 0 Disable .....default
- 1 Enable

6 Baseline Wander Lower Limit Overflow Indication .....LH
- 0 Disable .....default
- 1 Enable

5-4 FTxD10, FTxData10En Clock Phase Selection ..... default = 01b

3 Drive Kill Pattern Mode
- 0 Disable .....default
- 1 Enable

2 Asynchronous Baseline Wander Correction
- 0 Disable .....default
- 1 Enable

1-0 Asynchronous Baseline Wander Correction Peak Detection Threshold ..... default = 10h

Offset 27 (1Bh) – PHY Test Configuration 2 (C500h) .. RW

15 10 Squelch Signals Debounce
- 0 Disable
- 1 Enable**..... default**

14 10 Squelch Signals Go Idle State Debounce
- 0 Disable
- 1 Enable**..... default**

13 10 Squelch Signals Idle Condition Select ..... def = 0

12 NLP Pulse Length
- 0 100 ns ..... default
- 1 150 ns

11 Force Transmit Data
- 0 Disable..... default
- 1 Enable

10 NLP Watchdog
- 0 Disable
- 1 Enable (10 will go Link Fail if too many NLP's received in NLPMinTime at Link Up Status)**..... default**

9 Set Rx21-23 MIB Counters to FFFEh
- 0 Disable..... default
- 1 Enable..... Self Clearing

8 10 Stop Receive Data if Squelch Signals Go Idle State
- 0 Disable
- 1 Enable**..... default**

7 Drive Overshoot Pattern for 100 Characterization
- 0 Disable..... default
- 1 Enable

6 Fast Drive NLP Pattern for 10 Characterization
- 0 Disable..... default
- 1 Enable

5 F Direct Drive (See Bits 0-4)
- 0 Disable..... default
- 1 Enable

4 Replacement Value for TXER if FDirectDrive (bit-5) is Set

3-0 Replacement Value for TXD if FDirectDrive (bit-5) is Set

Offset 28 (1Ch) – PHY Test Configuration 3 (0208h) ...RW

15 Hold DPLL Phase Setting
- 0 Disable .....default
- 1 Enable

14-10 DPLL Clock Phase Setting..... default = 0

9-8 DPLL Low Pass Filter Bandwidth ..... default = 10b

7 Output DPLL Recovered Clock Phase to PHY
- 0 Disable .....default
- 1 Enable

6 PHY Set DPLL Phase Capability
- 0 Disable .....default
- 1 Enable

5 DPLL Loopback Mode
- 0 Disable .....default
- 1 Enable

4 Rd100, Rd10 Output to PHY
- 0 Disable .....default
- 1 Enable

3 Slew Rate Control for 100 Transmitter
- 0 Disable
- 1 Enable **.....default**

2 Baseline Wander Correction
- 0 Disable .....default
- 1 Enable

1 Equalizer Peak Detector Scheme Control Using Value in Bit-0
- 0 Disable .....default
- 1 Enable

0 Control Equalizer Peak Detector Scheme ... def = 0

Offset 29 (1Dh) – PHY Test Configuration 4 (0030h)... RW

15 Hold Adeq Operation, Keep Current Equalizer Gain Setting
- 0 Disable..... default
- 1 Enable

14-9 Adeq Gain Amount Setting ..... default = 0

8 Adeq Can Output Gain Setting
- 0 Disable..... default
- 1 Enable

7 PHY Can Set Adeq Gain Amount
- 0 Disable..... default
- 1 Enable

6-5 Adeq Low Pass Filter Bandwidth ..... default = 01b

4 Adeq Test Buffers AOP1/AON1, AOP2/AON2
- 0 Disable
- 1 Enable**..... default**

3-2 Adeq Clock Setting for 100BaseT Adaptive Equalizer ..... default = 0

1 Bypass 10BaseT Receiver Filter
- 0 Disable..... default
- 1 Enable

0 Mask Sqh10m and Sq110m in Test Mode
- 0 Disable..... default
- 1 Enable

Offset 30 (1Eh) – PHY Test Configuration 5 (001Bh) .. RW

15-14 Fx Mode Transmitter Current Source Control, 10BaseT Transmitter Output Slew Rate Control ..... default = 00b

13-12 10BaseT Pre-Emphasis Control..... default = 00b

11-10 Control Attenuator Attenuation Factor, 100 Transmitter Output Amplitude ... default = 00b

9-8 100BaseT Programmable Select Clock Phase to Latch Transmit Data ..... default = 00b

7-6 10BaseT Transmitter Output Signal Amplitude ..... default = 00b

5-3 ADEQ Peak Detector Reference Peak Select ..... default = 011b

2-0 ADEQ Slicer Threshold Level Select ..... default = 011b

Offset 31 (1Fh) – PHY Test Configuration 6 (0000h) ... RW

15-10 Select Signal Output to LED Pins..... default = 0

9-5 Select Signal Output to MII Pins ..... default = 0

4 Speedup Flags in NwayTxSm..... default = 0

3 Speedup Tx10Flag in TxAct10..... default = 0

2 Speedup NLPMaxFlag in Timer..... default = 0

1 Speedup NLPMinFlag in Timer ..... default = 0

0 Speedup StabFlag in MLTStatus..... default = 0

FUNCTIONAL DESCRIPTION

General

The VT6103 is a complete 10 / 100 Mbps Ethernet Media Interface IC. The VT6103 has the following main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, and MI serial port. A block diagram is shown in Figure 3.

The VT6103 can operate as a 100Base-TX device (hereafter referred to as 100 Mbps mode) or as a 10Base-T device (hereafter referred to as 10 Mbps mode). The differences between 100 Mbps mode and 10 Mbps mode are data rate, signalling protocol, and allowed wiring. 100 Mbps TX mode uses two pairs of category 5 or better UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a throughput of 100 Mbps. 10 Mbps mode uses two pairs of category 3 or better UTP or STP twisted pair cable with Manchester encoded, 10 MHz binary data to achieve a 10 Mbps thruput. The data symbol format on the twisted pair cable for the 100 and 10 Mbps modes is defined in the IEEE 802.3 specification.

On the transmit side for 100 Mbps TX operation, data is received on the controller interface from an external Ethernet controller. The data is then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, preshapes the output, and drives the twisted pair cable.

On the receive side for 100 Mbps TX operation, the twisted pair receiver receives incoming encoded and scrambled MLT-3 data from the twisted pair cable, removes any high frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted pair levels to internal digital levels. The output of the twisted pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses the clock to latch in valid data into the device, and converts the data back to NRZ format. The NRZ data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and outputted to an external Ethernet controller by the controller interface. 10 Mbps operation is similar to 100 Mbps TX operation except (1) there is no scrambler/descrambler, (2) the encoder/decoder is Manchester instead of 4B5B, (3) the data rate is 10 Mbps instead of 100 Mbps, and (4) the twisted pair symbol data is two level Manchester instead of ternary MLT-3.

The Management Interface, (hereafter referred to as the MI serial port), is a two-pin bidirectional link through which configuration inputs can be set and status outputs can be read. Each block plus the operating modes is described in more detail in the following sections. Since the VT6103 can operate as either a 100Base-TX or a 10Base-T device, each of the following sections describes the performance of the respective section in both 100 and 10 Mbps modes.

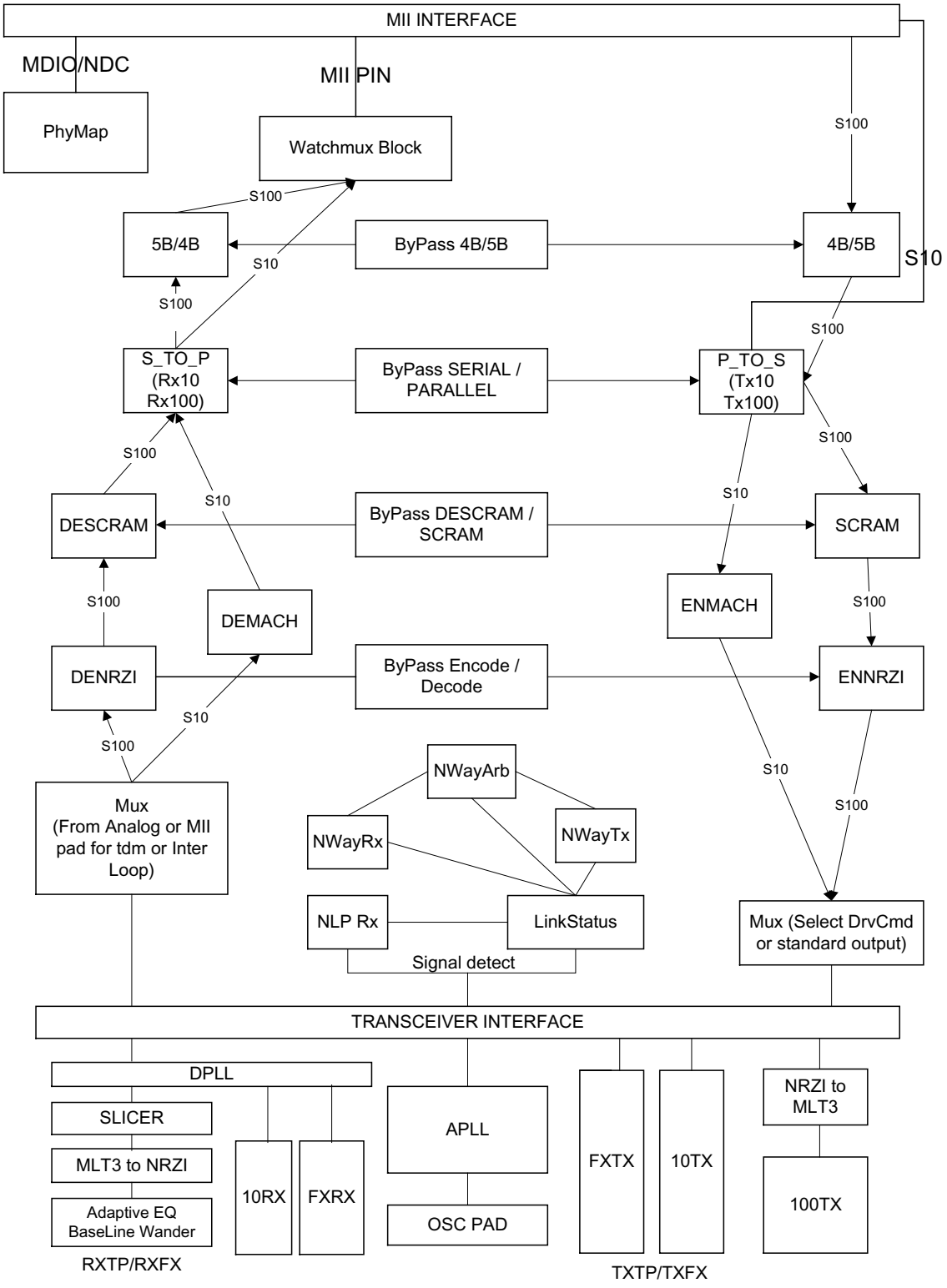


Figure 3. Internal Block Diagram

802.3u MII

The VT6103 incorporates the Media Independent Inter-face (MII) as specified in clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to MAC or repeater devices in 10/100 Mb/s systems. This section describes both the serial MII management interface as well as the nibble wide MII data interface. The management interface of the MII allows the configuration and control of multiple PHY devices, the gathering of status and error information, and the determination of the type and abilities of the attached PHY(s). The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC or repeater.) The VT6103 supports the MII interrupt function.

Serial Management Register Access

The serial MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the serial management data interface pins MDC and MDIO. The VT6103 implements all the required MII registers as well as several optional registers. These registers are fully described in the registers section of this document. A description of the serial management access protocol follows.

Serial Management Access Protocol

The serial control interface consists of two pins, Management Data Clock (MDC) and Management Data Input/Output (MDIO). MDC has a maximum clock rate of 10 MHz and no minimum rate. The MDIO line is bidirectional and may be shared by up to 32 devices. The MDIO frame format is shown in IEEE802.3, section 22.2.4.4. The MDIO pin has an internal pull-up resistor (1.5Kohm) which will pull MDIO high during IDLE and turnaround. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the VT6103 with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pull-up resistor to pull the MDIO pin high during which time 32 MDC clock cycles are provided. In addition, 32 MDC clock cycles should be used if an invalid start, pop code, or turn-around bit is detected.

The VT6103 waits until it has received this preamble sequence before responding to any other transaction. Once the VT6103 serial management port has initialized, no further preamble sequencing is required until after a power-on / reset has occurred. The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state. Turnaround is an idle bit time inserted between the Register Address field and the Data field. To avoid contention, no device actively drives the MDIO signal during the first bit of Turnaround during a read transaction. The addressed VT6103 drives MDIO with a zero for the second bit of Turn-around and follows this with the required data. IEEE 802.3 section 22.3.4.1 shows the timing relationship between MDC and MDIO as driven / received by the Station Management Entity (SME) and the VT6103 (PHY) for a typical register read access. For write transactions, the station management entity writes data to an addressed VT6103 eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity inserting <10> for these two bits.

Preamble Suppression

The VT6103 supports a Preamble Suppression mode. If the station management entity (i.e. MAC or other management controller) determines that all PHYs in the system support Preamble Suppression by returning a one in this bit, then the station management entity need not generate preamble for each management transaction. The VT6103 requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by the mandatory pull-up resistor on MDIO in conjunction with a continuous MDC, or the management access made to determine whether Preamble Suppression is supported. While the VT6103 requires an initial preamble sequence of 32 bits for management initialization, it does not require a full 32 bit sequence between each subsequent transaction. A minimum of one idle bit between management transactions is required as specified in IEEE 802.3u.

PHY Address Sensing

The VT6103 can be set to respond to any of the possible 32 PHY addresses. Each VT6103 connected to a common serial MII must have a unique address. It should be noted that while an address selection of all zeros <00000> will result in PHY Isolate mode, this will not effect serial management access. The VT6103 provides five PHY address pins, the state of which are latched into the PHYCTRL register (address 10h) at system power-up / reset. These pins are described in the pin descriptions section of this document.

Nibble-Wide MII Data Interface

Clause 22 of the IEEE 802.3u specification defines the Media Independent Interface. This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and indicate signals, allow for the simultaneous exchange of data between the VT6103 and the upper layer agent (MAC or repeater). The receive interface consists of a nibble wide data bus RXD[3:0], a receive error signal RXER, a receive data valid flag RXDV, and a receive clock RXC for synchronous transfer of the data. The receive clock can operate at either 2.5 MHz to support 10 Mb/s operation modes or at 25 MHz to support 100 Mb/s operational modes. The transmit interface consists of a nibble wide data bus TXD[3:0], a transmit error flag TXER, a transmit enable control signal TXEN, and a transmit clock TXC which runs at either 2.5 MHz or 25 MHz. Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The COL signal asserts as an indication of a collision which can occur during half-duplex operation when both a transmit and a receive operation occur simultaneously.

Collision Detect

For Half Duplex, a 10Base-T or 100Base-X collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

If the VT6103 is transmitting in 10 Mb/s mode when a collision is detected, the collision is not reported until seven bits have been received while in the collision state. This prevents a collision from being reported incorrectly due to noise on the network. The COL signal remains set for the duration of the collision. If a collision occurs during a receive operation, it is immediately reported by the COL signal. When heartbeat is enabled (only applicable to 10 Mb/s operation), approximately 1 ms after the transmission of each packet, a Signal Quality Error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity, once valid data is detected via the Smart Squelch function during 10 Mb/s operation. For 10 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mb/s Full Duplex operation, CRS is asserted only due to receive activity. CRS is deasserted following an end of packet. In Repeater mode (pin 63 / bit 9, register address 19h), CRS is only asserted due to receive activity.

MII Isolate Mode

A 100Base-X PHY connected to the mechanical MII interface specified in IEEE 802.3u is required to have a default value of one in bit 10 of the Basic Control Register (BCR, address 00h.). The VT6103 will set this bit to one if the PHY Address is set to 00000 upon power-up / hardware Reset. Otherwise, the VT6103 will set this bit to zero upon power-up / hardware reset. With bit 10 in the BMCR set to one, the VT6103 does not respond to packet data present at TXD[3:0], TXEN, and TXER inputs and presents a high impedance on the TXCK, RXCK, RXDV, RXER, RXD[3:0], COL, and CRS outputs. The VT6103 will continue to respond to all serial management transactions over the MII. While in Isolate mode, the TX+ / TX– outputs are dependent on the current state of Auto-Negotiation. The VT6103 can Auto-Negotiate or parallel detect to a specific technology depending on the receive signal at the RX+ / RX– inputs. It is recommended that the user have a basic understanding of clause 22 of the 802.3u standard.

Link Integrity and AutoNegotiation

General

The VT6103 can be configured to implement either the standard link integrity algorithms or the Auto Negotiation algorithm. The standard link integrity algorithms are used solely to establish an active link to and from a remote device. There are different standard link integrity algorithms for 10 and 100 Mbps modes. The Auto Negotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The standard link integrity and Auto Negotiation algorithms are described below.

10Base-T Link Integrity Algorithm – 10Mbps

The VT6103 uses the same 10Base-T link intergrity algorithm that is defined in IEEE 802.3 Clause 14. This algorithm uses normal link pulses, referred to as NLP's and transmitted during idle periods, to determine if a device has successfully established a link with a remote device (called Link Pass state). The transmit link pulse meets the template defined in IEEE 802.3 Clause 14. Refer to IEEE 802.3 Clause 14 for more details if needed.

100Base-TX Link Integrity Algorithm -100Mbps

Since 100Base-TX is defined to have an active idle signal, there is no need to have separate link pulses like those defined for 10Base-T. The VT6103 uses the squelch criteria and descrambler synchronization algorithm on the input data to determine if the device has successfully established a link with a remote device (called Link Pass state). Refer to IEEE 802.3 for both of these algorithms for more details.

AutoNegotiation Algorithm

As stated previously, the Auto Negotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The Auto Negotiation algorithm is the same algorithm that is defined in IEEE 802.3 Clause 28. Auto Negotiation uses a burst of link pulses, called fast link pulses and referred to as FLP's, to pass up to 16 bits of signaling data back and forth between the VT6103 and a remote device. The transmit FLP pulses meet the templated specified in IEEE 802.3. A timing diagram contrasting NLP's and FLP's is shown in IEEE802.3. The Auto Negotiation algorithm is initiated by any of the following events: (1) Power up, (2) device reset, (3) Auto Negotiation reset, (4) Auto Negotiation enabled, or (5) a device entering the Link Fail State. Once a negotiation has been initiated, the VT6103 first determines if the remote device has Auto Negotiation capability. If the remote device is not Auto Negotiation capable and is just transmitting either a 10Base-T or 100Base-TX signal, the VT6103 will sense that and place itself in the correct mode. If the VT6103 detects FLP's from the remote device, then the remote device is determined to have Auto Negotiation capability and the device then uses the contents of the MI serial port Auto Negotiation Advertisement register and FLP's to advertise its capabilities to a remote device. The remote device does the same, and the capabilities read back from the remote device are stored in the MI serial port Auto Negotiation Remote End Capability register. The VT6103 negotiation algorithm then matches its capabilities to the remote device's capabilities and determines what mode the device should be configured to according to the priority resolution algorithm defined in IEEE 802.3 Clause 28. Once the negotiation process is completed, the V6103 then configures itself for either 10 or 100 Mbps mode and either Full or Half Duplex modes (depending on the outcome of the negotiation process), and it switches to either the 100Base-TX or 10Base-T link integrity algorithms (depending on which mode was enabled by AutoNegotiation). Refer to IEEE 802.3 Clause 28 for more details.

AutoNegotiation Outcome Indication

The outcome or result of the Auto Negotiation process is stored in the speed detect and duplex detect bits in the MI serial port Status Output register.

AutoNegotiation Status

The status of the Auto Negotiation process can be monitored by reading the Auto Negotiation acknowledgement bit in the MI serial port Status register. The MI serial port Status register contains a single Auto Negotiation acknowledgement bit which indicates when an AutoNegotia-tion has been initiated and successfully completed.

AutoNegotiation Enable

The Auto Negotiation algorithm can be enabled (or re-started) by setting the Auto Negotiation enable bit in the MI serial port Control register or by strapping the LED3 pin (NWAYEN strap). When the Auto Negotiation algorithm is enabled, the device halts all transmissions including link pulses for 1250-1600 mS, enters the Link Fail State, and restarts the negotiation process. When the Auto Negotiation algorithm is disabled, the selection of 100 Mbps or 10 Mbps modes is determined by the speed select bit in the MI serial port Control register, and the selection of Half or Full Duplex is determined by the duplex select bit in the MI serial port Control register.

Auto Negotiation Reset

The AutoNegotiation algorithm can be initiated at any time by setting the Auto Negotiation reset bit in the MI serial port Control register.

Link Indication

Link activity is also indicated on the LED0 pin whenever a link is detected. LED0 starts blinking on activity.

Encoder

4B5B Encoder – 100 Mbps

100Base-TX requires that the data be 4B5B encoded. 4B5B coding converts the 4-Bit data nibbles into 5-Bit data code words. The mapping of the 4B nibbles to the 5B code words is specified in IEEE 802.3. The 4B5B encoder takes 4B nibbles and converts to 5B words according to IEE802.3, and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first 8 bits of the preamble with the SSD delimiters (/J/K symbols) and adds an ESD delimiter (/T/R symbols) to the end of every packet, as defined in IEEE 802.3. The 4B5B encoder also fills the period between packets, called the idle period, with a continuous stream of idle symbols, as shown in IEE802.3.

Manchester Encoder – 10 Mbps

The Manchester encoding process combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit cell. The Manchester encoder in the VT6103 converts the 10 Mbps NRZ data from the controller interface into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Manchester encoding of the NRZ data occurs only when TXEN is asserted.

Decoder

4B5B Encoder – 100 Mbps

Since the TP input data is 4B5B encoded on the transmit side, it must also be decoded by the 4B5B decoder on the receive side. The mapping of 5B nibbles to 4B code words is specified in IEEE 802.3. The 4B5B decoder takes the 5B code words from the descrambler, converts them into 4B nibbles. The 4B5B decoder also strips off the SSD delimiter (/J/K symbols) and replaces them with two 4B Data 5 nibbles (/5 symbol), and strips off the ESD delimiter (/T/R symbols) and replaces it with two 4B Data 0 nibbles (/I symbol), per IEEE 802.3 specifications. The 4B5B decoder detects SSD, ESD and, codeword errors in the incoming data stream as specified in IEEE 802.3. These errors are indicated by asserting RXER output while the errors are being transmitted across RXD[3:0], and they are also indicated in the MI Register by setting SSD, ESD, and codeword error bits in the MI Status Output register.

Manchester Encoder – 10 Mbps

In Manchester coded data, the first half of the data bit contains the complement of the data and the second half of the data bit contains the true data. The Manchester decoder converts the Manchester encoded data stream from the TP receiver into NRZ data for the controller interface by decoding the data and stripping off the SOI pulse. Since the clock and data recovery block has already separated the clock and data from the TP receiver, the Manchester decoding process to NRZ data is inherently performed by that block.

Clock and Data Recovery

Clock Recovery – 100 Mbps

Clock recovery is done with a PLL. If there is no valid data present on the TP inputs, the PLL is locked to the 25 MHz TXC Transmit Clock. When valid data is detected on the TP inputs with the squelch circuit and when the adaptive equalizer has settled, the PLL input is switched to the incoming data on the TP input. The PLL then recovers a clock by locking onto the transitions of the incoming signal from the twisted pair wire. The recovered data clock frequency is 125 MHz and is divided down to produce a 25 MHz clock that is sent to the controller interface signal RXC Receive Clock. The PLL can reliably perform the clock and data recovery process with up to +/-3 ns or jitter on the TP input. The VT6103 has an internal PLL watchdog timer that monitors the receiver PLL output frequency. If the receive PLL output frequency deviates from the TXC frequency by more that 3% over a 8 us interval, the device assumes that the receive PLL has not locked onto the TP input data properly and the PLL is reset. The PLL is reset by switching its input from the TP input data to the TXC for a period of 200 us to retrain it to the 25 MHz frequency from the oscillator.

Data Recovery – 100 Mbps

Data recovery is performed by latching in valid data from the TP receiver with the recovered clock extracted by the PLL. When invalid data is detected on the TP input, the receive data is held low. When valid data is detected on the TP inputs, the clock recovery block extracts a 125 MHz clock from the data stream from the TP receiver. This 125 MHz recovered clock is then used to latch in valid data from the TP receiver.

Clock Recovery – 10 Mbps

The clock recovery process for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the recovered clock frequency is a 2.5 MHz nibble clock, (2) the PLL is switched from TXC to the TP input when the squelch indicates valid data, and (3) the PLL takes up to 12 transitions (bit times) to lock onto the preamble, so some of the preamble data symbols are lost, but the clock recovery block recovers enough preamble symbols to pass at least 6 nibbles of preamble to the receive controller interface.

Data Recovery – 10 Mbps

The data recovery process for 10 Mbps mode is identical to the 100 Mbps mode. As mentioned in the Manchester Decoder section, the data recovery process inherently performs decoding of Manchester encoded data from the TP inputs.

Scrambler / Descrambler

100 Mbps Scrambler

100Base-TX requires scrambling to reduce the radiated emissions on the twisted pair. The VT6103 scrambler takes the encoded data from the 4B5B encoder, scrambles it per the IEEE 802.3TP-PMD specifications, and sends it to the TP transmitter.

10 Mbps Scrambler

A scrambler is not used in 10 Mbps mode.

100 Mbps Descrambler

The VT6103 descrambler takes the scrambled data from the data recovery block, descrambles it per the IEEE 802.3 TP-PMD specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder. The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE802.3 TP-PMD specification. Once the descrambler is synchronized, it will maintain synchronization as long as enough descrambled idle pattern 1's are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern 1's in a 1 ms interval. If 25 consecutive descrambled idle pattern 1's are not detected within the 1 ms interval, the descrambler goes out of synchronization and restarts the synchronization process. If the descrambler is in the unsynchronized state, the descrambler loss of synchronization detect bit is set in the MI Status Output register to indicate this condition. Once this bit is set, it will stay set until the descrambler achieves synchronization. The output of the descrambler is also aligned according to the 4B/5B code groups. This alignment procedure is done by looking for the /J/K/ symbols at the beginning of the packet and then aligning all subsequent 4B/5B words relative to the beginning of the /J/K/ symbols.

10 Mbps Descrambler

A descrambler is not used in 10 Mbps mode.

Twisted Pair Transmitter

Transmitter - 100 Mbps

The transmitter consists of an MLT-3 encoder, waveform generator and line driver. The MLT-3 encoder converts the NRZ data from the scrambler into a three level MLT-3 code. MLT-3 coding uses three levels, converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level. The purpose of the waveform generator is to shape the transmitter output pulse. The waveform generator takes the MLT-3 three level encoded waveform and uses an array of switched current sources to control the rise / fall time and level of the signal at the output. The output of the switched current sources then goes through a lowpass filter in order to "smooth" the current output and remove any high frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output. The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 ohm shielded twisted pair cable.

Transmitter - 10 Mbps

The operation of the 10 Mbps transmitter is much different from the operation of the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver. The purpose of the waveform generator is to shape the output transmit pulse.

Twisted Pair Receiver

Receiver - 100 Mbps

The TP receiver detects input signals from the twisted pair input and converts them to a digital data bit stream ready for clock and data recovery. The receiver can reliably detect data from a 100Base-TX compliant transmitter that has been passed through 0-100 meters of 100 Ohm category 5 UTP or 150 Ohm STP. The 100 Mbps receiver consists of a level shifter, low pass filter, adaptive equalizer, peak detector, comparator, baseline wander correction circuit, and MLT-3 decoder. A block diagram of the receiver is shown in Figure 3. The TP receiver inputs are assumed to be transformer coupled and terminated by external resistors. The TP inputs are then level shifted and pass through a 2nd order low pass filter designed to eliminate any high frequency noise on the input. The signal then goes to an adaptive equalizer. The adaptive equalizer consists of a programmable bandpass filter and peak detector. The adaptive equalizer uses the bandpass filter characteristic to compensate for the low pass characteristics of the cable, and it uses the peak detector to capture the peak value of the input waveform. It then uses the peak value as a measure of cable length to adjust the pole and zero placement of the bandpass filter. The bandpass filter is digitally programmable and has a 5 bit digital input, called the equalizer setting, that adjusts the frequency response to one of 32 settings. The peak detector captures the peak voltage of the TP inputs, qualifies the input, and digitizes the qualified value to a 5 bit digital result. This digital result, called the equalizer setting, is used to adjust the programmable bandpass filter characteristic. The peak detector qualifies the incoming data stream by only allowing single and double baud wide pulses to update the equalizer setting. If the digitized peak value of any single or double baud wide pulse deviates from the current equalizer setting in the same direction for more than 16 consecutive pulses, the equalizer setting is incremented by one digital step only, independent of how much the new setting and current setting differ. The equalizer updating is only enabled when the receiver is in the unsquelch state (valid data detected by the TP squelch circuit). The baseline wander correction circuit restores the DC component of the input waveform that was removed by external transformers by subtracting the filtered output of the data comparator from the filtered output of the equalizer and adding this difference back into the input of VT6103. The baseline wander correction circuit is only enabled when the descrambler is in the synchronized state. The comparators are used to qualify and slice the data. There are two types of receive comparators: squelch and data. The squelch comparator compares the signal and the output of the LPF before the equalizer against a fixed threshold. The output of the squelch comparator is used by the squelch circuit and link integrity blocks to qualify the data. The data comparators compare the signal at the output of the equalizer against fixed positive and negative thresholds. The MLT-3 decoder takes the three level MLT-3 encoded output data from the comparators and converts it to normal NRZ data to be used for clock and data recovery.

Receiver - 10 Mbps

The 10 Mbps receiver is able to detect input signals from the twisted pair cable that are within the template shown in IEEE802.3. The inputs are biased by internal resistors. The TP inputs pass through a low pass filter designed to eliminate any high frequency noise on the input. The output of the receive filter goes to two different types of comparators: squelch and zero crossing. The squelch comparator determines whether the signal is valid and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid. The output of the squelch comparator goes to the squelch circuit and is also used for link pulse detection, SOI detection, and reverse polarity detection. The output of the zero crossing comparator is used for clock and data recovery in the Manchester decoder.

Miscellaneous Functions

Smart Squelch

Smart squelch is responsible for determining when valid data is present on the differential receive inputs (TPRD+/-). The VT6103 implements an intelligent receive squelch algorithm to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. Smart squelch operation is independent of the 10Base-T operational mode. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted pair inputs (refer to IEEE802.3).

The signal at the Start of Packet is checked by the smart squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally the signal must exceed the original squelch level within a further 150 ns to ensure that the input waveform will not be rejected. The checking procedure results in the loss of typically three preamble bits at the beginning of each packet. Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart squelch circuitry is reset. Valid data is considered to be present until squelch level has not been generated for a time longer than 150ns, indicating End of Packet. Once good data has been detected the squelch levels are reduced to minimize the effect of noise causing premature End of Packet detection. The receive squelch threshold level can be lowered for use in longer cable or STP applications. This is achieved by setting the F10LSS bit in the PHYCONFIG register (bit 7, register 10h).

Collision Detection

For Half Duplex, a 10Base-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII. If the ENDEC is transmitting when a collision is detected, the collision is not reported until seven bits have been received while in the collision state. This prevents a collision from being reported incorrectly due to noise on the network. The COL signal remains set for the duration of the collision. If the ENDEC is receiving when a collision is detected, it is reported immediately (through the COL signal). When heartbeat is enabled, approximately 1 ms after the transmission of each packet, a Signal Quality Error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mb/s Full Duplex operation, CRS is asserted only due to receive activity. CRS is deasserted following an end of packet. In Repeater mode, CRS is only asserted due to receive activity.

Normal Link Pulse Detection / Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10Base-T standard. Each link pulse is nominally 100 ns in duration and is transmitted every 16 ms ± 8 ms, in the absence of transmit data. Link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted pair trans-mitter, receiver and collision detection functions. When the link integrity function is disabled, the 10Base-T transceiver will operate regardless of the presence of link pulses.

Jabber Function

The jabber function monitors the VT6103's output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 20-30 ms. Once disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal has to be deasserted for approximately 400-600 ms (the "unjabber" time) before the Jabber function re-enables the transmit outputs. The Jabber function is only meaningful in 10Base-T mode.

Status Information

VT6103 Status Information is available on the LED output pins. Transmit activity, receive activity, link status, link polarity and collision activity information is output to the four LED output pins, selectable via LEDSEL at Rx16 (Rx10h) bit[6:5] as follows:

Table 6. LED Function Definition

LEDSEL	LED0	LED1	LED2	LED3
00	Link / Act	Speed	Duplex	COL
01	Pwr / TxAct	Link / RxAct	Speed	Duplex
10	Speed 100	Speed 10	Act	Duplex
11	Pwr / TxAct	Link / RxAct	Speed	COL

Automatic Link Polarity Detection

The VT6103's 10Base-T transceiver module incorporates an automatic link polarity detection circuit. When seven consecutive link pulses or three consecutive receive packets with inverted End-of-Packet pulses are received, bad polarity is reported. The VT6103's 10Base-T transceiver module corrects for this error internally and will continue to decode received data correctly. This eliminates the need to correct the wiring error immediately.

Internal Loopback

When the FLB_DPLL bit (bit-5) of the PHY Configuration Register (register address 1Ch) is set, transmit data is looped back in the ENDEC to the receive channel. The transmit drivers and receive input circuitry are enabled in transceiver loopback mode. Loopback is used for diagnostic testing of the data path through the transceiver without transmitting on the network or being interrupted by receive traffic. This loopback function causes the data to loop back via the output driver buffers such that the entire transceiver path is tested.

100Base-FX

The VT6103 is fully capable of supporting 100Base-FX applications. 100Base-FX is similar to 100Base-TX with the exceptions being the PMD sublayer, lack of data scrambling, and signaling medium and connectors. Chapter 26 of the IEEE 802.3u specification defines the interface to this PMD sublayer. The VT6103 can be configured for 100Base-FX operation through either hardware or software. Configuration through hardware is accomplished by forcing the FXEN pin (pin 34) to a logic low level prior to power-up / reset

APPLICATION SCHEMATICS

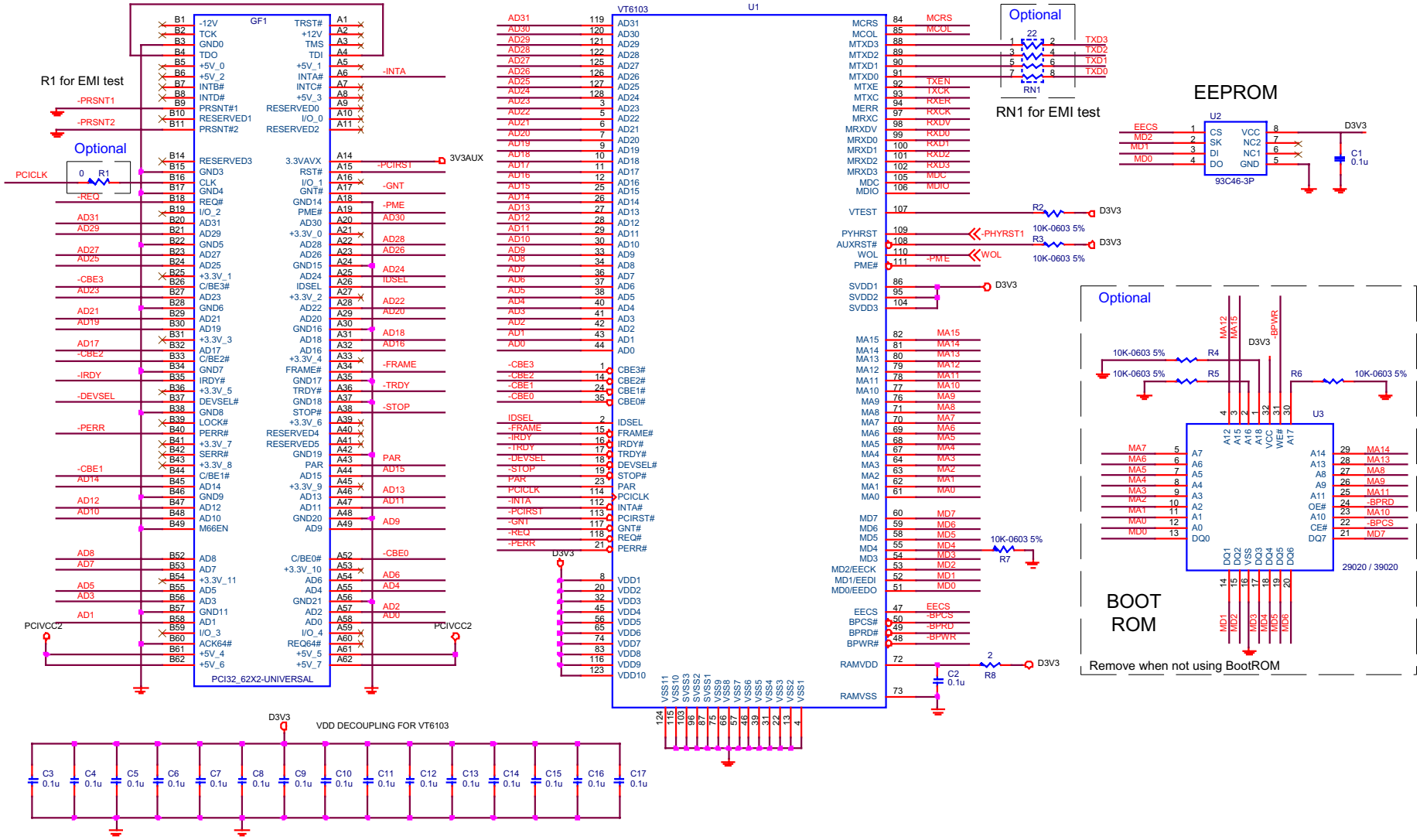


Figure 4. Application Schematic Example Page 1

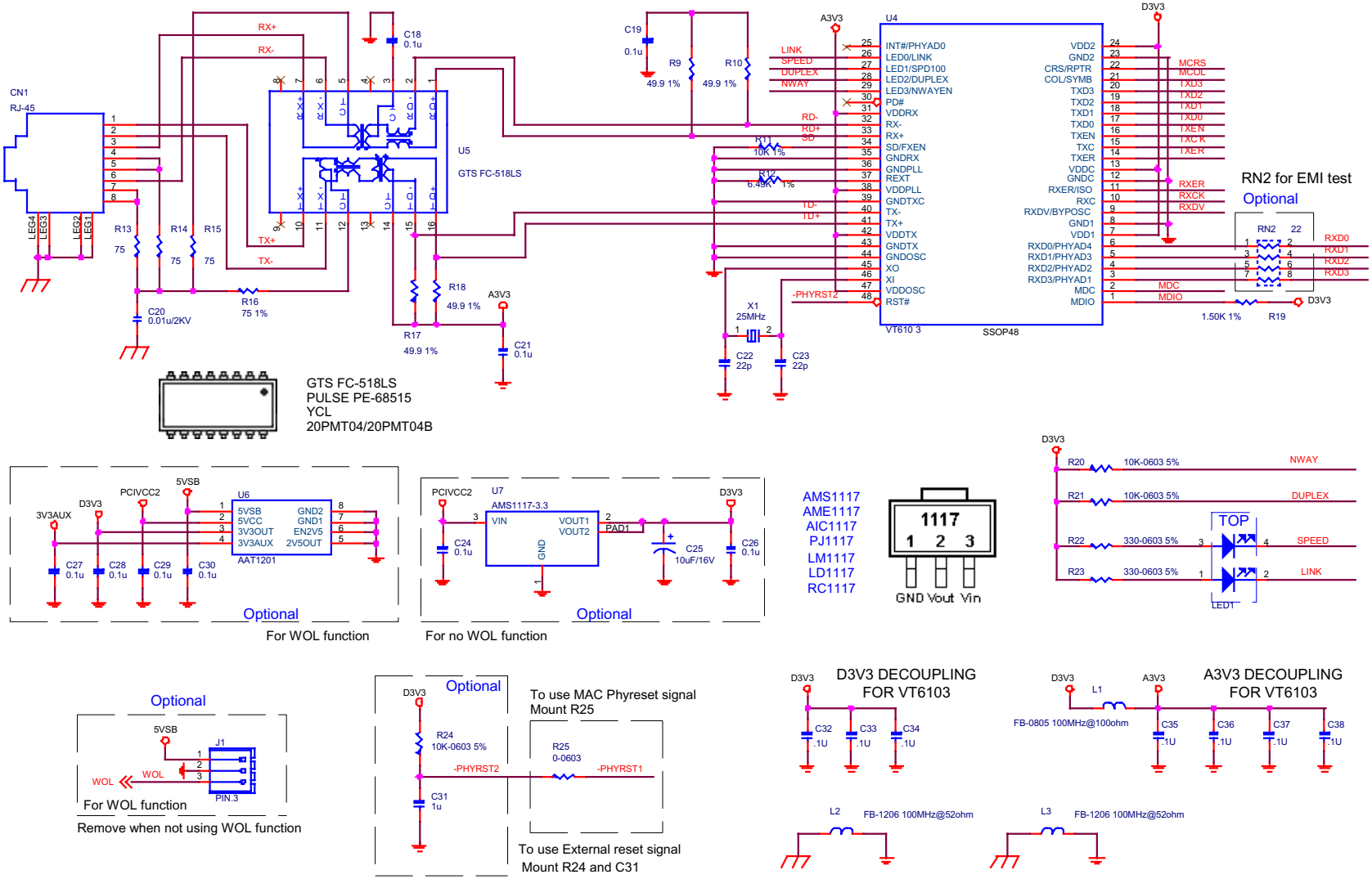


Figure 5. Application Schematic Example Page 2

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comment
Storage Temperature	-55	125	^{O}C	T_S
Operating Temperature – Case	0	100	^{O}C	T_C
Electrostatic Discharge	-	3	KV	Human Body Model
Power Supply Voltages (All)	-0.5	4.0	Volts	VDD, VCC, VCCOSC, VCCPLL, VCCRX, VCCTX
Input voltage	-0.5	V_{DD}+0.5	Volts	
Output Voltage At Any Output	-0.5	V_{DD}–0.5	Volts	

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C -0-100^{O}C, V_{DD} =3.3V ±0.3V, GND = 0V

Symbol	Parameter	Min	Max	Unit	Comment
V_{IL}	Input Low Voltage	-0.5	0.9	V	
V_{IH}	Input High Voltage	2.4	V_{DD}+0.5	V	
V_{OL}	Output Low Voltage	-	0.1 V_{DD}	V	LED0-3
V_{OH}	Output High Voltage	0.9 V_{DD}	-	V	LED0-3
I_{IL}	Input Leakage Current	-	±50	uA	
I_{OZ}	Tristate Leakage Current	-	±50	uA	
C_{IN}	Input Capacitance	-	7.5	pF	Fc=1MHz, TXD, TXEN, TXER
C_{OUT}	Output Capacitance	-	7.5	pF	Fc=1MHz, RXD, RXDV, RXER, RXCK, TXCK
I_{DD}	Power Supply Current	-	130	mA	10Base-T
I_{DD}	Power Supply Current	-	80	mA	100Base-Tx
T_{PU}	Power-Up Reset Time	2	-	ms	
T_{SETUP}	Setup Time	6		ns	50% to 50%, 10pF load
T_{HOLD}	Hold Time	0		ns	50% to 50%, 10pF load
T_{DELAY}	Delay Time		6	ns	50% to 50%, 10pF load

AC Characteristics

AC timing specifications provided assume an REXT of 6.19K ±1%, clock rate of 25MHz ±0.005%, power supply voltage of 3.3 to 3.6V, and case temperature between 0 and 100 ^{O}C.

100BaseT Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
	Output Differential Amplitude		2		Vpp	UTP (100 ohm)
	Output Differential Amplitude		2		Vpp	STP (100 ohm)
	Output Differential Amplitude		2.45		Vpp	STP (150 ohm)
	Output Symmetry	0.98		1.02	V/V	Differential Pos/Neg
T_R / T_F	Output Rise / Fall	3	4	5	ns	
	Output Rise / Fall Skew			0.5	ns	
	Output Overshoot			5	%	
	Output Timing Jitter (Peak to Peak)		0.4	1.4	ns	Scrambled
	Return Loss	16			dB	2 ~ 30 MHz
	Return Loss	16			dB	30 ~ 60 MHz
	Return Loss	20log(f/30M)10			dB	60 ~ 80 MHz
DCD	Duty Cycle Distortion	-	–0.25	0.25	ns	
	Transmitter On-Chip Power Consumption			45	mA	100 ohm

10BaseT Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
	Output Differential Amplitude	4.4	5	5.6	Vpp	UTP (100 ohm)
THD	Total Harmonic Distortion			5	%	All 1 and all 0
	Idle Pulse Width	250			ns	
	Link Pulse Width		100		ns	
	Output Jitter without Cable			±8	ns	
	Output Jitter with Cable			±3.5	ns	

Crystal Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
	Output Frequency	24.9975	25	25.0025	MHz	
	Output Frequency Jitter - Short Term			50	ps	
	Output Frequency Jitter - Long Term			500	ps	

PLL Frequency Multiplier Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
	PLL Loop Bandwidth		2.5	5	MHz	
	PLL Acquisition Time			50	us	25% Frequency Change
	VCO Operating Frequency – 100Base Mode		250		MHz	
	VCO Operating Frequency – 10Base Mode		200		MHz	
	PLL Output Clock Jitter – Short Term			200	ps	
	PLL Output Clock Jitter – Long Term			1000	ps	

FX Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
V_{OH}	PECL Output Voltage High	2.28	2.35	2.42	Volts	
V_{OL}	PECL Output Voltage Low	1.49	1.58	1.68	Volts	
V_{IH}	PECL Input Voltage High	2.135		2.42	Volts	
V_{IL}	PECL Input Voltage Low	1.49		1.825	Volts	
	FX Mode Enable Voltage (SD)	1.49		1.825	Volts	
	Input Common Mode Range	1.3		2.8	Volts	
	Input Differential Amplitude	0.15			Volts	
	Output Jitter			1.4	ns	

Table 7. MI Interface MDIO Output Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T4 / T_{MC}	MDCK Frequency			10	MHz	
T2 / T_{MIOS}	MDIO Input Setup Time	10			ns	To MDCK rising edge
T3 / T_{MIOH}	MDIO Input Hold Time	10			ns	To MDCK rising edge
T1 / T_{MOD}	MDIO Output Delay	0		300	ns	To MDCK rising edge

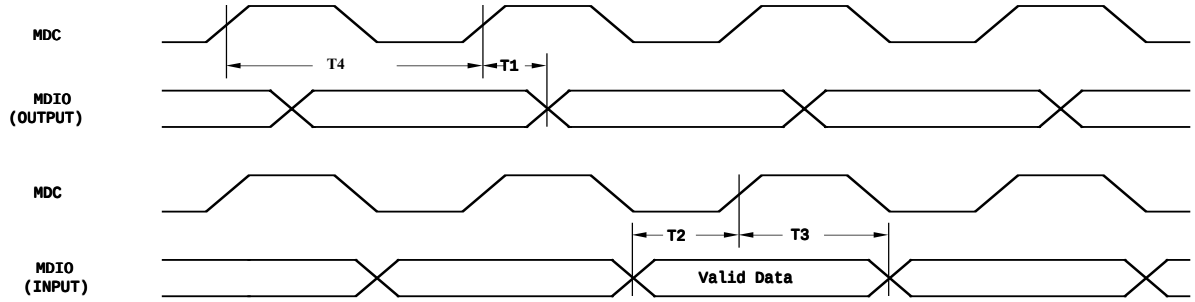


Figure 6. MI Interface MDIO Timing

Table 8. MI Interface MDIO Interrupt Pulse Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	MDCK to MDIO Interrupt Pulse Asertion Delay	10			ns	
T_2	MDCK to MDIO Interrupt Pulse Deassertion Delay	10			ns	

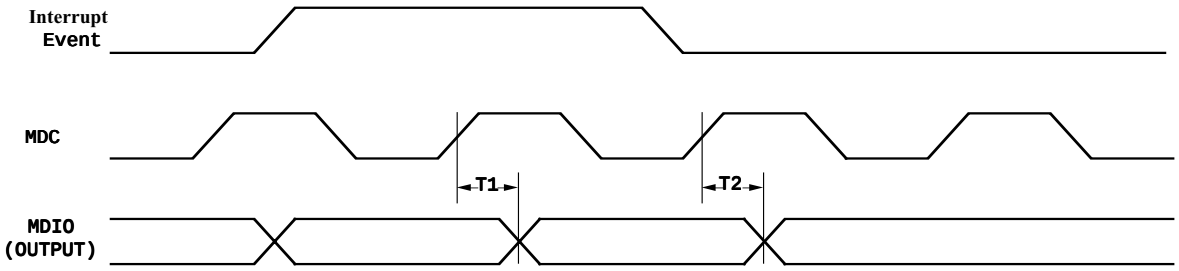


Figure 7. MI Interface MDIO Interrupt Pulse Timing

Table 9. LED On / Off Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	LED[3:0] On Time		68		ms	
T_2	LED[3:0] Off Time		68		ms	

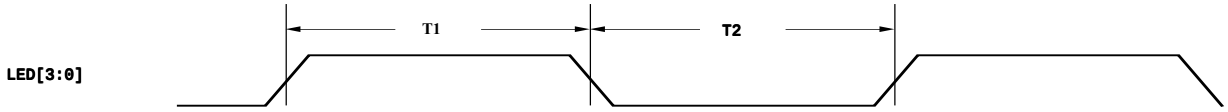


Figure 8. LED On / Off Timing

Table 10. MII Transmit Data Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	TXD[3:0], TXEN, TXER Setup to TXC	10			ns	
T_2	TXD[3:0], TXEN, TXER Hold from TXC	0			ns	

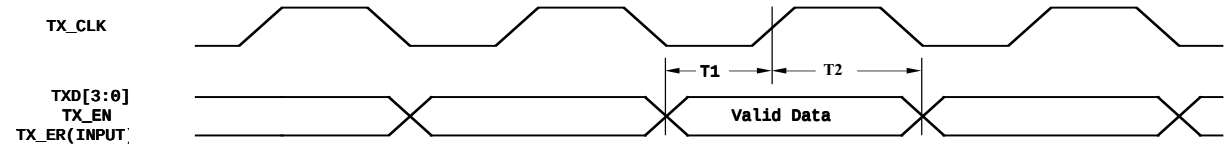


Figure 9. MII Transmit Data Timing

Table 11. MII Receive Data Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	RXD[3:0], RXDV, RXER to RXC Output Delay			25	ns	
T_2	RXC Clock Period		40		ns	

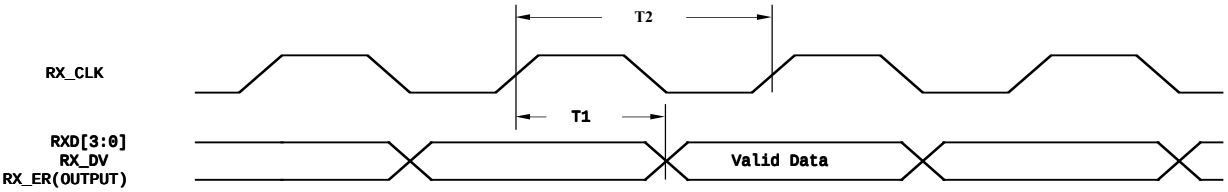


Figure 10. MII Receive Data Timing

Table 12. MII Heartbeat Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	COL Heartbeat Delay		900		ns	
T_2	COL Heartbeat Duration		1000		ns	

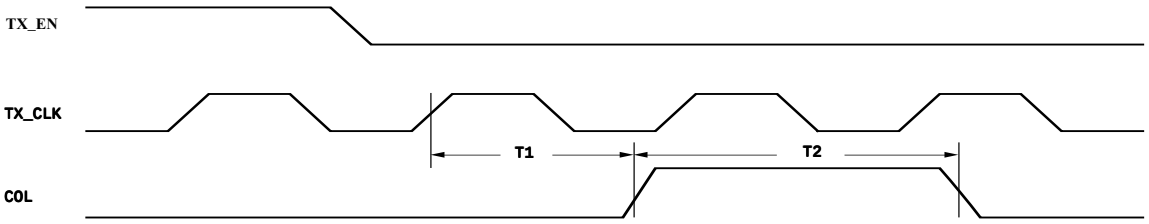


Figure 11. MII Heartbeat Timing

Table 13. MII Jabber Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	Jabber Activation Time		20	150	ms	
T_2	Jabber Deactivation Time		490		ms	

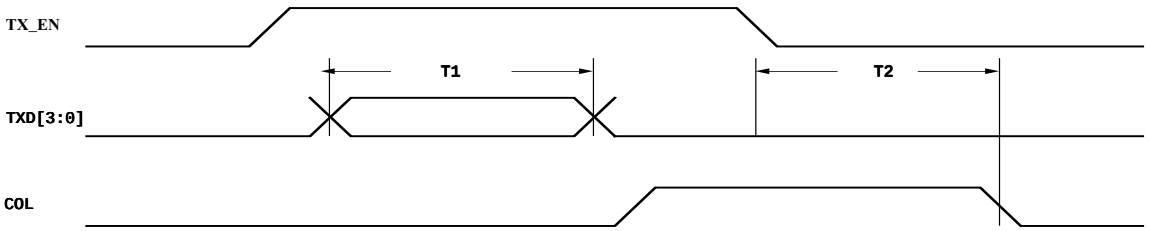


Figure 12. MII Jabber Timing

Table 14. MII 10Base-T Normal Link Pulse Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	Clock, Data Pulse Width		100		ns	
T_2	Link Pulse to Link Pulse Period		8		ms	

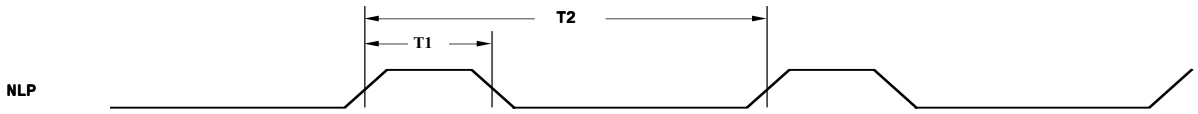


Figure 13. MII Normal Link Pulse Timing

Table 15. MII Auto-Negotiation Fast Link Pulse Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	Clock, Data Pulse Width		100		ns	
T_2	Clock Pulse to Clock Pulse Period		125		us	
T_3	Clock Pulse to Data Pulse Period		62.5		us	
T_4	Burst Width		2		ms	
T_5	FLP Burst to FLP Burst Period		8		ms	

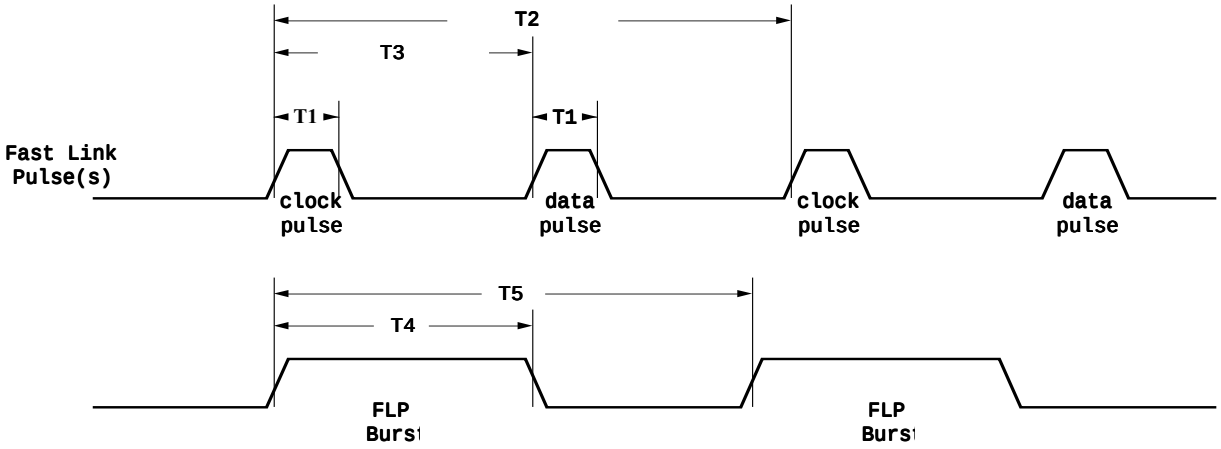


Figure 14. MII Auto-Negotiation Fast Link Pulse Timing

Table 16. 100Mb/s Receive Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	Carrier Sense On Delay		100		ns	
T_2	Receive Data Latency		160		ns	

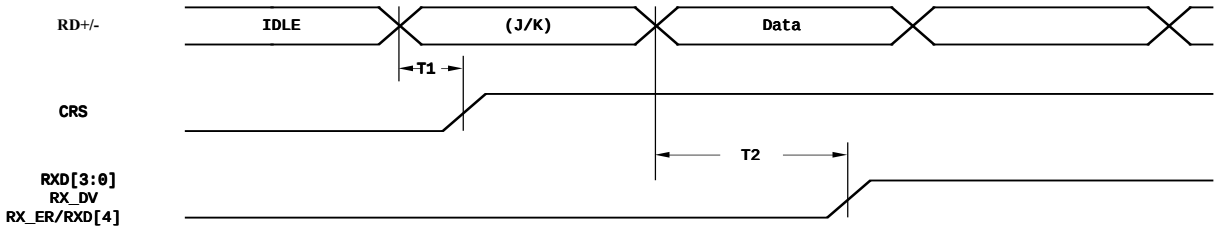


Figure 15. 100Mb/s Receive Packet Timing

Table 17. 100Mb/s Transmit Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	TXC to TX+/– Latency			120	ns	
T_2	TXC to TX+/– Deassertion			120	ns	

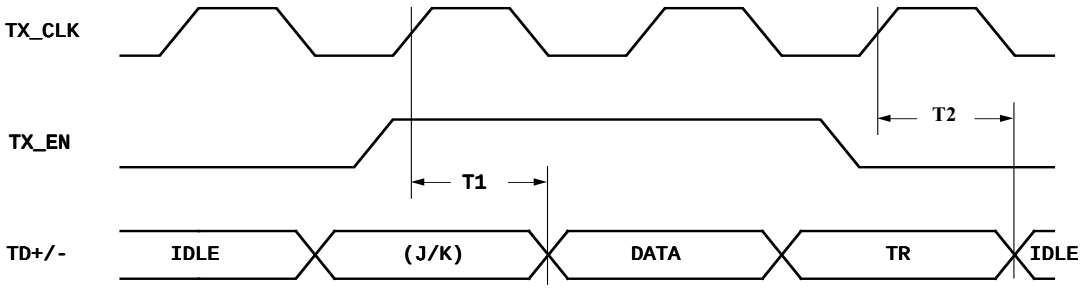


Figure 16. 100Mb/s Transmit Packet Timing

Table 18. 10Mb/s Receive Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	Carrier Sense On Delay		550		ns	
T_2	Receive Data Valid Delay		2200		ns	
T_3	Receive Data Latency		750		ns	

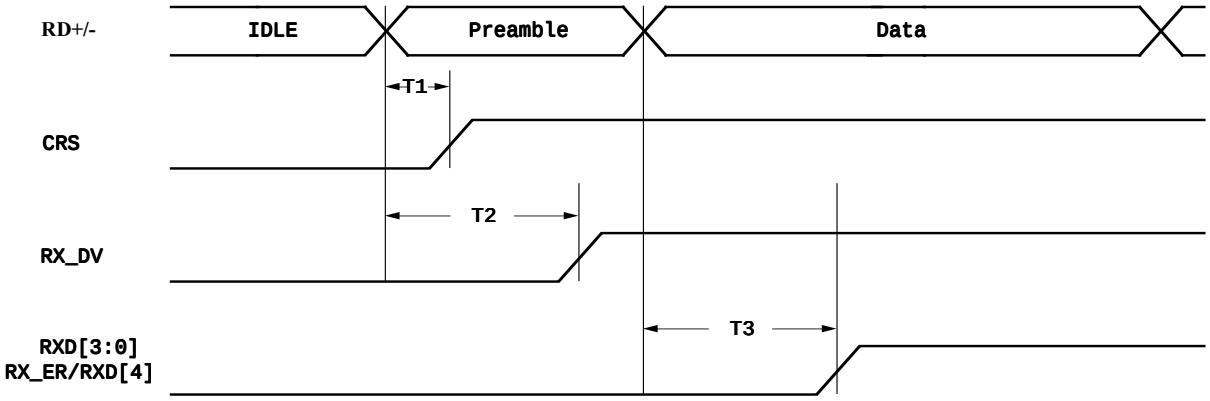


Figure 17. 10Mb/s Receive Packet Timing

Table 19. 10Mb/s Transmit Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T_1	TXC to TX+/– Latency		470		ns	
T_2	TXC to TX+/– Deassertion		700		ns	

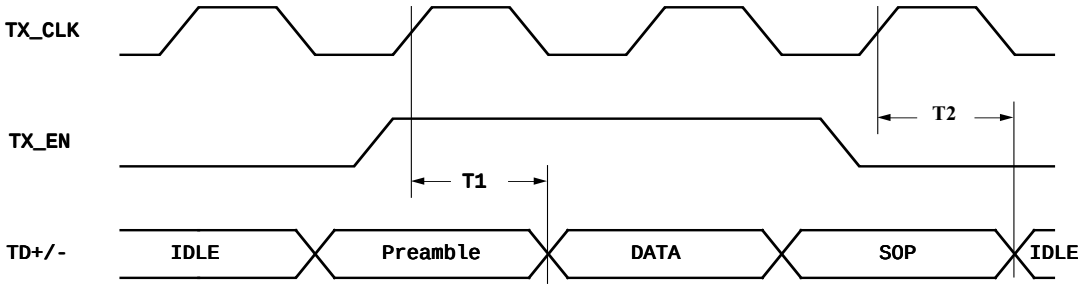
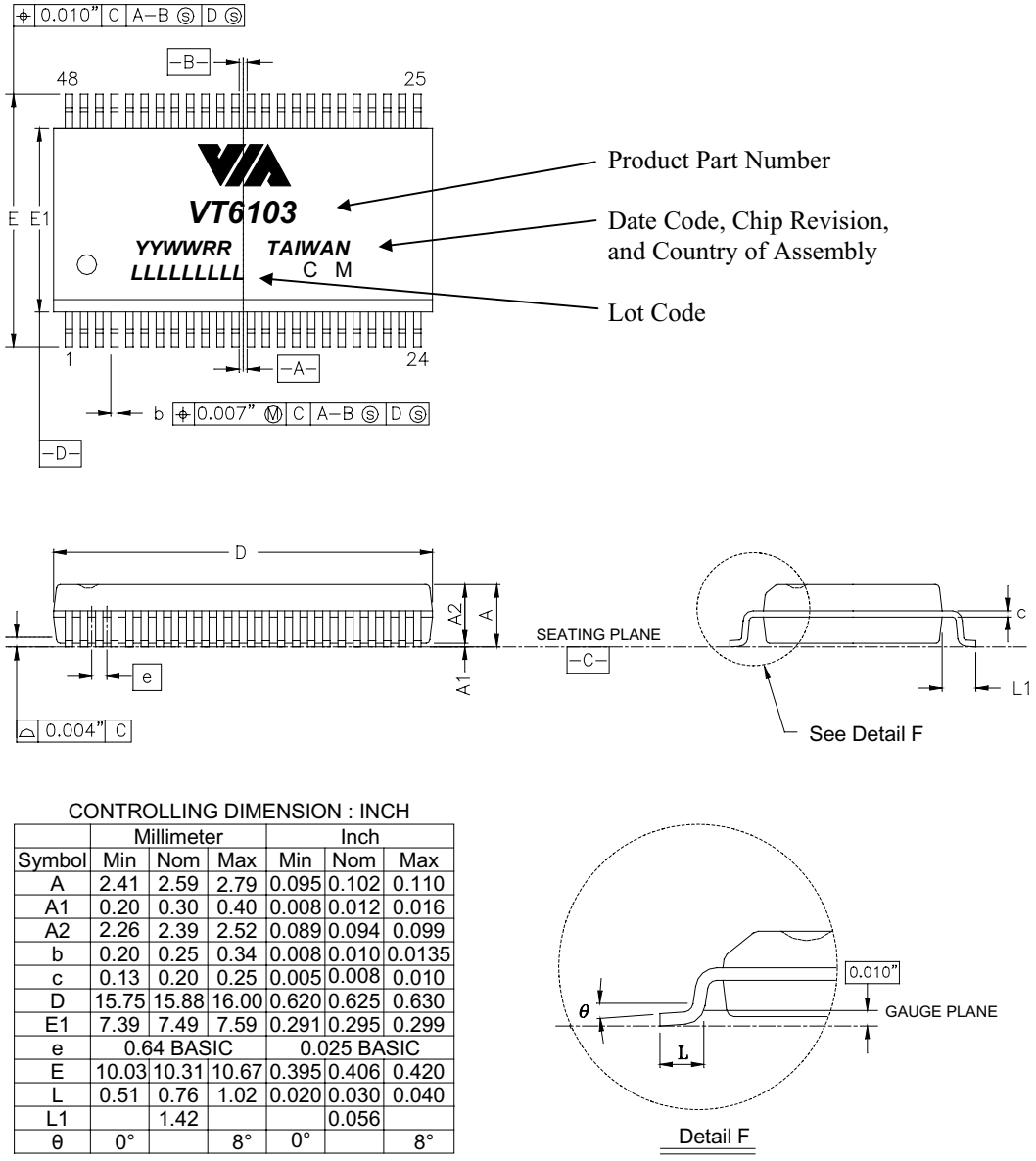


Figure 18. 10Mb/s Transmit Packet Timing

PACKAGE MECHANICAL SPECIFICATIONS



CONTROLLING DIMENSION : INCH

	Millimeter			Inch		
Symbol	Min	Nom	Max	Min	Nom	Max
A	2.41	2.59	2.79	0.095	0.102	0.110
A1	0.20	0.30	0.40	0.008	0.012	0.016
A2	2.26	2.39	2.52	0.089	0.094	0.099
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	0.20	0.25	0.005	0.008	0.010
D	15.75	15.88	16.00	0.620	0.625	0.630
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	0.64 BASIC			0.025 BASIC		
E	10.03	10.31	10.67	0.395	0.406	0.420
L	0.51	0.76	1.02	0.020	0.030	0.040
L1		1.42			0.056	
θ	0°		8°	0°		8°

Figure 19. Mechanical Specifications – 48 Pin SSOP Package