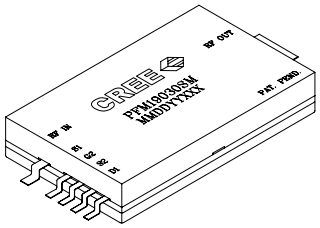
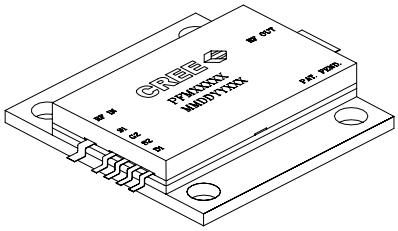
PFM19030 SPECIFICATION

1930-1990 MHz, 30W, 2-Stage Power Module
Enhancement-Mode Lateral MOSFETs



Package Type: Surface Mount

PN: PFM19030SM



Package Type: Flange

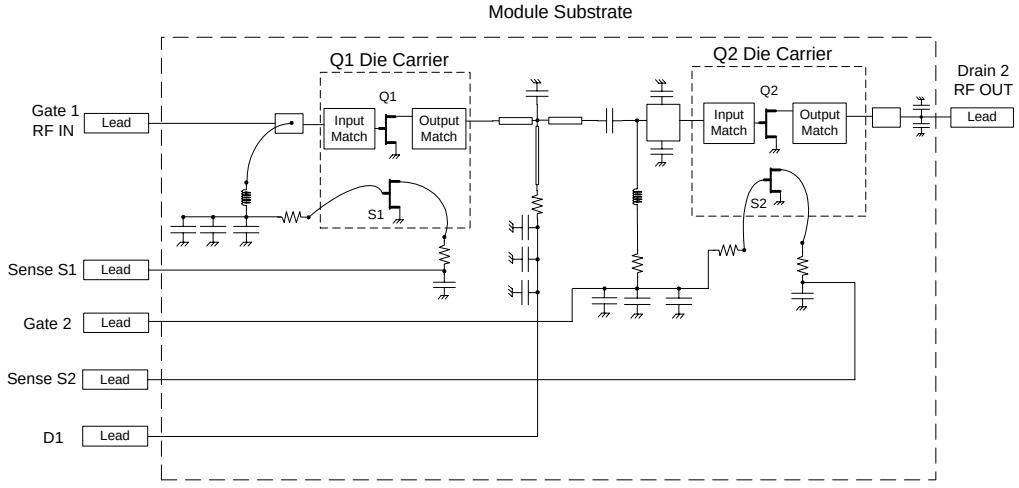
PN: PFM19030F

This versatile PCS module provides excellent linearity and efficiency in a low-cost surface mount package. The PFM19030 includes two stages of amplification, along with internal sense FETs that are on the same silicon die as the RF devices. These thermally coupled sense FETs simplify the task of bias temperature compensation of the overall amplifier. The module includes RF input, interstage, and output matching elements. The source and load impedances required for optimum operation of the module are much higher (and simpler to realize) than for unmatched Si LDMOS transistors of similar performance.

The surface mount package base is typically soldered to a conventional PCB pad with an array of via holes for grounding and thermal sinking of the module. Optimized internal construction supports low FET channel temperature for reliable operation.

- 28 dB Gain
- 30 Watts Peak Output Power
- Internal Sense FETs
  (for improved bias control)
- IS95 CDMA Performance
  5 Watts Average Output Level
  20% Power Added Efficiency
  –49 dBc ACPR

Module Schematic Diagram



Note: Additionally, there are 250 KOhm resistors connected in shunt with all leads, to enhance ESD protection.

Electrical Specification

	Parameter	Limits			Units	Comments
		Min	Typ	Max		
1	Operating Frequency	1930	-	1990	MHz	
2	Gain	27.0	29.0	31.5	dB	Note 1.
3	Gain Compression at Pout =30 Watts	-	0.8	1.5	dB	Pulsed CW compression measurement (12 µsec pulse, 120 µsec period, 10% duty cycle).
4	Gain Flatness over any 30 MHz bandwidth	-	± 0.2	± 0.3	dB	
5	Deviation from Linear Phase over any 30 MHz bandwidth	-	± 0.8	± 1.5	°	
6	Group Delay	-	3.1	3.7	nanosec	Includes delay of test fixture (~0.6 nanosec.).
7	ACPR with IS95A CDMA Pave = 5 W	-45	-49	-	dBc	Note 3. Refer to applications data for performance with other protocols.
8	Efficiency under IS-95 Protocol, Pave = 5 W	18	20.5	-	%	Note 3.
9	Efficiency @ 30W CW Output		42	-	%	
10	DC Drain Supply Voltage	24	27	30	Volts	Testing for conformance with RF specifications is at +27 V.
11	Operating Temperature Range (base temperature)	-40	-	+115	°C	Testing for conformance with RF specification is at +25 °C.
12	Gain Variation versus Temperature	-	-0.033	-	dB/°C	Bias quiescent currents held constant.
13	Output Mismatch Stress	-	-	30	Watts CW	VSWR 10:1, all phase angles. No degradation in output power before & after test.
14	Stability	-60	-	-	dBc	0<Pout<44.8 dBm CW, 3:1 VSWR
15	Theta jc (channel)	-	1.9	2.1	°C/W	Theta jc is for output device. Verified with IR scan. Note 2.
16	Quiescent Currents a) Q1 b) Q2		 75 260		 mA mA	These DC quiescent currents are typical of the levels that produce optimum linearity for CDMA protocol.
17	Sense FET Current/RF FET Current Ratio a) Stg 1 Sense b) Stg 2 Sense		 3.0 1.7		 % %	Ratio of sense FET current, relative to RF FET current. Ratios are: Stg 1: 33:1; Stg 2: 58:1 Gates of sense & RF FETs are DC connected. Measured with no RF signal present.
18	ESD Protection a) Human Body Model b) Machine Model	 Class 1 Class M3				 a) 2000V, 100 pF, 1500 Ohms b) 400V, 200 pF, zero Ohms Mil STD 883E, Method 3015 for Human Body Model and for Machine Model.

Electrical Specification (Continued)

MAXIMUM RATINGS

	Rating	Symbol	Value	Units
19	DC Drain Supply a) Drain-to-Source Voltage, (V_{GS}=0), D1 & D2 & Track D1 & Track D2 b) Normal Operation (Class AB operation)	V_{DS} V_{D_SUPPLY}	+50 +30	Volts DC Volts DC
20	DC Gate Supply a) Gate-to-source Voltage (V_{DS}=0) Normal Operation (Class AB operation)	V_{GS} V_{G_SUPPLY}	$-0.5<V_{GS}<+15$ $0<V_{GS}<+6$	Volts DC Volts DC
21	RF Input Power	P_{IN}	+25	dBm
22	Maximum Power Dissipation (T ≤ +85 °C) a) Derate above +85 °C base temperature.	P_{TOTAL}	65 -0.7	Watts Watts/°C
23	Maximum Channel Operating Temperature	T_{CH}	+200	°C
24	Storage Temperature Range	T_{STG}	-40 to +150	°C

RECOMMENDED SOURCE AND LOAD IMPEDANCES

	Impedance	Units	Comments
Nominal Source Impedance for Optimum Operation	19 + j1.9	Ohms	Matched for near-optimum linearity and gain flatness. Impedance is looking from the module input lead into the input matching circuit. Reference plane is 0.105 inches from the input end (case edge)of the module.
Nominal Load Impedance for Optimum Operation	21 + j6.3	Ohms	Matched for near-optimum linearity under CDMA protocol. Impedance is from the module output lead looking into the output matching circuit. Reference plane is 0.105 inches from the output end (case edge) of the module.

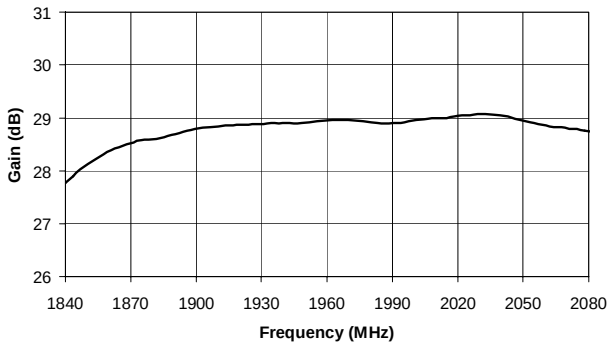
Specification Notes:

1) The module is mounted in a test fixture with external matching elements for all testing. Quiescent current bias conditions are those appropriate for minimum ACPR under CDMA protocol. Supply voltage for all tests is +27 volts DC. Testing is at +25 °C unless otherwise specified.
2) Theta jc is measured with a package mounting (base) temp of +85 °C, and with 10 Watts CW output.
3) Pout=5Watts average; IS-95A protocol: IS95 Forward Link PPS+ 9CH.
   ACPR conditions: a) 900 kHz offset, 30 kHz BW, b) 2.75 MHz offset, 1 MHz BW.
4) Sense FETs are scaled versions of the main RF FETs, formed from electrically isolated cells at end of the RF structure. Current scales according to periphery (threshold voltages offset is less than ±150 millivolts between adjacent devices). RF & Sense FET gates and sources are DC connected. Drains are DC isolated. Leads S1 & S2 are DC connected to drains of sense FETs 1 & 2. Sources are connected to package base. Sense FETs are electrically isolated from the RF signals.

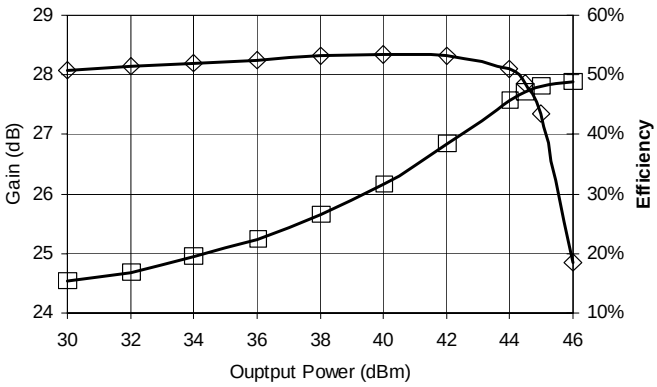
Typical Module Performance

T=+25 °C, unless otherwise noted. Data is for module in a test fixture with external matching elements. See following page for test fixture details.

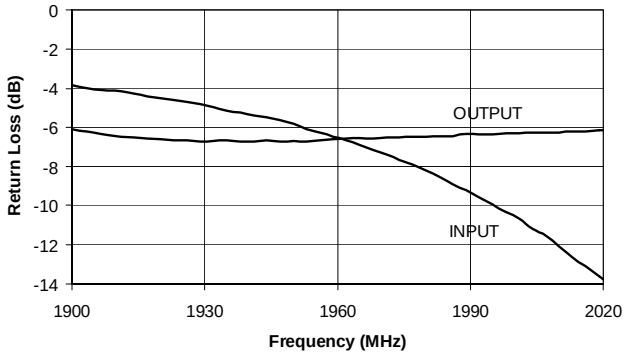
Typical Small-Signal Gain vs. Frequency



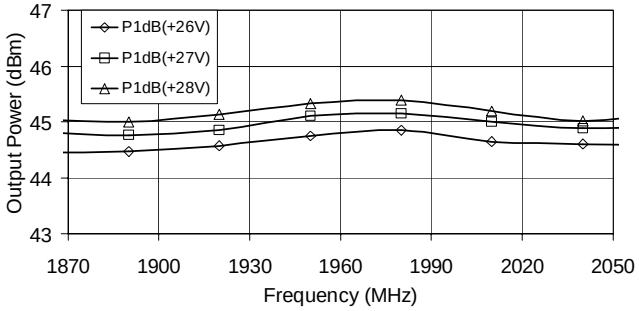
Gain & Efficiency vs. Output Power
Pulsed Measurement, Vdc=+27V, F=1960 MHz



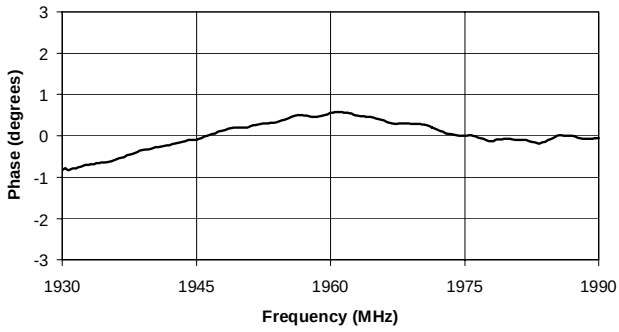
Input and Output Return Loss vs Frequency.



Typical Output Power at 1 dB Gain Compression vs Freq. & Supply Voltage

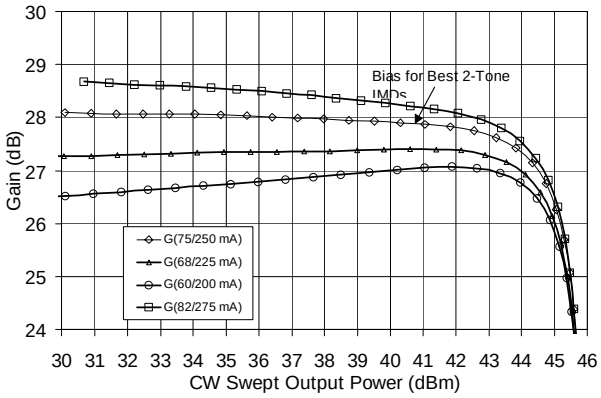


Typical S21 Phase Variation Versus Frequency
(normalized about average insertion phase)



Time delay offset = 3.2 nanosec (includes time delay of test fixture).

Typical CW Gain vs Swept CW Output Power, with Various Quiescent Bias Conditions

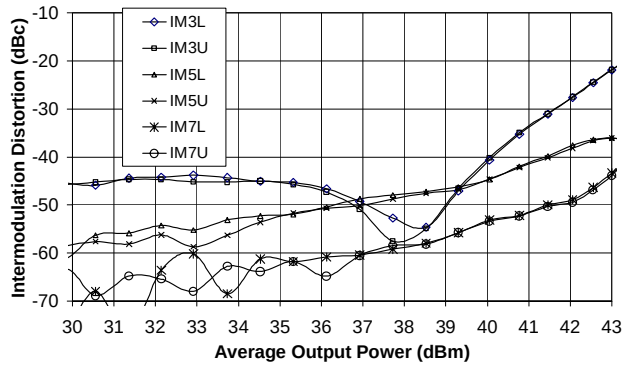


Note: This data illustrates the significance of quiescent bias current level. The unit was press mounted in the fixture & thermal effects are exagerated for this CW test.

Typical Module Performance

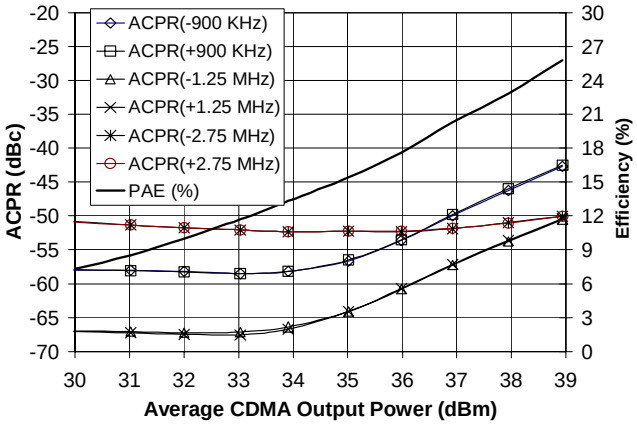
T=+25 °C, unless otherwise noted. Data is for module in a test fixture with external matching elements. See following page for test fixture details.

Typical CW 2-Tone Intermods vs. Output Power

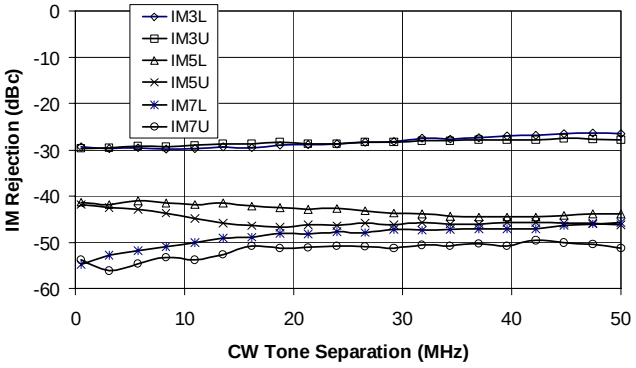


F1=1959.5 MHz, F2=1960.5 MHz
Vsupply = +27 V, Idsq1 = 75 mA, Idsq2=250 mA

Single-Signal IS95 CDMA ACPR & Efficiency vs Average Output Power (F=1960 MHz)

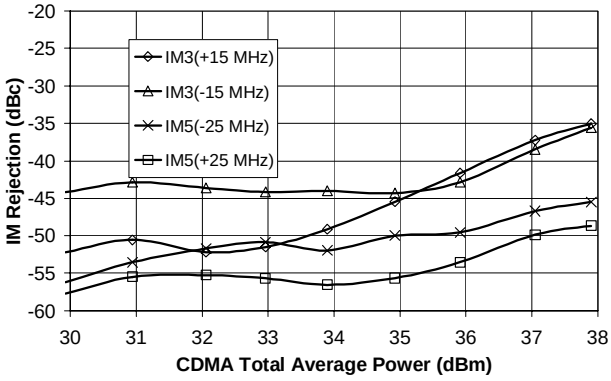


2-Tone IMD Rejection vs. Tone Separation (Peak Envelope Power = 44.5 dBm)

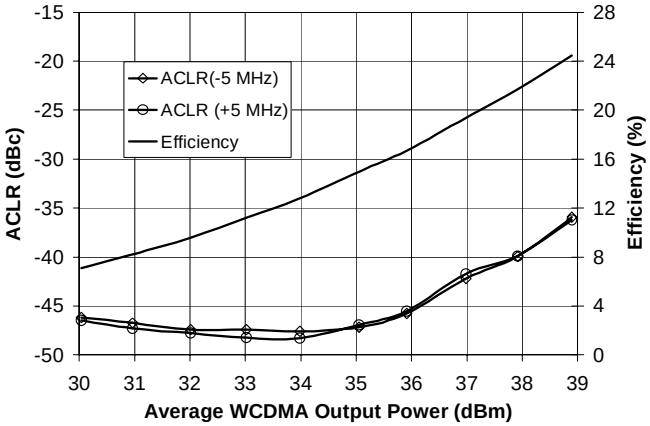


F1=1930 MHz, F2=1930.5 MHz to 1980 MHz
Vsupply = +27 V, Idsq1 = 75 mA, Idsq2=250 mA

2 IS95 CDMA Signal IM Distortion vs. Ave Output Power (F=1955, 1965 MHz)



WCDMA ACLR & Efficiency vs Output Power (F=1960 MHz, Test Model 1)

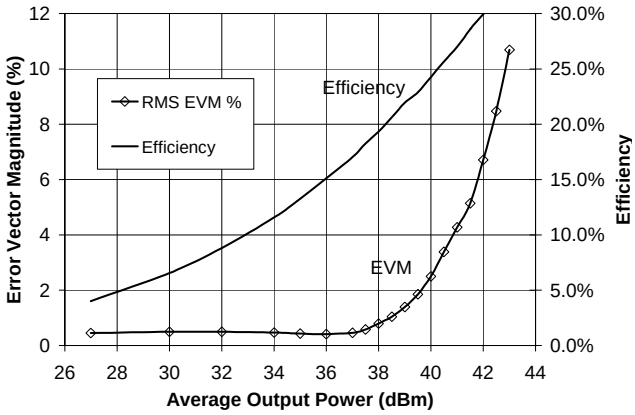


PFM19030

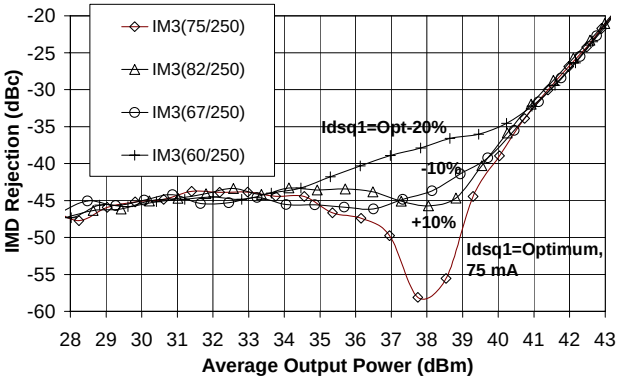
Typical Module Performance

T=+25 °C, unless otherwise noted. Data is for module in a test fixture with external matching elements. See following page for test fixture details.

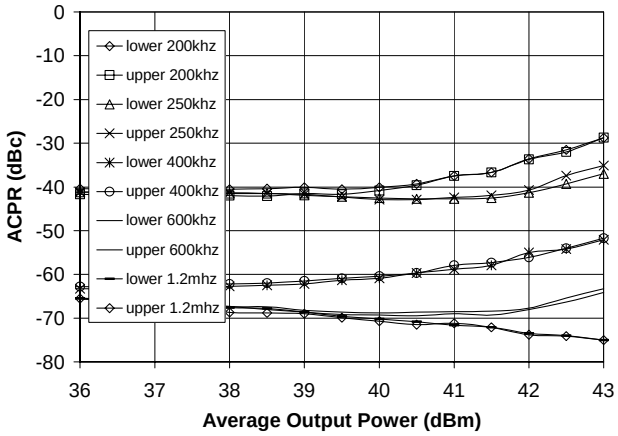
EDGE EVM & Efficiency vs. Pout



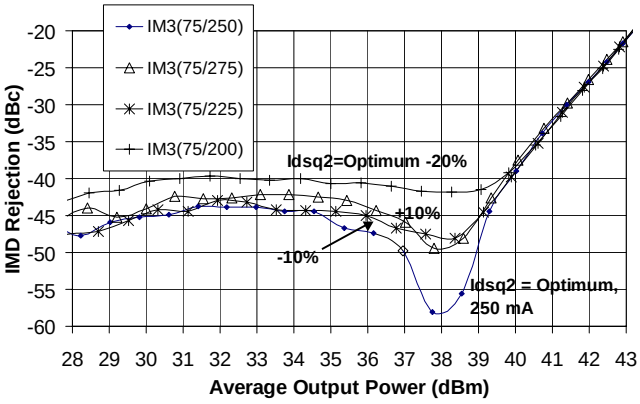
2-Tone 3rd Order IMD Rejection vs. Pout & First Stage Quiescent Bias Currents



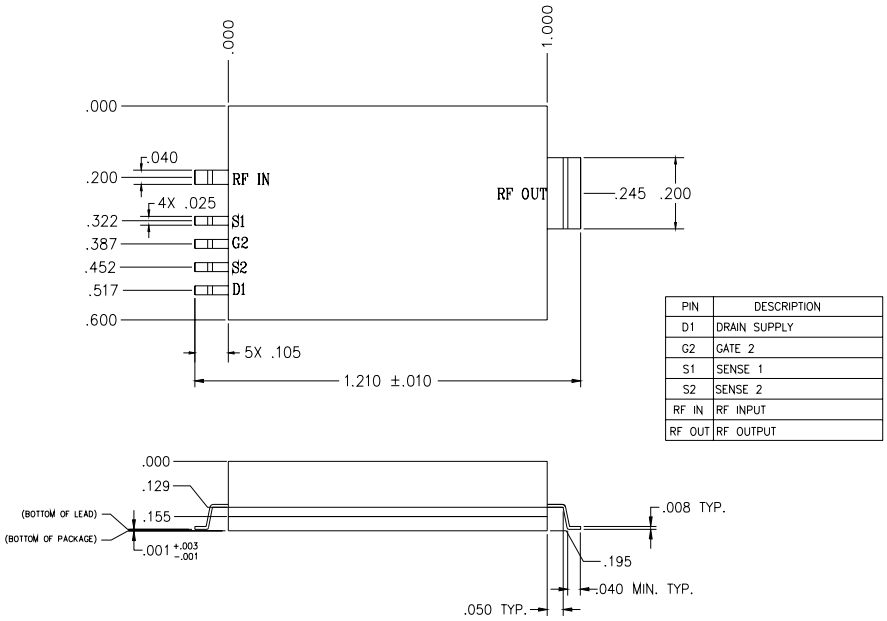
EDGE ACPR vs. Average Pout



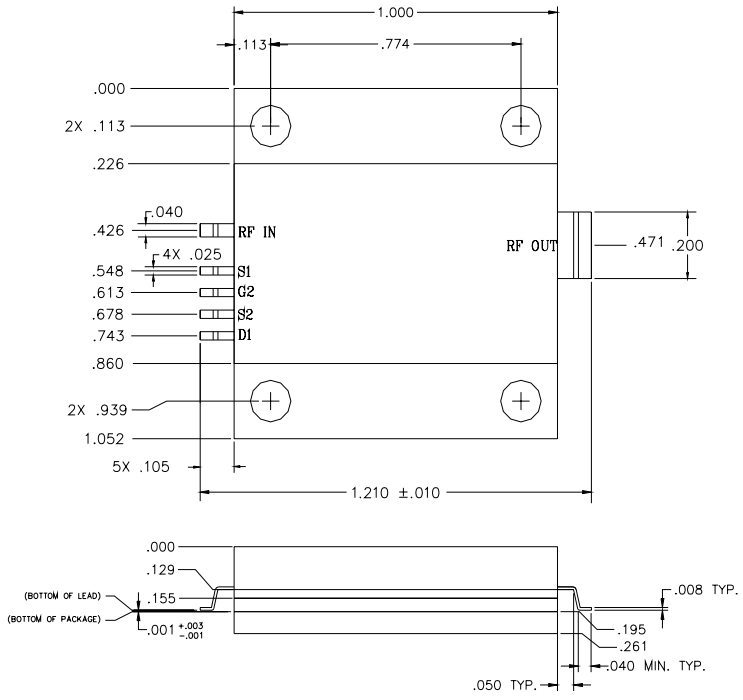
2-Tone 3rd Order IMD Rejection vs. Pout & Second Stage Quiescent Bias Currents



PFM19030SM Package Outline



PFM19030F Package Outline



Module Application Notes

The PFM19030 was designed to provide a versatile low cost solution for a wide variety of wireless applications requiring 30 Watt peak output levels. This hybrid module contains two stages of Si LDMOS FET amplification: a nominally 5 Watt input stage driving a 30 Watt output stage. The module is optimized for efficient, linear operation with EDGE and CDMA signals. The input and output of this module are partially matched, and require source and load impedances of nominally 19 and 21 Ohms (much higher than typically required by unmatched Si LDMOS FETs). These source and load impedances can be achieved with compact conventional external PCB circuitry.

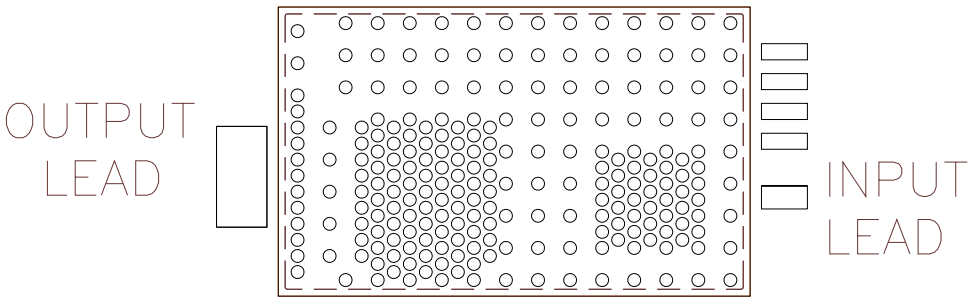
Performance for particular signal protocols can be improved slightly by small adjustments in quiescent currents and load impedances presented to the module. The data presented in the previous pages was taken at one set of quiescent currents and in a fixture with source and load impedances that were fixed for all measurements. The data presented is generally representative of the performance – benefits from further optimization in quiescent current are small.

In addition to the two RF gain stages, there are Sense FET (thermally tracking) devices that serve as optional DC circuit elements. The Sense FETs are fabricated on the same epi material with nominally identical physical characteristics (but smaller gate periphery) as the RF devices. The sense devices can be applied as temperature compensation elements in conjunction with external bias circuitry. Alternatively, the two-stage amplifier can be operated with the Sense FETs unused (S1 and S2 leads floating).

The base of the module is high conductivity copper of 40 mil thickness. It is well matched to typical PCB material, and it serves as a heat spreader for the device when mounted as a surface-mount component. The module thermal characteristics were measured with the unit soldered to a 20 mil thick PCB material with an array of plated via holes for electrical grounding and thermal sinking. IR scans of this configuration demonstrated maximum die channel temperatures of 142 degrees C with a PCB base temperature of +95 degrees C, and 10 Watts CW output power.

These modules can be provided in tape-and-reel configuration for high volume applications.

Typical PCB Mounting Pattern

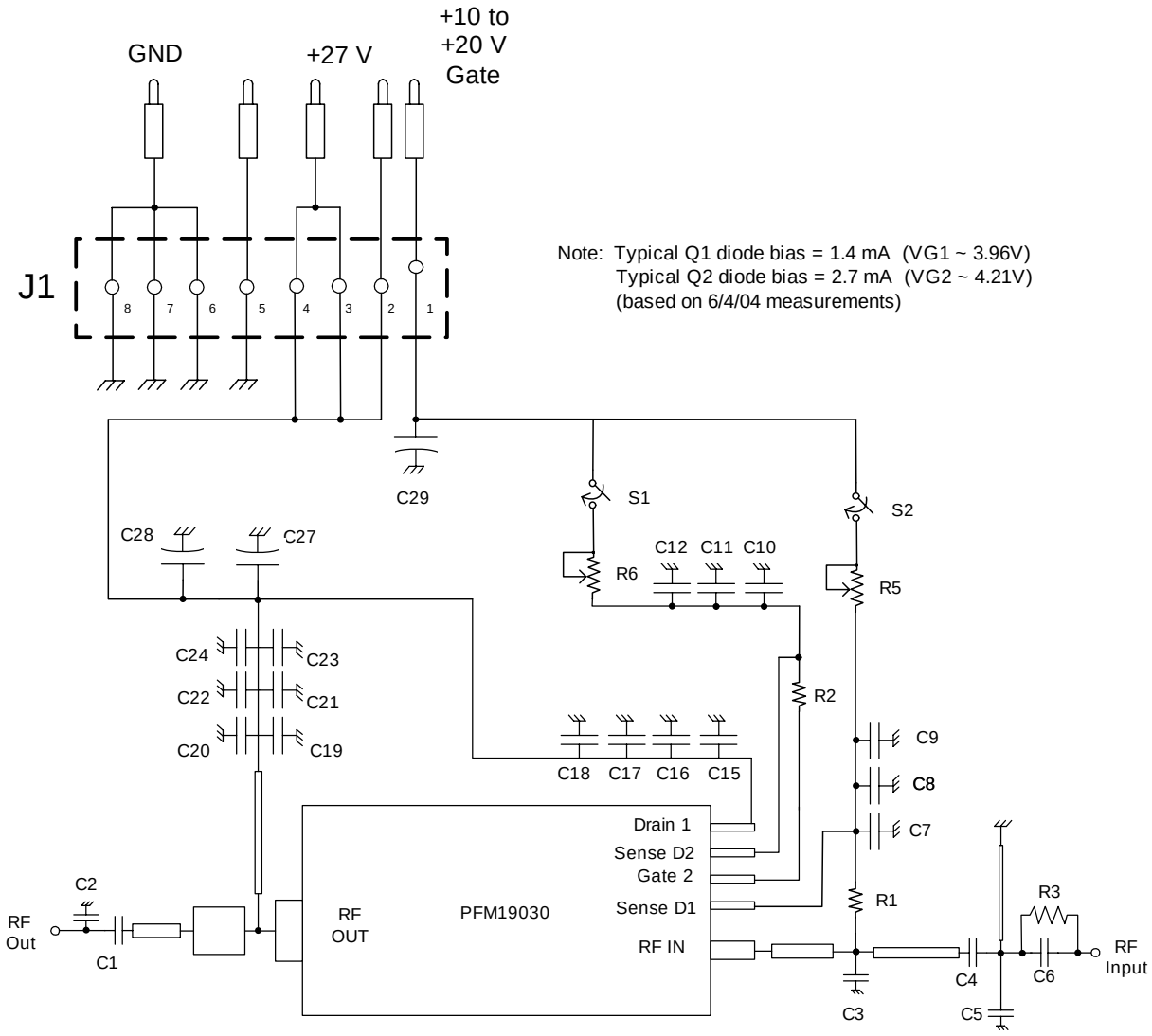


The module outline is indicated by dashed line (0.60 X 1.00 inches). The ground pad is 1.030 X 0.630 inches. Ground vias in this example are 28 mil diameter on 35 mil (or 70 mil) centers. Thermal resistance is proportional to the thickness of the PC board (height of vias), and inversely proportional to the total ground hole array periphery (and thickness of plating in the holes). The densely spaced vias in this layout (on 35 mil spaces) are located in areas of maximum heat generation. The gap between the lead pads and the ground pad is 25 mils. Note that the underside of the PCB must be connected to a thermal heat sink and ground.

The above hole pattern is an example of one that maximizes thermal transfer. There are numerous alternative approaches. Depending on the application (signal protocol, thermal environment, etc.), the number of via holes can be reduced. High average power applications require the most extensive thermal sinking.

Recommended Passive Bias Circuit

This schematic demonstrates a method of applying the Sense FETs internal to the module that uses passive external circuitry. The circuit maintains a constant current through the Sense FETS, independent of temperature of the die. The Sense FETs are configured in this case as diodes. The temperature dependence of the Vf of the diode is very similar to that of the RF FET gate voltage, and therefore the quiescent current remains nearly constant over a wide temperature range. The advantage of this circuit is its simplicity and stability (avoidance of operational amplifiers) under all layout conditions. The main limitation of the circuit is that quiescent currents must be adjusted for each individual module (they are not easily pre-set with precision).

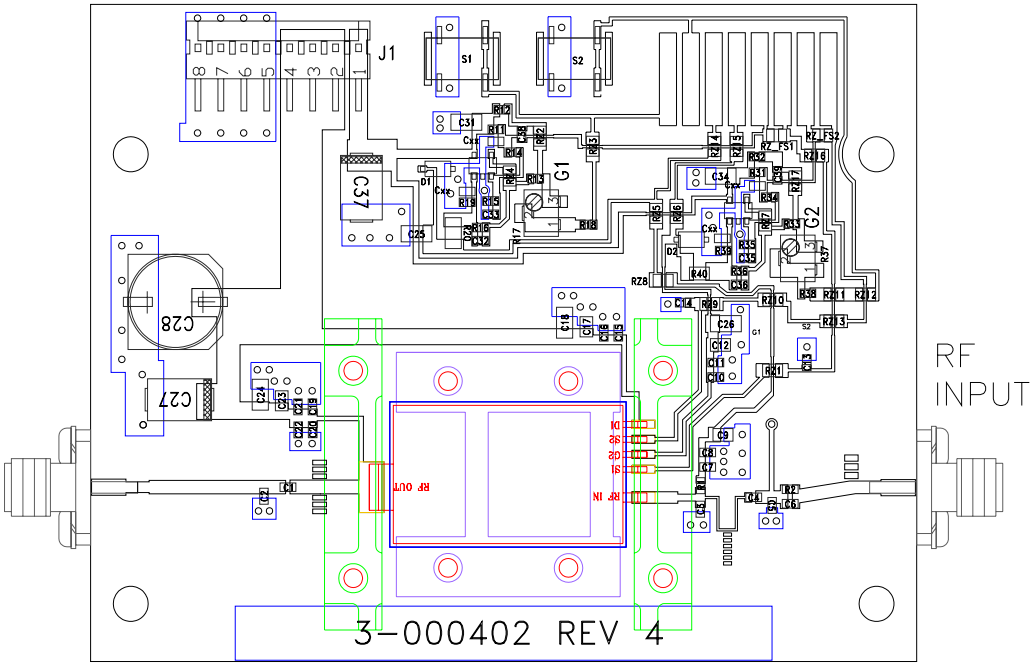


Passive Bias Circuit Parts List

Designator	Description	Qty
C2	CAP, 1.2 PF±0.1 pF, 0603, ATC 600S	1
C3	CAP, 2.0 PF±0.1 pF, 0603, ATC 600S	1
C5	CAP, 1.8 PF±0.1 pF, 0603, ATC 600S	1
C4	CAP, 4.7 PF±0.1 pF, 0603, ATC 600S	1
C6	CAP, 3.0 PF±0.1 pF, 0603, ATC 600S	1
C1, C7, C19, C20	CAP, 27 PF±5%, 0603, ATC 600S	4
C10, C13, C14, C15,	CAP, 27 PF±5%, 100V (min), 0603, any vendor.	4
C8, C11, C16, C21	CAP, 470 PF ±10%,100 V, 0603, any vendor.	4
C22	CAP, 3300 PF±10%, 100 V, 0603, Murata GRM39X7R332K100??, or equivalent.	1
C23, C9, C17, C12	CAP, 15000 PF±10%, 100 V, 0805, MurataGRM40X7R153K100??, or equivalent.	4
C24, C18	CAP, 150000 1206, 50V, X7R, 10% Suggest Murata GRM42-6-X7R-154-K-050-A-L or equivalent.	2
R5	RES, potentiometer, 10Kohms, Digikey SM4W103-ND	1
R6	RES, potentiometer, 5 Kohms, Digikey SM4W502-ND	1
R1	RES, 1/16W, 0603, 1000 ohms, 5%	1
R3	RES, 1/16W, 0805, 124 Ohms, 5%	1
C27	CAP, 2.2uf SMT TANTALUM, 50V (240097)	1
C29	CAP, 10uf 16V SMT TANTALUM (240096)	1
C28	CAP, 47UF, 50V, ELECTR SMT (240087)	1
S1, S2	SPST Switch, Digikey PN CKN1100CT-ND	2

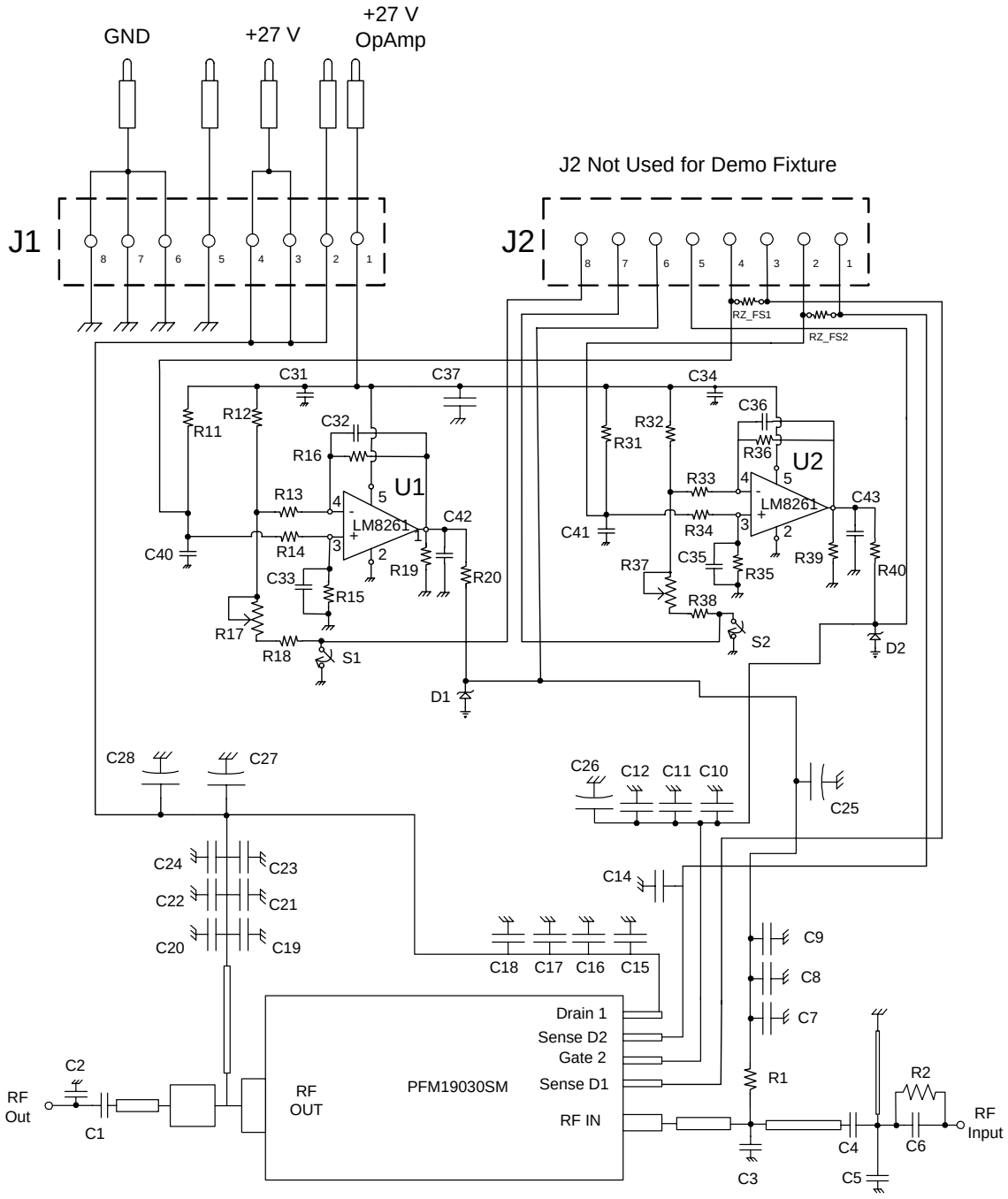
Test Fixture

A metal-backed PCB with clamps for securing the module is used for module electrical testing and for product demonstration. The fixture is supplied mounted to a finned heat sink. The fixture schematic is provided on the following page.



This test fixture uses an active bias circuit, which sets the bias circuit through the Sense FETs (configured as FETs) and applies the derived gate voltage to the associated RF FETs. This assures particular quiescent bias currents, with accuracy determined by the Sense FET-to-RF FET current ratios.

Test Fixture Schematic



See the following pages for the parts list and a description of the principle of operation. Note that an alternative, less complex bias scheme is provided later in this applications note. The advantage of the above bias design is that bias currents are set by the RF-to-Sense FET ratios, and once the optimum bias circuit resistor (potentiometer) values are established, the circuit can stay fixed for multiple modules (thus eliminating module-specific bias alignment). Additionally, aging effects are minimized because of the

similar bias conditions for Sense and RF FETs. The disadvantage of this design is its relative complexity and the incorporation of operational amplifiers, for which stability is potentially circuit layout dependent.

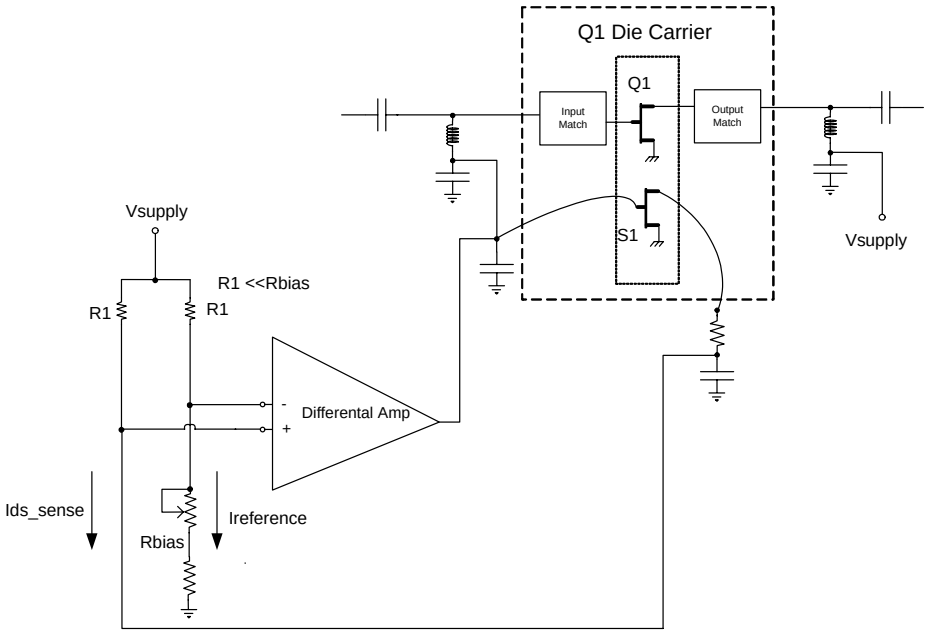
Parts List for Cree Microwave Test Fixture

Designator	Description	Qty
C2	CAP, 1.2 PF±0.1 pF, 0603, ATC 600S	1
C3	CAP, 2.0 PF±0.1 pF, 0603, ATC 600S	1
C5	CAP, 1.8 PF±0.1 pF, 0603, ATC 600S	1
C4	CAP, 4.7 PF±0.1 pF, 0603, ATC 600S	1
C6	CAP, 3.0 PF±0.1 pF, 0603, ATC 600S	1
C1, C7, C19, C20	CAP, 27 PF±5%, 0603, ATC 600S	4
C10, C13, C14, C15,	CAP, 27 PF±5%, 100V (min), 0603, any vendor.	4
C8, C11, C16, C21	CAP, 470 PF ±10%,100 V, 0603, any vendor.	4
C22	CAP, 3300 PF±10%, 100 V, 0603, Murata GRM39X7R332K100	1
C9, C23, C17, C12	CAP, 15000 PF±10%, 100 V, 0805, MurataGRM40X7R153K100	4
C18, C24, C25, C26, C31, C34	CAP, 150000 1206, 50V, X7R, 10% Murata GRM42-6-X7R-154-K-050-A-L	6
C27, C37	CAP, 2.2uf SMT TANTALUM, 50V	2
C28	CAP, 47UF, 50V, ELECTR SMT	1
C33, C35	CAP, 18,000 PF ±10%,100 V, 0603	2
C32, C36	CAP, 33,000 PF ±10%,100 V, 0603	2
C40, C41, C42, C43	CAP, 1000 PF ±10%,100 V, 0603.	4
R1	RES, 1/16W, 0603, 1000 ohms, 5%	1
R2	RES, 1/16W, 0805, 124 Ohms, 5%	1
R11, R12	RES, 1/16W, 0603, 332 Ohms, 1%	2
R31, R32	RES, 1/16W, 0603, 147 Ohms, 1%	2
R13, R14, R33, R34	RES, 1/16W, 0603, 2370 Ohms, 1%	4
R16, R15, R35, R36	RES, 1/16W, 0603, 511 KOhms, 1%	4
R19, R39	RES, 1/16W, 0603, 100 KOhms, 5%	2
R18	RES, 1/16W, 0603, 3320 Ohms, 5%	1
R38	RES, 1/16W, 0603, 2000 Ohms, 5%	1
R20, R40	RES, 1/8W, 1206, 1000 Ohms, 5%	2
R17, R37	RES, potentiometer, 10 Kohms, Digikey SM4W103-ND, 11T	2
RZ_FS1, RZ_FS2	RES, 1/16W, 0805, 0 Ohms (used as jumpers, demo fixture only)	2
D1, D2	Zener diode, 6.2 V, Digikey PN BZT52C6V27DICT-ND	2
S1, S2	SPST Switch, Digikey PN CKN1100CT-ND	2
U1, U2	Op Amp, High Output, LM8261M5 (5 pin, SOT23 package)	2

It is also possible to bias the two stages in a conventional manner, with the two tracking FET drains left unused (floating or grounded). The above bias circuits are just two of several possibilities.

Test Fixture Active Bias Circuit Principles of Operation

The test fixture operates off of a single voltage supply. It contains two switches and two potentiometers. The switches provide for independent on/off for the input and output devices of the module. The potentiometers allow adjustment of quiescent current level of each stage. The adjustments should be made with no RF applied to the module.



Principal of Operation of Bias Circuitry

The principal of operation of the fixture bias circuit is demonstrated in the above Figure. The potentiometer establishes a reference current, and the operational amplifier adjusts gate voltage to maintain that current in the sense device. The same DC gate voltage is also applied to the main (RF) device. Sense devices are scaled versions of the main (RF) devices, on the same die (to facilitate temperature tracking). As the temperature of the die changes due to RF drive (or ambient temperature changes), the operational amplifier maintains constant current through the Sense FET, and thus constant quiescent bias for the main (RF) FET. No RF signal is applied to the Sense FET.

There is a separate independent bias circuit for the input (Q1) device and for the output device (Q2) of the module.

Experience has shown this bias circuit to be a reliable method of maintaining tight control of quiescent current over operating temperature, and for minimizing the impact of device aging effects on amplifier performance. However, there are some precautions regarding use of this circuit. The principle of the circuit is for the differential amplifier (op amp) to adjust gate voltage until the desired current is achieved through the sense FETs. If the current path is interrupted (thereby not allowing I_{ds_sense} to flow), the operational amplifier will increase gate bias in an attempt to increase current, with the possibility that the quiescent bias current in the RF FET may increase beyond a safe limit (the device may be destroyed). The zener diodes in the test fixture circuit (D1 and D2, test fixture schematic) are safeguards for prohibiting excessive gate voltage to be applied to the transistors.

Contact Information:

Cree Microwave, Inc.
160 Gibraltar Court
Sunnyvale, CA 94089-1319

Sheryle Henson (Cree Microwave—Marketing Manager) 408-962-7783
Tom Dekker (Cree Microwave—Sales Director) 919-313-5639