

# **PBL 403 10**

# 3.5 V GSM 900 MHz Power Amplifier

#### Description.

The PBL 40310 is a highly integrated single-ended silicon MMIC power amplifier intended for use in GSM terminals. It delivers 35 dBm at 900 MHz with 55 % power added efficiency into a 50  $\Omega$  unbalanced load using a single 3.5 V supply.

The circuit has an analog ramp signal to control output power level and a logical on/ off signal for power down mode. It can be used in dual-band amplifiers using the band select logical signal. It can be operated up to 50 % duty cycle with minimum performance degradation. The circuit is housed in a specially designed QSOP16 (150 mil body) package and the implementation requires only few external components.

 $25~\mathrm{GHz}~\mathrm{f_t}$  state-of-the-art deep trench isolated double-poly silicon bipolar process with additional features for improved wireless performance has been used. On-chip capacitors and inductors are used for the integrated internal matching network. Special front-side metallized substrate contacts provide excellent ground paths from active devices to the highly doped semiconductor substrate and package ground.

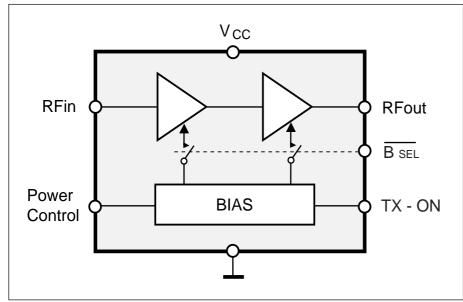


Figure 1. Block diagram.

#### Key features.

- 2.7 to 5.0 V single supply operation
- 35 dBm output power at 3.5 V
- 55 % Power Added Efficiency
- Input matched to 50  $\Omega$
- Complete on chip input and interstage matching
- Analog power control
- Less than 10 μA current consumption in power down mode
- Proven RF Silicon Technology Reliability
- Minimum number of external components for low overall solution cost



Figure 2. Package outlook.



### **Maximum Ratings**

Parameter	Conditions	Symbol	Min.	Тур.	Max.	Unit
Supply voltage, continuous		$V_{cc}$	-0.5		6.0	V
Power control voltage		$V_{APC}$	-0.5		6.0	V
Input power		P <sub>IN</sub>			+20	dBm
Operating Case Temperature		T <sub>OP</sub>	-40		+85	°C
Storage Temperature Range		T <sub>STORAGE</sub>	-30		+100	°C

#### **DC Electrical Characteristics**

 $V_{CC} = 3.5 \text{ V}, T_A = +25^{\circ}\text{C}$  unless otherwise stated.

Parameter	Conditions	Symbol	Min.	Тур.	Max.	Unit
Supply voltage range		V <sub>cc</sub>	2.7		5.0	V
Supply current	V <sub>APC</sub> = 2.5 V, no RF signal applied	I <sub>cc</sub>		150		mA
Standby supply current	V <sub>APC</sub> <=0.5 V, TX-ON=HIGH	I <sub>STBY</sub>			3.0	mA
Power down leakage current	$V_{APC} \le 0.5 \text{ V, TX-ON=LOW}$	I <sub>LEAK</sub>			5.0	μΑ
Input current, V <sub>APC</sub>	$0 < V_{APC} < 3.5 V$			2.0	3.0	mA

#### **AC Electrical Characteristics**

 $V_{\text{CC}} = 3.5 \text{ V, } \\ f_{\text{IN}} = 900 \text{ MHz, } \\ P_{\text{IN}} = 8 \text{ dBm, } \\ V_{\text{APC}} = 2.5 \text{ V, TX-ON} = \\ \text{high (V}_{\text{CC}}), \\ \overline{\text{Bsel}} = \\ \text{low (GND), duty cycle} = 12.5 \text{ \%, pulse width} = 577 \\ \mu\text{s, } \\ T_{\text{A}} = +25 \\ \text{°C unless otherwise stated. All data measured on evaluation board.}$ 

Parameter	Conditions	Symbol	Min.	Тур.	Max.	Unit
Frequency range		f <sub>IN</sub>	880		915	MHz
Input impedance		Z <sub>IN</sub>		50		Ω
Input VSWR	P <sub>IN</sub> = -10 to +20 dBm	VSWR		2:1		
Recommended input power		P <sub>IN</sub>	8.0		12.0	dBm
Power gain	P <sub>IN</sub> = 0 dBm	G <sub>P</sub>	30	31		dB
Output power		P <sub>out</sub>	34.5	35		dBm
Power added efficiency		η	50	55		%
Output power	$V_{cc} = 2.9 \text{ V}$	P <sub>out</sub>		33		dBm
2 <sup>nd</sup> harmonic		2 fo		tbd		dBc
3 <sup>rd</sup> harmonic		3 fo		tbd		dBc
Output Noise	RBW=100 kHz, f=925 to 935 MHz			tbd		dBm
Output Noise	RBW=100 kHz, f=925 to 960 MHz			tbd		dBm
Forward isolation	$V_{APC}$ < 0.5 V, $P_{IN}$ = -10 to + 10 dBm			-25		dB
Stability, load VSWR	All phases, no oscillations.	VSWR			6:1	
Ruggedness, load VSWR	All phases, no damage.	VSWR			10:1	
Power control for max. $P_{\text{out}}$		$V_{\mathtt{APC}}$	2.5			V
Power control for min. P <sub>OUT</sub>	P <sub>out</sub> < -30 dBm	V <sub>APC</sub>			0.5	V
Power control slope	-10 dBm < P <sub>out</sub> < 35 dBm			tbd	tbd	dB/V

This document contains advance information of a new product. Data given in this document shall be considered as preliminary and may be changed without notice.



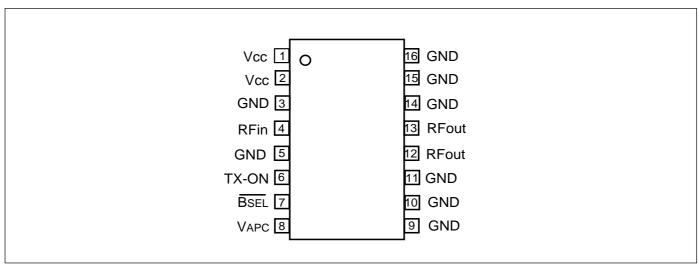


Figure 3. Pin configuration.

## **Pin Descriptions:**

Refer to pin configuration.

so	Name	Function	so	Name	Function
1	Vcc	Supply voltage	9	GND	Common ground
2	Vcc	Supply voltage	10	GND	Common ground
3	GND	Common ground	11	GND	Common ground
4	RFin	RF input	12	RFout	RF output
5	GND	Common ground	13	RFout	RF output
6	TX-ON	Transmit ON	14	GND	Common ground
7	BSEL	Band select	15	GND	Common ground
8	VAPC	Power control voltage	16	GND	Common ground

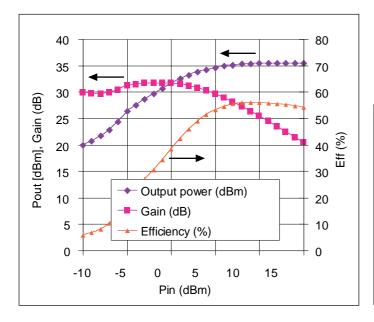


Figure 4. RF performance.

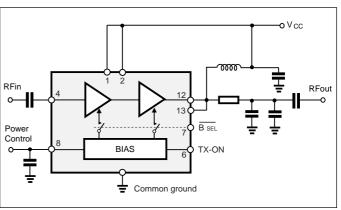
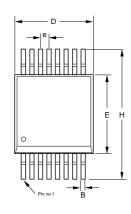


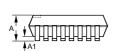
Figure 5. Evaluation setup including network for unbalanced input/output.

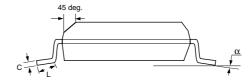


#### Package drawing, QSOP 16



Dim.	millimeters min. max.		inches min.	max.			
Α	1.35	1.75	0.532	0.688			
A1	0.10	0.25	0.004	0.0098			
В	0.21	0.31	0.008	0.012			
С	0.19	0.25	0.0075	0.0098			
D	9.80	9.98	0.386	0.393			
E	3.81	3.99	0.150	0.157			
е	0.635mm		0.025 inc	h ref.			
Н	5.70	6.20	0.2284	0.2240			
L	0.41	1.27	0.016	0.050			
$\alpha = 0$	$\alpha = 0-8$ deg.						





Note: This package has been chosen as a preliminary package. It will possibly be changed to a smaller solution.

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