

M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs with EDO mode function, fabricated with the high performance CMOS process, and is ideal for the buffer memory systems of personal computer graphics and HDD where high speed, low power dissipation, and low costs are essential. The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application. This device has 2CAS and 1W terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4265CXX-5,-5S	50	13	25	13	90	408
M5M4V4265CXX-6,-6S	60	15	30	15	110	363
M5M4V4265CXX-7,-7S	70	20	35	20	130	333

XX=TP,J

- Standard 40 pin SOJ, 44 pin TSOP (II)
- Single 3.3±0.3V supply
- Low stand-by power dissipation
 - CMOS Input level 1.8mW (Max)
 - CMOS Input level 360µW (Max) *
- Operating power dissipation
 - M5M4V4265CXX-5,-5S 486mW (Max)
 - M5M4V4265CXX-6,-6S 432mW (Max)
 - M5M4V4265CXX-7,-7S 396mW (Max)
- Self refresh capability *
 - Self refresh current 100µA (Max)
- Extended refresh capability
 - Extended refresh current 100µA (Max)
- EDO mode (512-column random access), Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities.
- Early-write mode, OE and W to control output buffer impedance
- 512 refresh cycles every 8.2ms (A0~A8)
- 512 refresh cycles every 128ms (A0~A8) *
- Byte or word control for Read/Write operation (2CAS, 1W type)
 - * : Applicable to self refresh version (M5M4V4265CJ,TP-5S,-6S,-7S : option) only

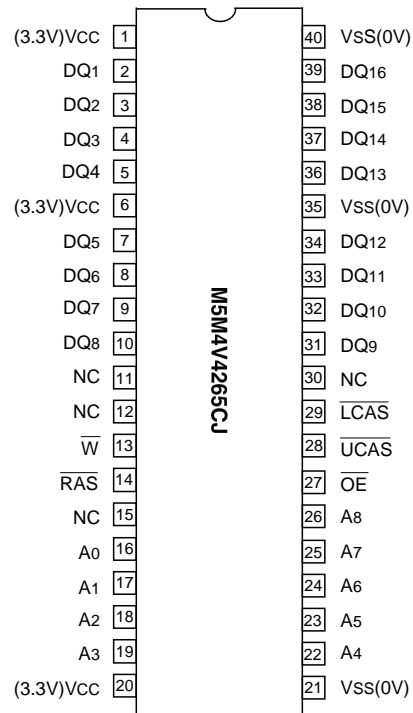
APPLICATION

Microcomputer memory, Refresh memory for CRT, Frame buffer memory for CRT

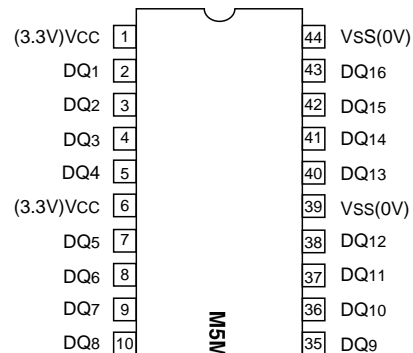
PIN DESCRIPTION

Pin name	Function
A0~A8	Address inputs
DQ1~DQ16	Data inputs / outputs
RAS	Row address strobe input
LCAS	Lower byte control column address strobe input
UCAS	Upper byte control column address strobe input
W	Write control input
OE	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (400mil SOJ)



Outline 44P3W-R (400mil TSOP Nomal Bend)

NC : NO CONNECTION

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FUNCTION

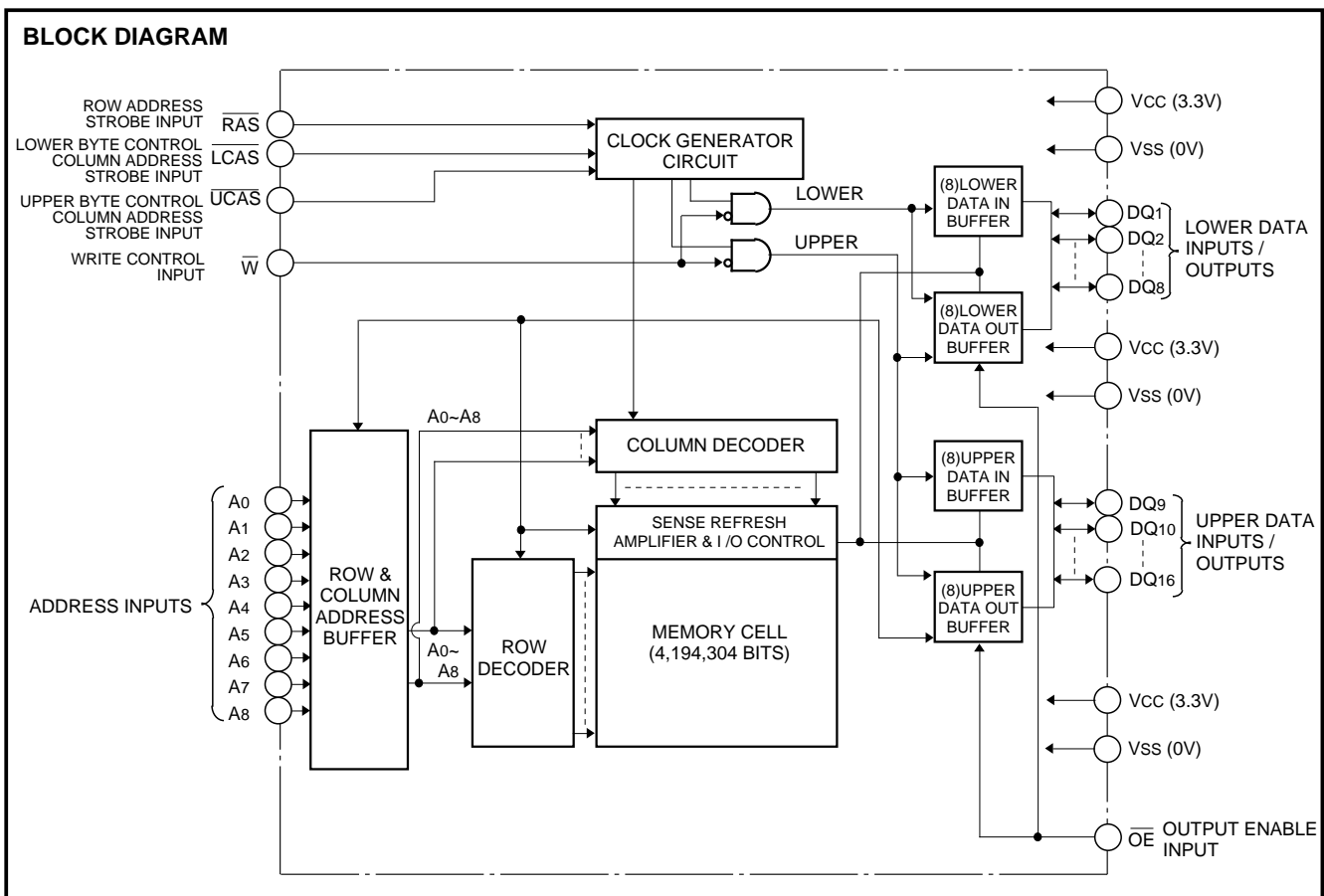
In addition to EDO Mode, normal read, write and read-modify-write operations the M5M4V4265CXX provides a number of other

functions, e.g., $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ ₁ ~DQ ₈	DQ ₉ ~DQ ₁₆
Lower byte read	ACT	ACT	NAC	NAC	ACT	D _{OUT}	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	D _{OUT}
Word read	ACT	ACT	ACT	NAC	ACT	D _{OUT}	D _{OUT}
Lower byte write	ACT	ACT	NAC	ACT	NAC	D _{IN}	D _{NC}
Upper byte write	ACT	NAC	ACT	ACT	NAC	D _{NC}	D _{IN}
Word write	ACT	ACT	ACT	ACT	NAC	D _{IN}	D _{IN}
$\overline{\text{RAS}}$ only refresh	ACT	NAC	NAC	D _{NC}	D _{NC}	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	D _{OUT}	D _{OUT}
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ (Extended *) refresh	ACT	ACT	ACT	D _{NC}	D _{NC}	OPN	OPN
Self refresh *	ACT	ACT	ACT	D _{NC}	D _{NC}	OPN	OPN
Stand-by	NAC	D _{NC}	D _{NC}	D _{NC}	D _{NC}	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, OPN : open



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-0.5~4.6	V
V _I	Input voltage		-0.5~4.6	V
V _O	Output voltage		-0.5~4.6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	3.0	3.3	3.6	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.0		V _{CC} +0.3	V
V _{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=3.3±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} =-2mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} =2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V V _{OUT} V _{CC}	-5		5	μA
I _I	Input current	0V V _{IN} V _{CC} +0.3V, Other inputs pins=0V	-5		5	μA
I _{CC1(AV)}	Average supply current from V _{CC} , operating (Note 3,4,5)	M5M4V4265C-5,-5S	R _{AS} , C _{AS} cycling tr _C =tw _C =min. output open		135	mA
		M5M4V4265C-6,-6S			120	
		M5M4V4265C-7,-7S			110	
I _{CC2}	Supply current from V _{CC} , stand-by (Note 6)	R _{AS} =C _{AS} =V _{IH} , output open			2	mA
		R _{AS} =C _{AS} V _{CC} -0.2V output open			0.5	
					0.1*	
I _{CC3(AV)}	Average supply current from V _{CC} , R _{AS} only refresh mode (Note 3,5)	M5M4V4265C-5,-5S	R _{AS} cycling, C _{AS} =V _{IH} tr _C =min. output open		125	mA
		M5M4V4265C-6,-6S			110	
		M5M4V4265C-7,-7S			95	
I _{CC4(AV)}	Average supply current from V _{CC} EDO mode (Note 3,4,5)	M5M4V4265C-5,-5S	R _{AS} =V _{IL} , C _{AS} cycling t _{PC} =min. output open		125	mA
		M5M4V4265C-6,-6S			110	
		M5M4V4265C-7,-7S			95	
I _{CC6(AV)}	Average supply current from V _{CC} C _{AS} before R _{AS} refresh mode (Note 3,5)	M5M4V4265C-5,-5S	C _{AS} before R _{AS} refresh cycling tr _C =min. output open		115	mA
		M5M4V4265C-6,-6S			100	
		M5M4V4265C-7,-7S			85	
I _{CC8(AV)*}	Average supply current from V _{CC} Extended-refresh mode (Note 6)	R _{AS} cycling C _{AS} 0.2V or C _{AS} before R _{AS} refresh cycling R _{AS} 0.2V or V _{CC} -0.2V C _{AS} 0.2V or V _{CC} -0.2V W 0.2V or V _{CC} -0.2V OE 0.2V or V _{CC} -0.2V A ₀ -A ₈ 0.2V or V _{CC} -0.2V, DQ=open tr _C =250μs, tr _{AS} =tr _{AS} min~1μs			100	μA
I _{CC9(AV)*}	Average supply current from V _{CC} Self-refresh mode (Note 6)	R _{AS} =C _{AS} 0.2V output open			100	μA

Note 2 : Current flowing into an IC is positive, out is negative.

3 : I_{CC1(AV)}, I_{CC3(AV)}, I_{CC4(AV)}, and I_{CC6(AV)} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4 : I_{CC1(AV)} and I_{CC4(AV)} are dependent on output loading. Specified values are obtained with the output open.

5 : Column Address can be changed once or less while R_{AS}=V_{IL} and C_{AS}=V_{IH}.

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CAPACITANCE (Ta=0~70°C, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I =V _{SS}			5	pF
C _{I(CLK)}	Input capacitance, clock inputs	f=1MHz			7	pF
C _{I/O}	Input/Output capacitance, data ports	V _I =25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t _{CAC}	Access time from $\overline{\text{CAS}}$ (Note 7,8)		13		15		20	ns
t _{RAC}	Access time from $\overline{\text{RAS}}$ (Note 7,9)		50		60		70	ns
t _{AA}	Column address access time (Note 7,10)		25		30		35	ns
t _{CPA}	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		28		33		38	ns
t _{OE}	Access time from $\overline{\text{OE}}$ (Note 7)		13		15		20	ns
t _{OH}	Output hold time from $\overline{\text{CAS}}$ (Note 13)	5		5		5		ns
t _{OH}	Output hold time from $\overline{\text{RAS}}$ (Note 13)	5		5		5		ns
t _{CLZ}	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		ns
t _{OEZ}	Output disable time after $\overline{\text{OE}}$ high (Note 12)		13		15		20	ns
t _{WEZ}	Output disable time after $\overline{\text{WE}}$ high (Note 12)		13		15		20	ns
t _{OFF}	Output disable time after $\overline{\text{CAS}}$ high (Note 12,13)		13		15		20	ns
t _{REZ}	Output disable time after $\overline{\text{RAS}}$ high (Note 12,13)		13		15		20	ns

Note 6 : An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 8.2ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 50pF, V_{OH} (I_{OH}=-2mA) and V_{OL} (I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V (V_{OH}) and 0.8V (V_{OL}).

8 : Assumes that t_{RCD} t_{RCD(max)} and t_{ASC} t_{ASC(max)} and t_{CP} t_{CP(max)}.

9 : Assumes that t_{RCD} t_{RCD(max)} and t_{RAD} t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10 : Assumes that t_{RAD} t_{RAD(max)} and t_{ASC} t_{ASC(max)}.

11 : Assumes that t_{CP} t_{CP(max)} and t_{ASC} t_{ASC(max)}.

12 : t_{OEZ} (max), t_{WEZ} (max), t_{OFF} (max) and t_{REZ} (max) defines the time at which the output achieves the high impedance state (I_{OUT} | ±5μA |) and is not reference to V_{OH}(min) or V_{OL}(max).

13 : Output is disabled after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and EDO Mode Cycles)

(Ta=0~70°C, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		8.2		8.2		8.2	ms
tREF	Refresh cycle time *		128		128		128	ms
tRP	$\overline{\text{RAS}}$ high pulse width	30		40		50		ns
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note 16)	18	32	20	45	20	50	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	5		5		5		ns
tRPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		0		ns
tCPN	$\overline{\text{CAS}}$ high pulse width	8		10		10		ns
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low	0		0		0		ns
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low	8		10		10		ns
tCAH	Column address hold time after $\overline{\text{CAS}}$ low	8		10		10		ns
tDZC	Delay time, data to $\overline{\text{CAS}}$ low (Note 19)	0		0		0		ns
tDZO	Delay time, data to $\overline{\text{OE}}$ low (Note 19)	0		0		0		ns
tRDD	Delay time, $\overline{\text{RAS}}$ high to data (Note 20)	13		15		20		ns
tCDD	Delay time, $\overline{\text{CAS}}$ high to data (Note 20)	13		15		20		ns
tODD	Delay time, $\overline{\text{OE}}$ high to data (Note 20)	13		15		20		ns
tT	Transition time (Note 21)	1	50	1	50	1	50	ns

Note 14 : The timing requirements are assumed tT=2ns.

15 : VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16 : tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17 : tRAD(max) is specified as a reference point only. If tRAD tRAD(max) and tASC tASC(max), access time is controlled exclusively by tAA.

18 : tASC(max) is specified as a reference point only. If tRCD tRCD(max) and tASC tASC(max), access time is controlled exclusively by tCAC.

19 : Either tDZC or tDZO must be satisfied.

20 : Either tRDD or tCDD or tODD must be satisfied.

21 : tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	8	10000	10	10000	13	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	40		48		55		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	13		15		20		ns
tRCS	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{\text{CAS}}$ high (Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{\text{RAS}}$ high (Note 22)	0		0		0		ns
tRAL	Column address to $\overline{\text{RAS}}$ hold time	25		30		35		ns
tCAL	Column address to $\overline{\text{CAS}}$ hold time	13		18		23		ns
tORH	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		20		ns
tOCH	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		20		ns

Note 22 : Either tRCH or tRRH must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	8	10000	10	10000	10	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	40		48		55		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	13		15		20		ns
twCS	Write setup time before $\overline{\text{CAS}}$ low (Note 24)	0		0		0		ns
twCH	Write hold time after $\overline{\text{CAS}}$ low	8		10		13		ns
tcWL	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	8		10		13		ns
trWL	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	0		0		0		ns
tDH	Data hold time after $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note 23)	109		133		161		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	75	10000	89	10000	107	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	38	10000	44	10000	57	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	70		82		99		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	38		44		57		ns
trCS	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
tcWD	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (Note 24)	28		32		42		ns
trWD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{\text{W}}$ low (Note 24)	40		47		57		ns
toEH	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	13		15		20		ns

Note 23 : trWC is specified as trWC(min)=trAC(max)+tODD(min)+trWL(min)+trP(min)+4t.

24 : twCS, tcWD, trWD and tAWD and tcpWD are specified as reference points only. If twCS twCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tcWD tcWD(min), trWD trWD(min), tAWD tAWD(min) and tcpWD tcpWD(min) (for EDO mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to VIH) is indeterminate.

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EDO Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by \overline{OE} or \overline{W}) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
tHPRWC	Hyper page mode read write/read modify write cycle time	57		66		79		ns
tDOH	Output hold time from \overline{CAS} low	5		5		5		ns
tRAS	\overline{RAS} low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
tCP	\overline{CAS} high pulse width (Note 28)	8	13	10	16	10	16	ns
tCPRH	\overline{RAS} hold time after \overline{CAS} precharge	28		33		38		ns
tCPWD	Delay time, \overline{CAS} precharge to \overline{W} low (Note 24)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until \overline{CAS} access	7		7		7		ns
tOEPE	\overline{OE} pulse width (Hi-Z control)	7		7		7		ns
twPE	\overline{W} pulse width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, \overline{CAS} low to \overline{W} low after read	28		32		42		ns
tHAWD	Delay time, Address to \overline{W} low after read	40		47		57		ns
tHPWD	Delay time, \overline{CAS} precharge to \overline{W} low after read	43		50		60		ns
tHCOD	Delay time, \overline{CAS} low to \overline{OE} high after read	13		15		20		ns
tHAOD	Delay time, Address to \overline{OE} high after read	25		30		35		ns
tHPOD	Delay time, \overline{CAS} precharge to \overline{OE} high after read	28		33		38		ns

Note 25 : All previously specified timing requirements and switching characteristics are applicable to their respective EDO mode cycle.

26 : tHPC(min) is specified in the case of read-only and early write-only in EDO mode.

27 : tRAS(min) is specified as two cycles of \overline{CAS} input are performed.

28 : tCP(max) is specified as a reference point only.

 \overline{CAS} before \overline{RAS} Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	\overline{CAS} setup time before \overline{RAS} low	5		5		5		ns
tCHR	\overline{CAS} hold time after \overline{RAS} low	10		10		15		ns
tCAS	\overline{CAS} low pulse width	17		17		22		ns

Note 29 : Eight or more \overline{CAS} before \overline{RAS} cycles instead of eight \overline{RAS} cycles are necessary for proper operation of \overline{CAS} before \overline{RAS} refresh mode.

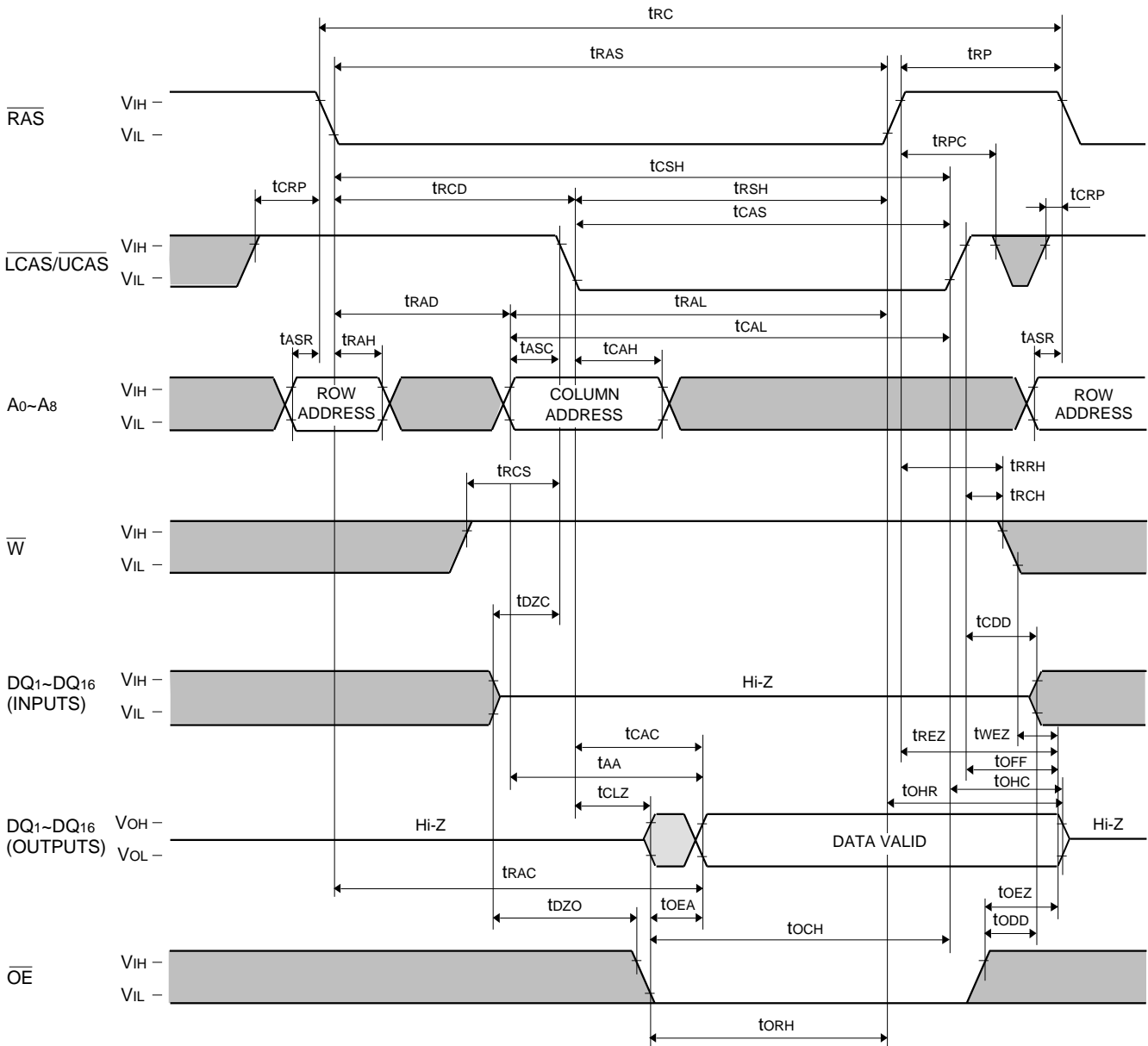
Self Refresh Cycle * (Note 30)

Symbol	Parameter	Limits						Unit
		M5M4V4265C-5,-5S		M5M4V4265C-6,-6S		M5M4V4265C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	CBR self refresh \overline{RAS} low pulse width	100		100		100		μ s
tRPS	CBR self refresh \overline{RAS} high precharge time	90		110		130		ns
tCHS	CBR self refresh \overline{CAS} hold time	-50		-50		-50		ns

M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Timing Diagrams (Note 31) Read Cycle



Note 31



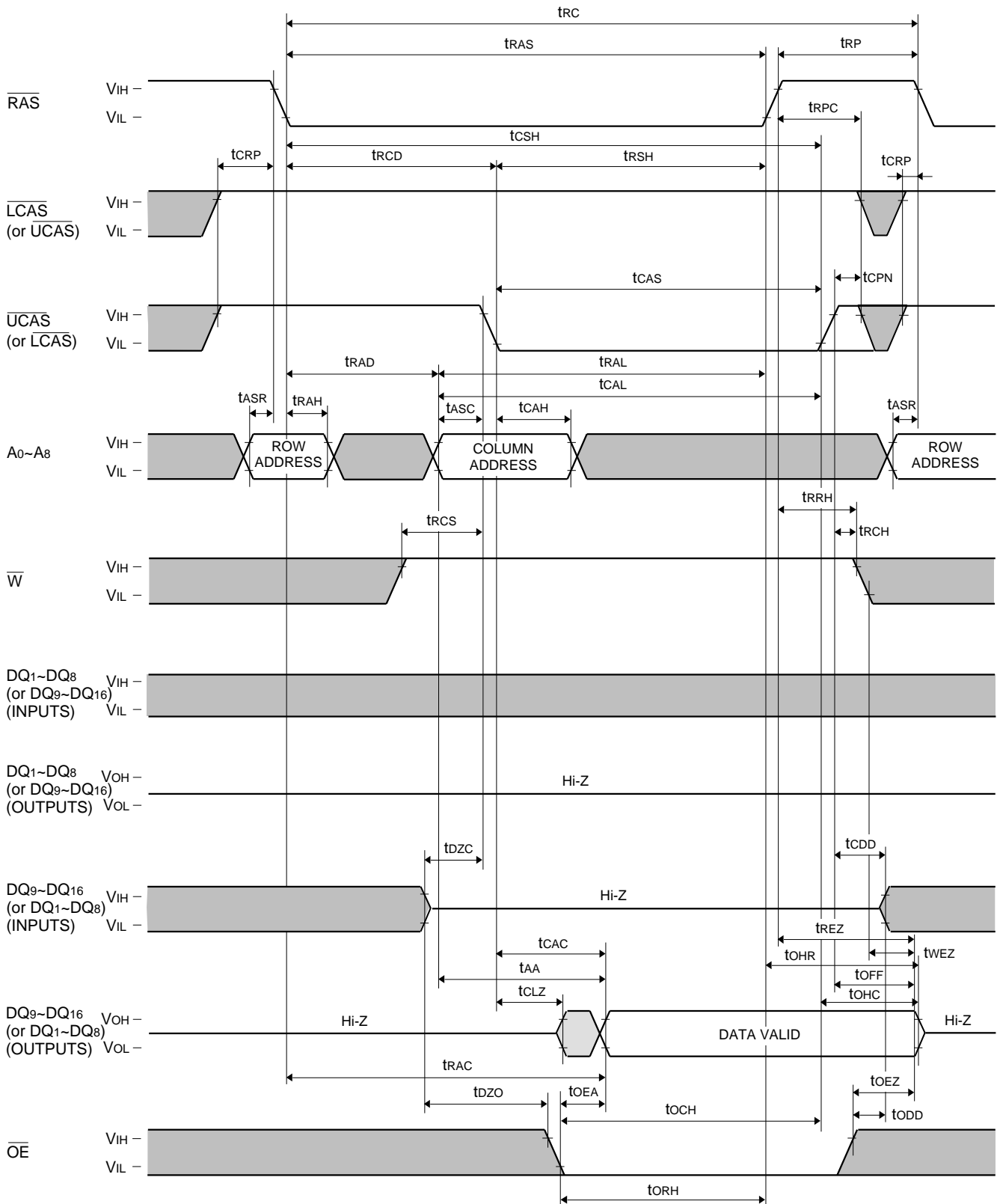
Indicates the don't care input.
 $V_{IH(min)}$ V_{IN} $V_{IH(max)}$ or $V_{IL(min)}$ V_{IN} $V_{IL(max)}$

Indicates the invalid output.

M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

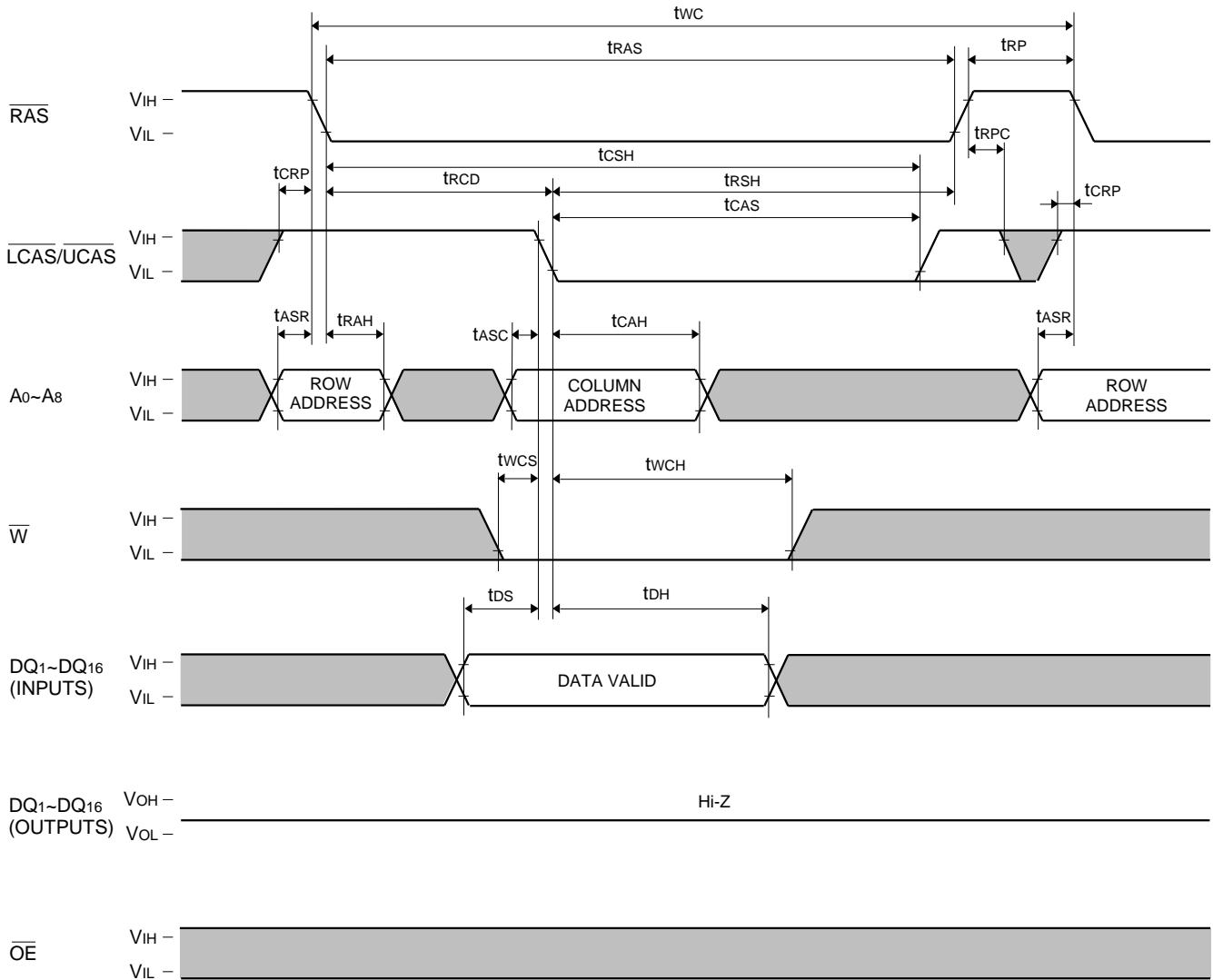
Byte Read Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

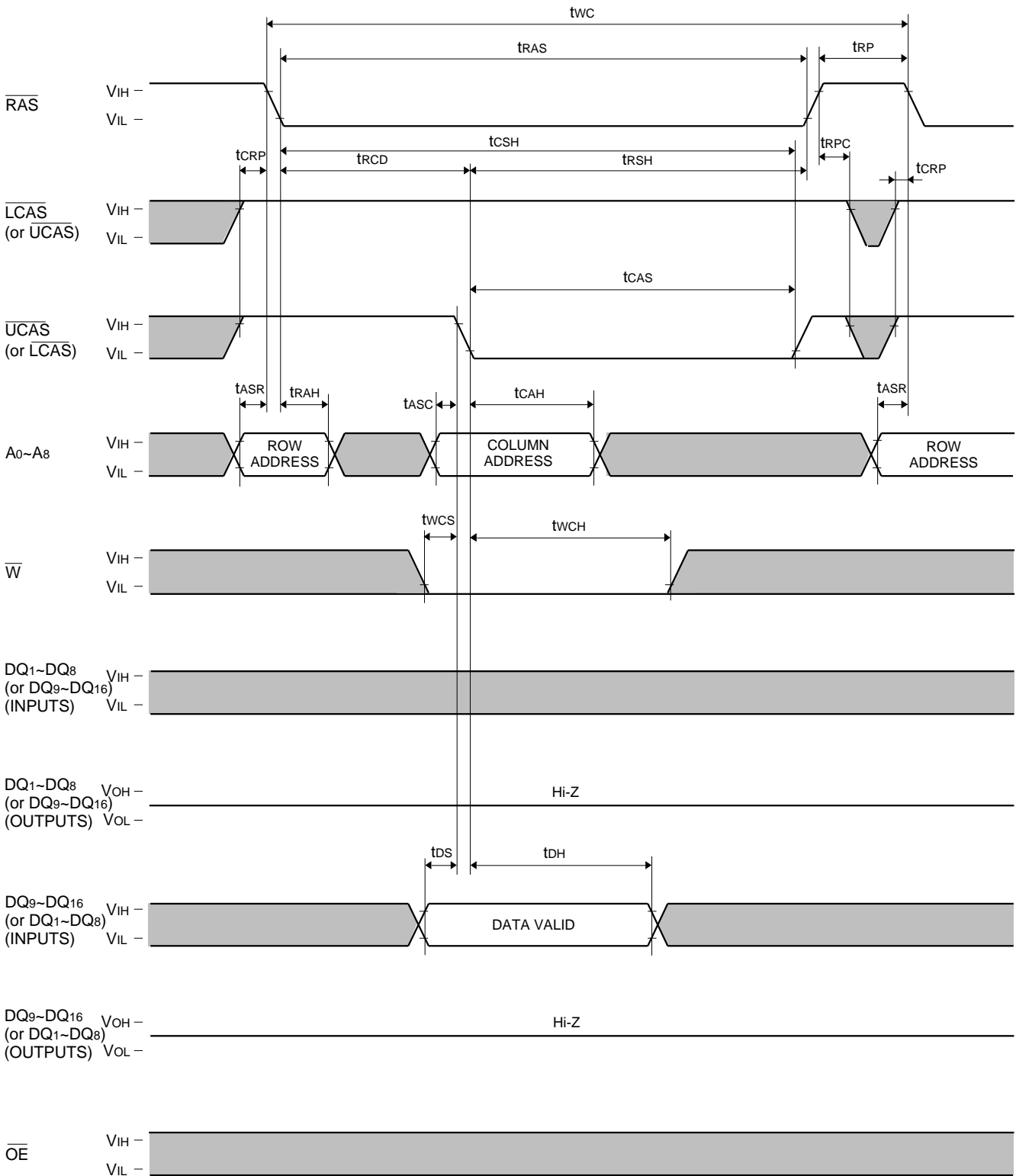
Early Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

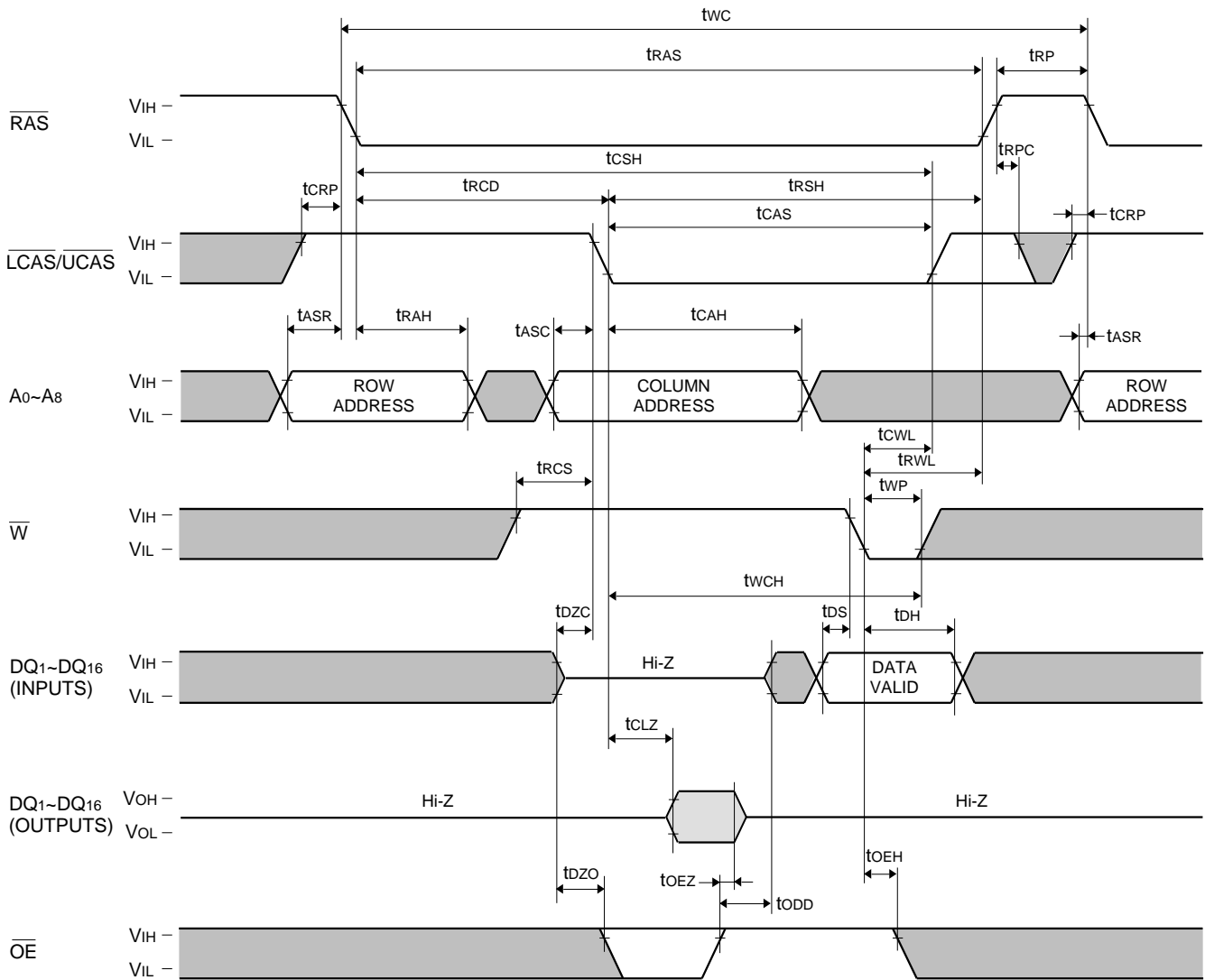
Byte Early Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

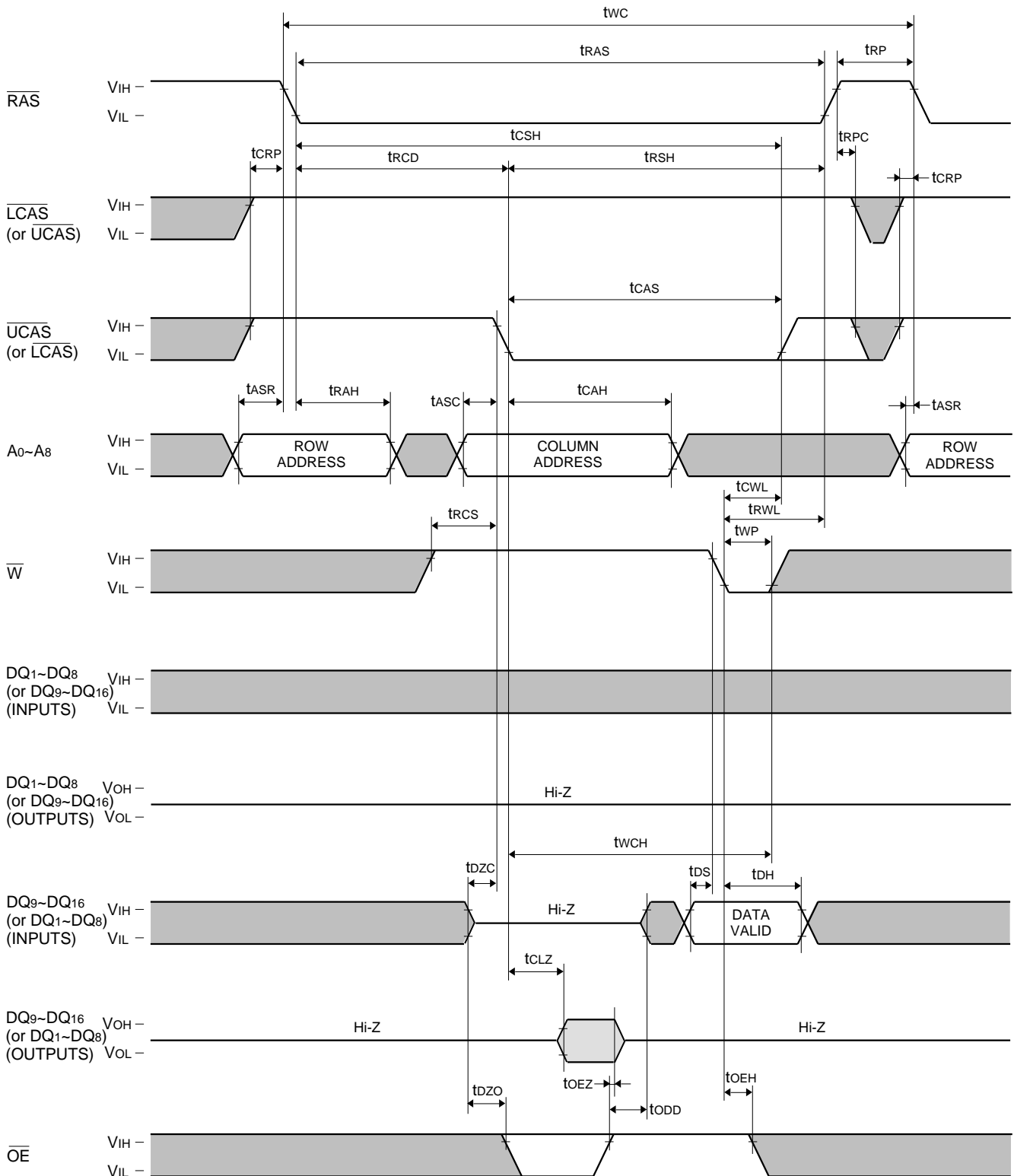
Delayed Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

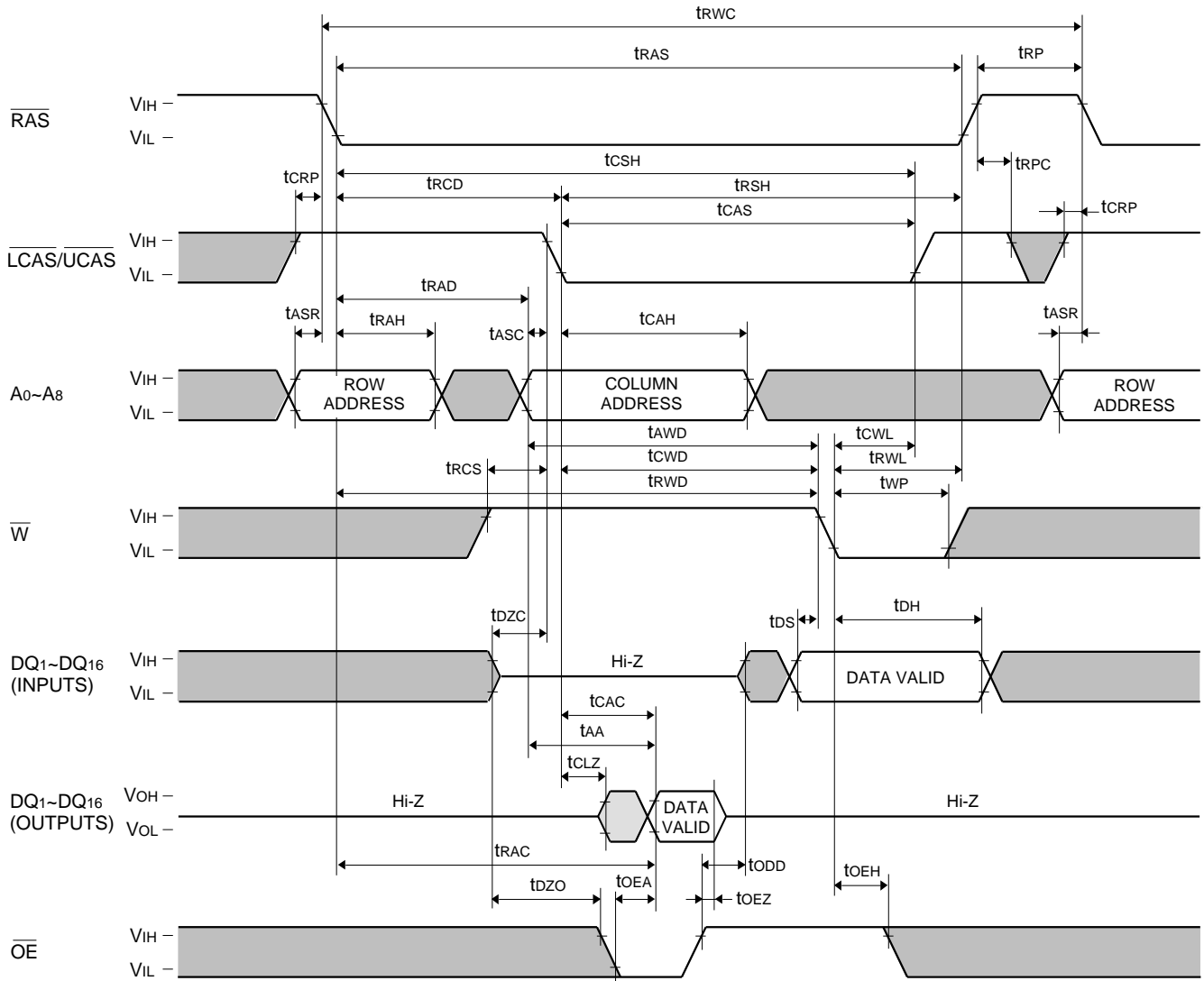
Byte Delayed Write Cycle



M5M4V4265CJ, TP-5, -6, -7, -5S, -6S, -7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

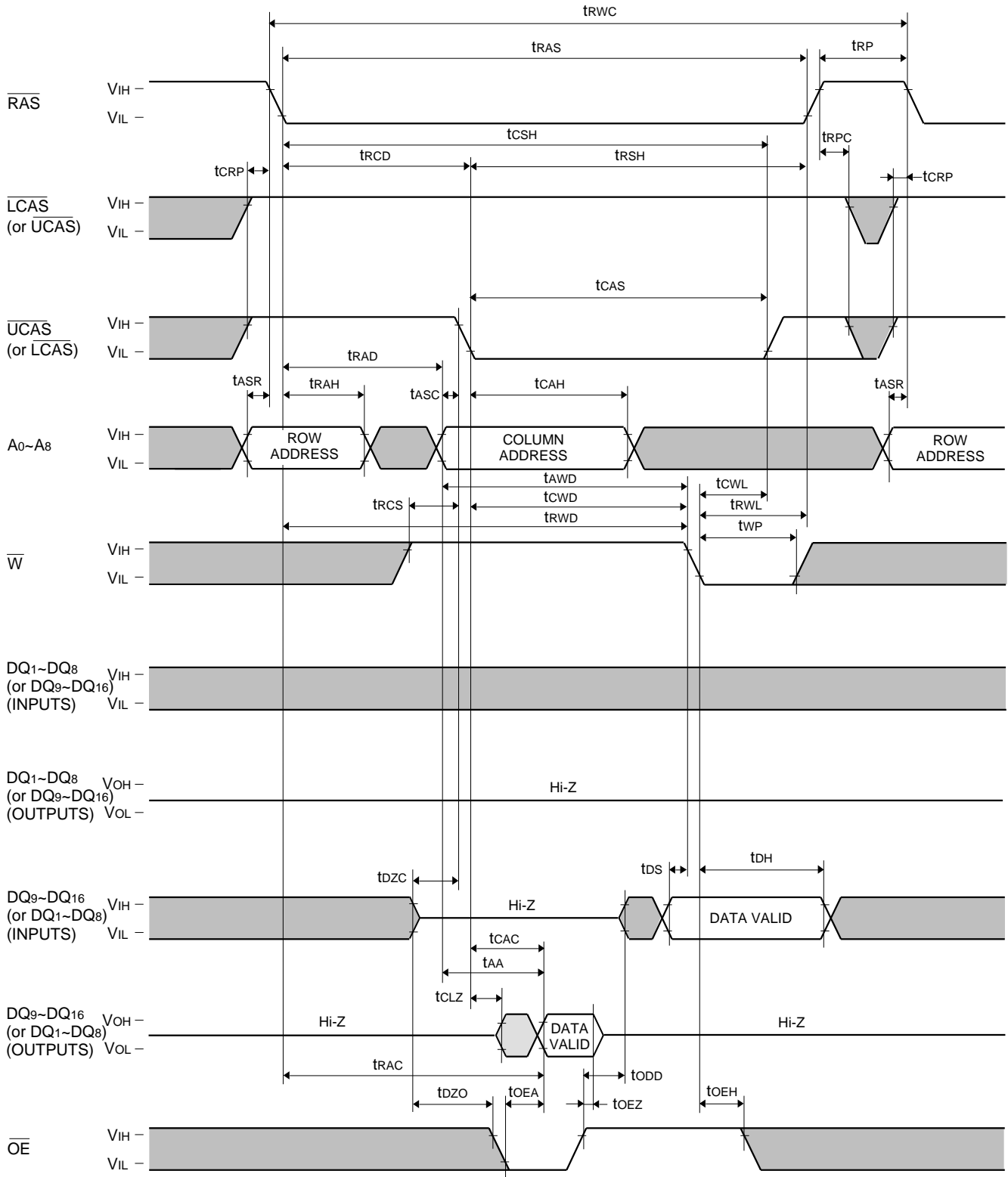
Read-Write, Read-Modify-Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

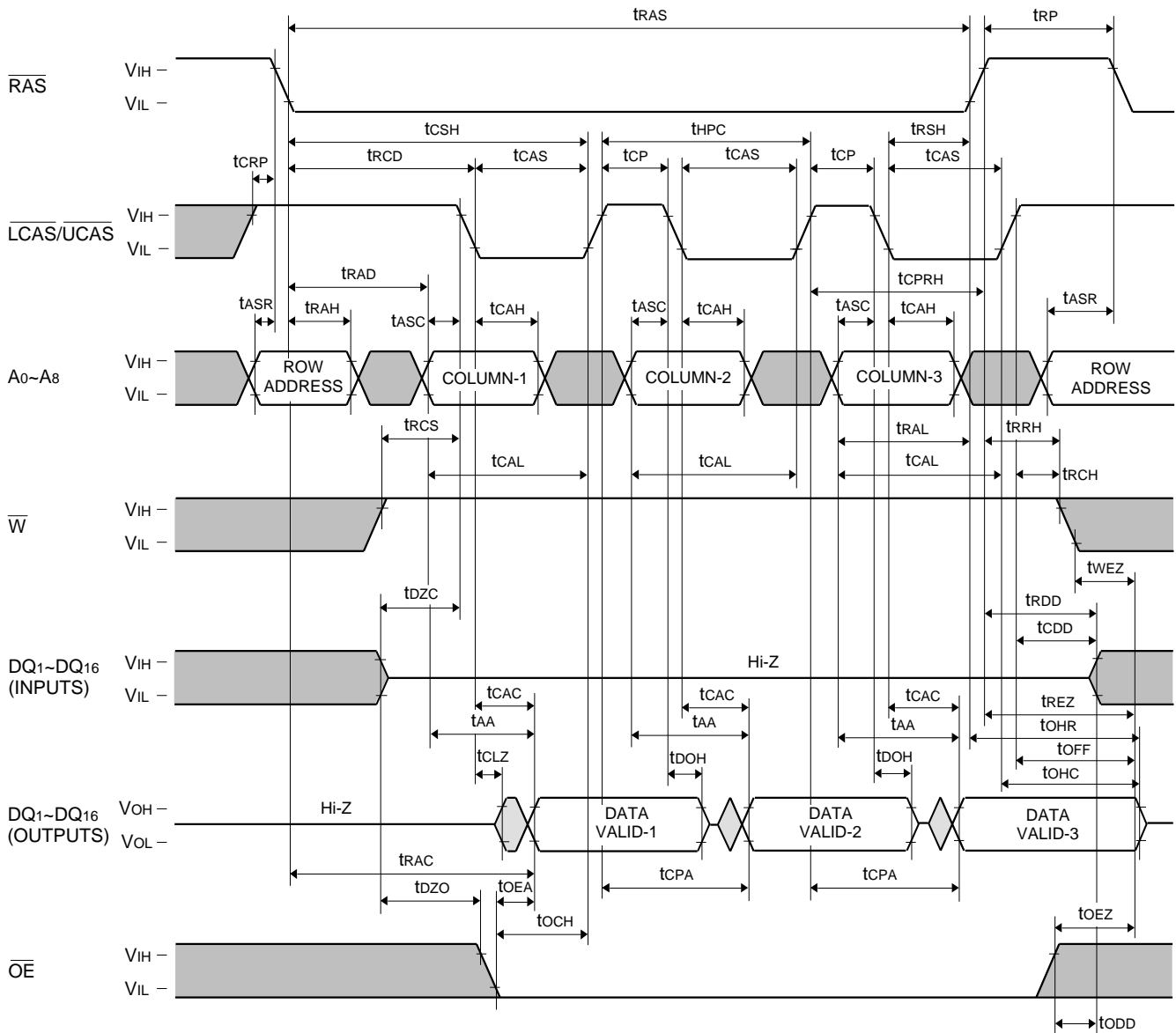
Byte Read-Write, Read-Modify-Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

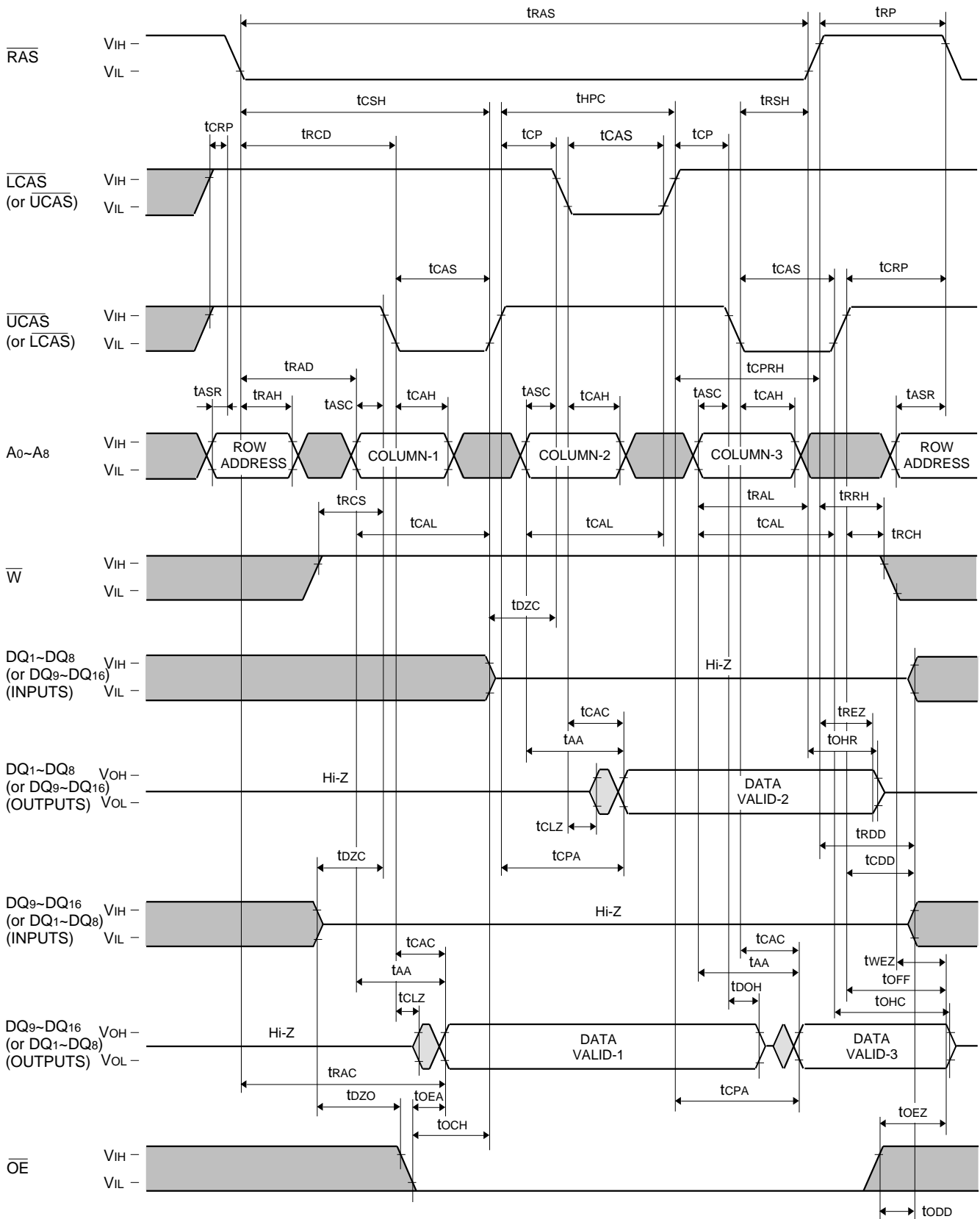
EDO Mode Read Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

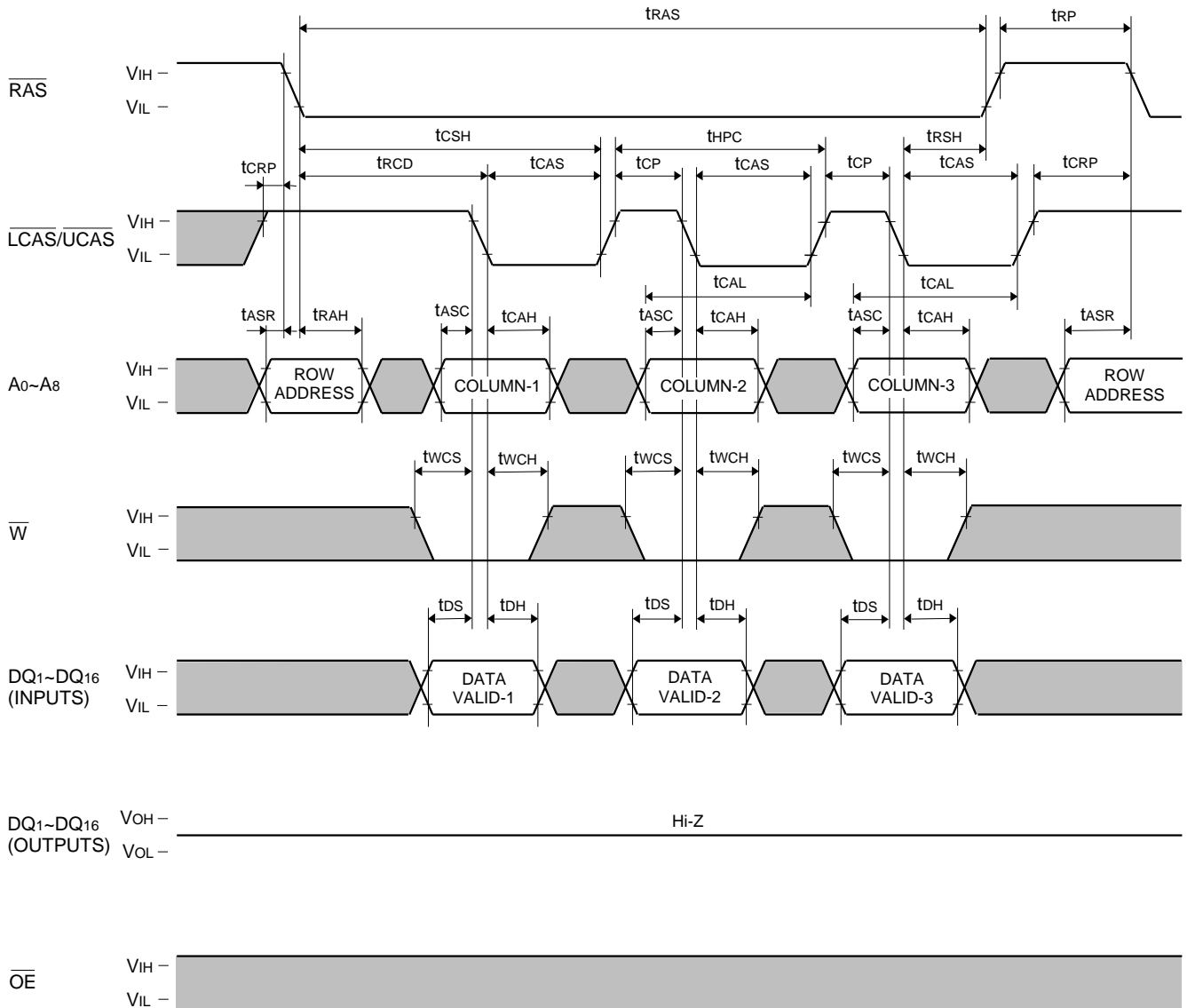
EDO Mode Byte Read Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

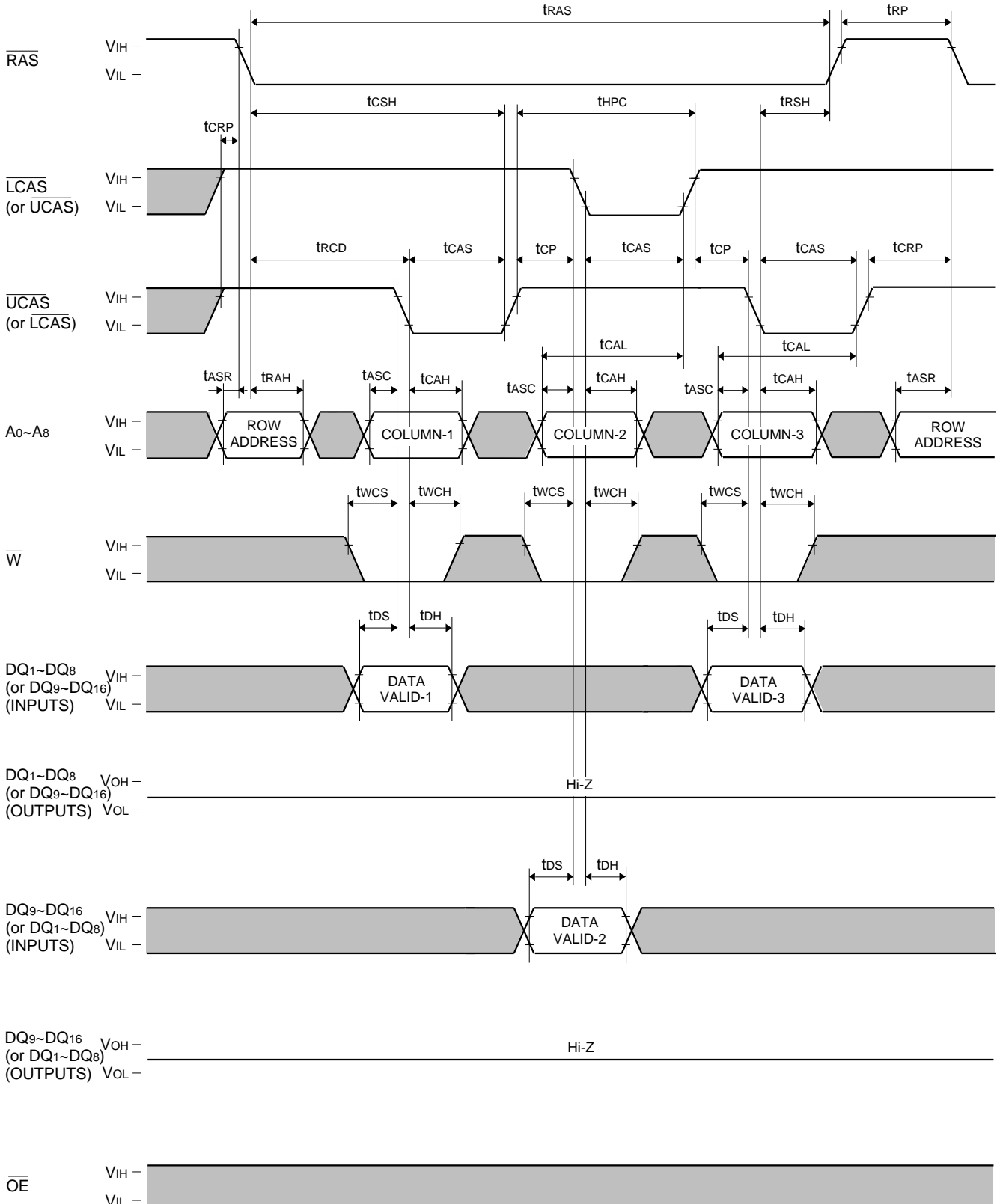
EDO Mode Early Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

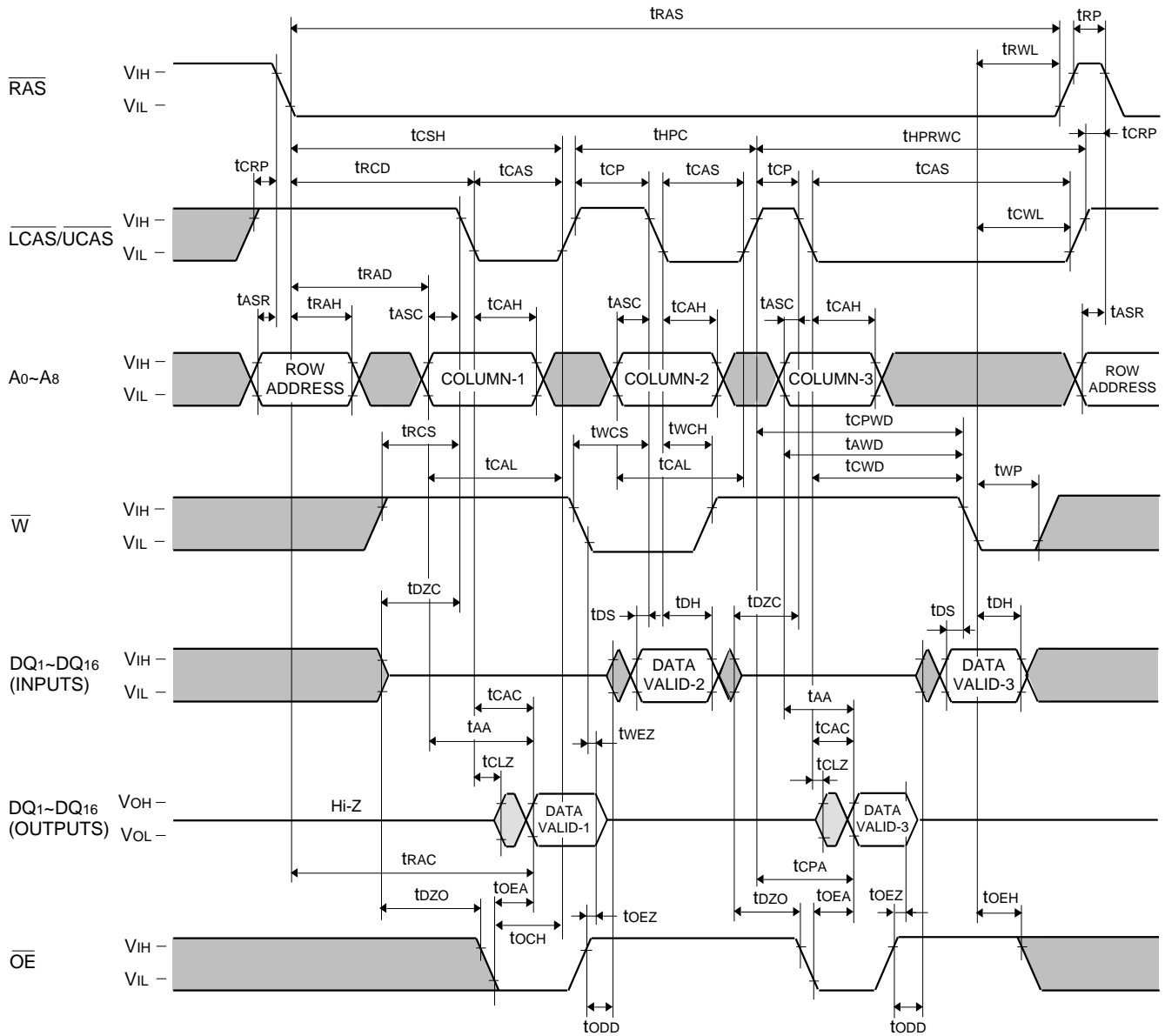
EDO Mode Byte Early Write Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

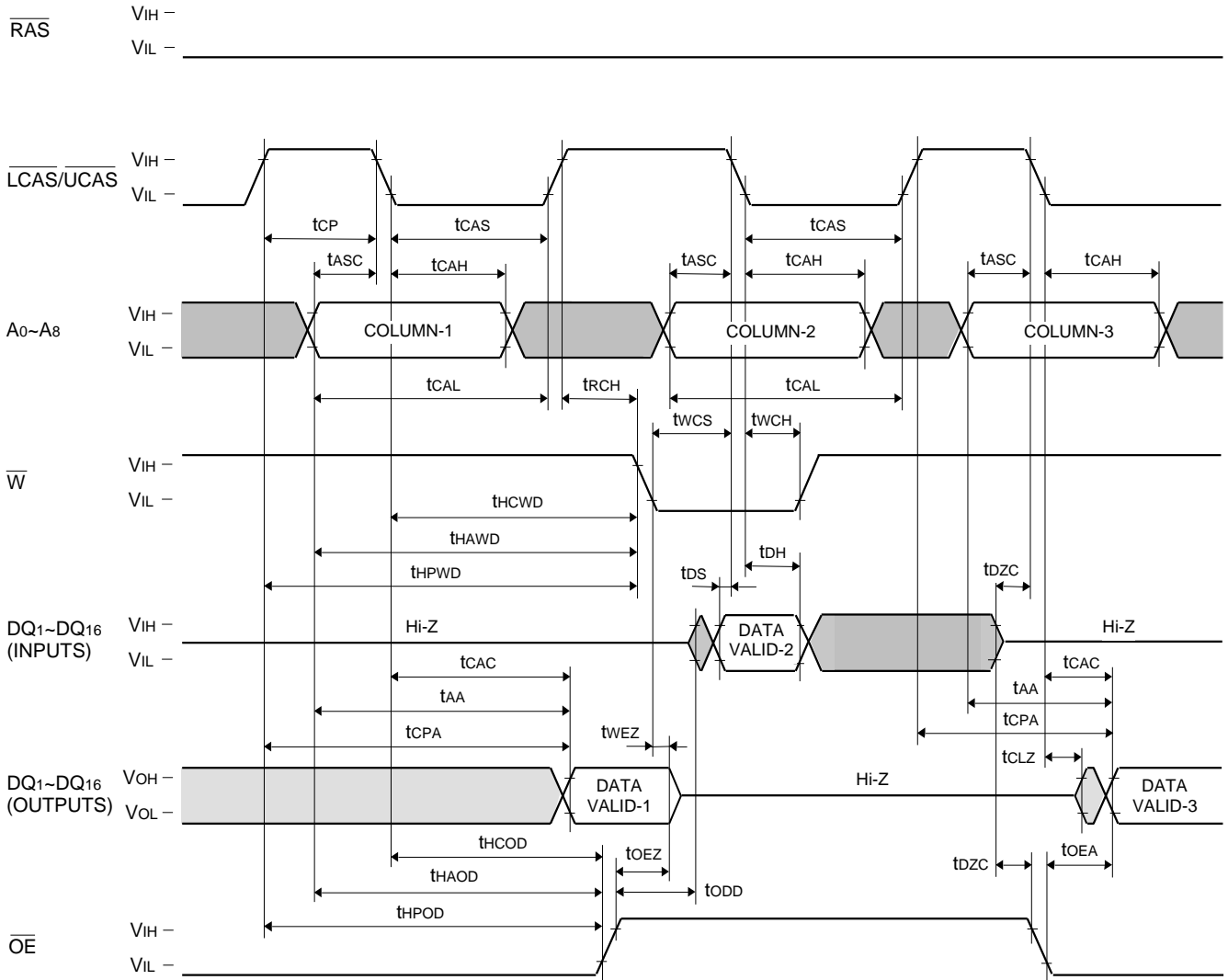
EDO Mode Mix Cycle (1)



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

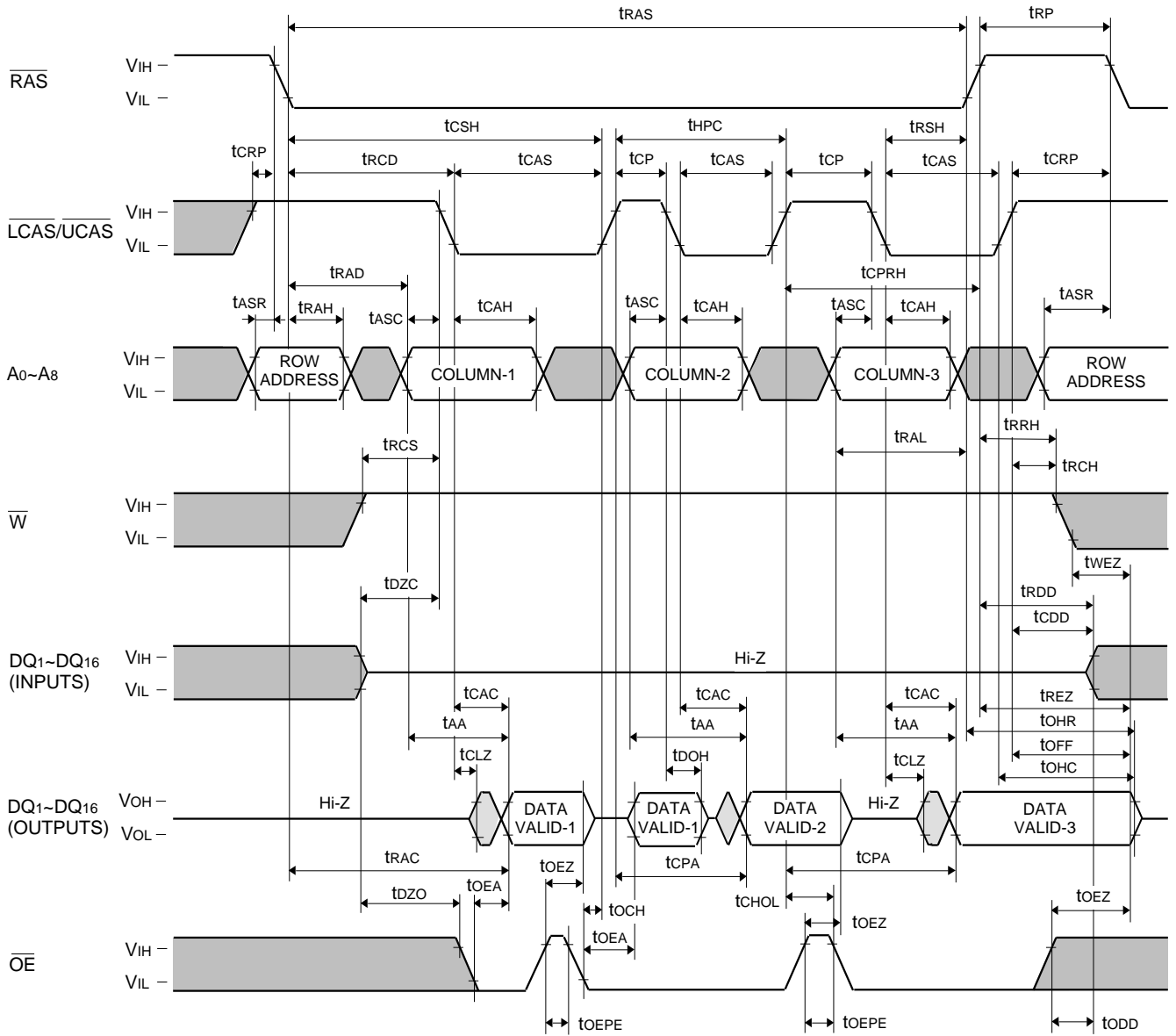
EDO Mode Mix Cycle (2)



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

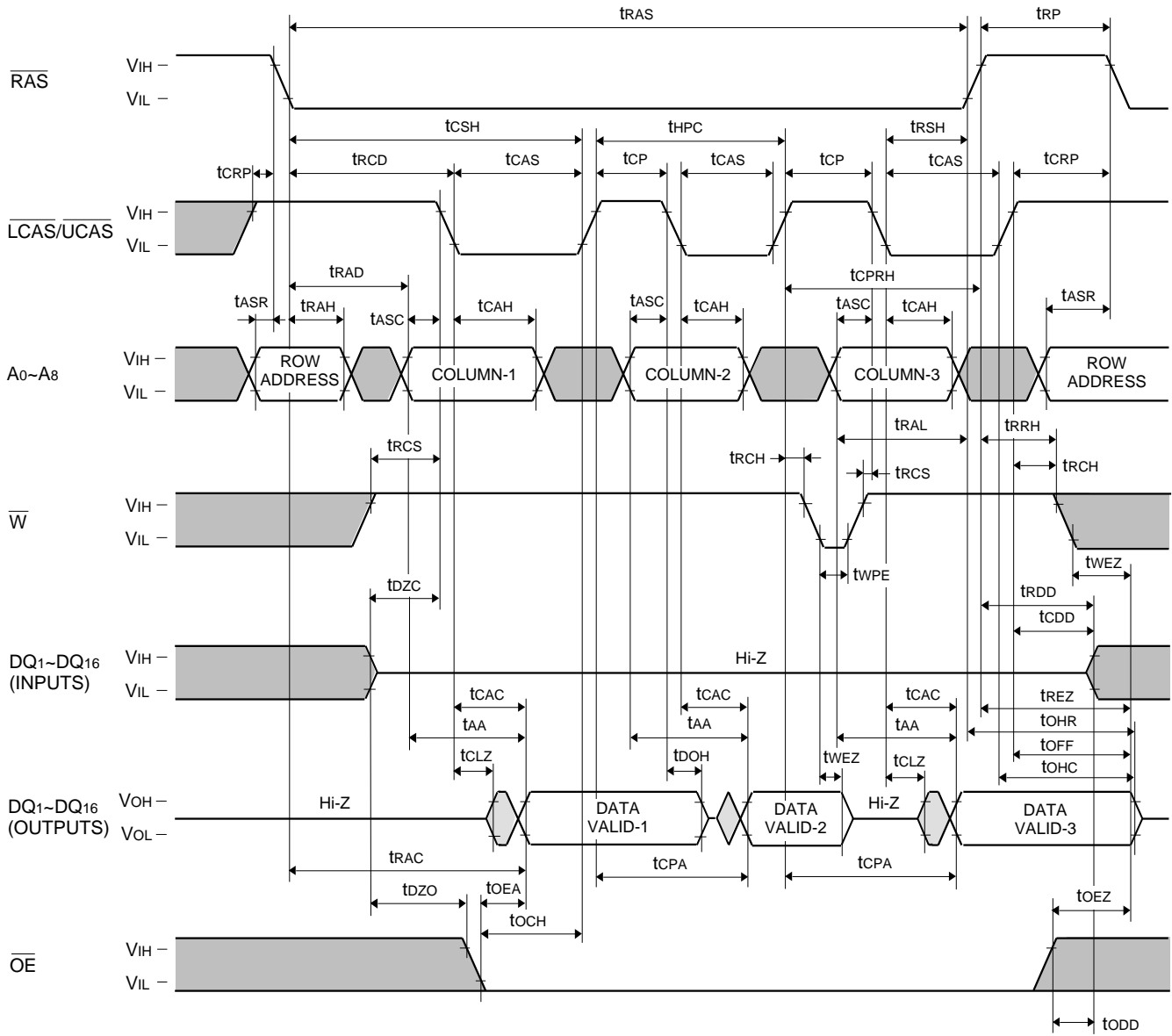
EDO Mode Read Cycle (Hi-Z control by \overline{OE})



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

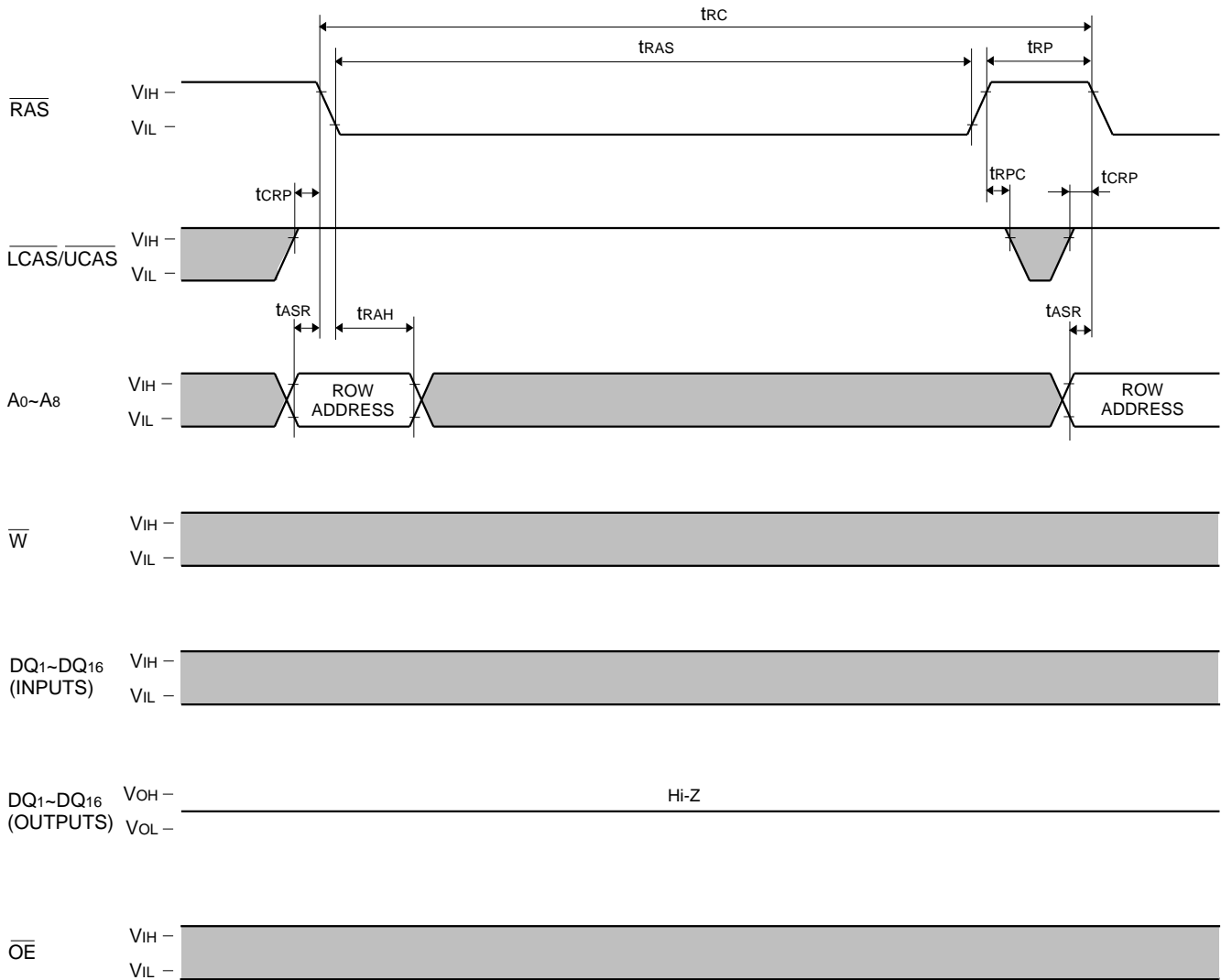
EDO Mode Read Cycle (Hi-Z control by \overline{W})



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

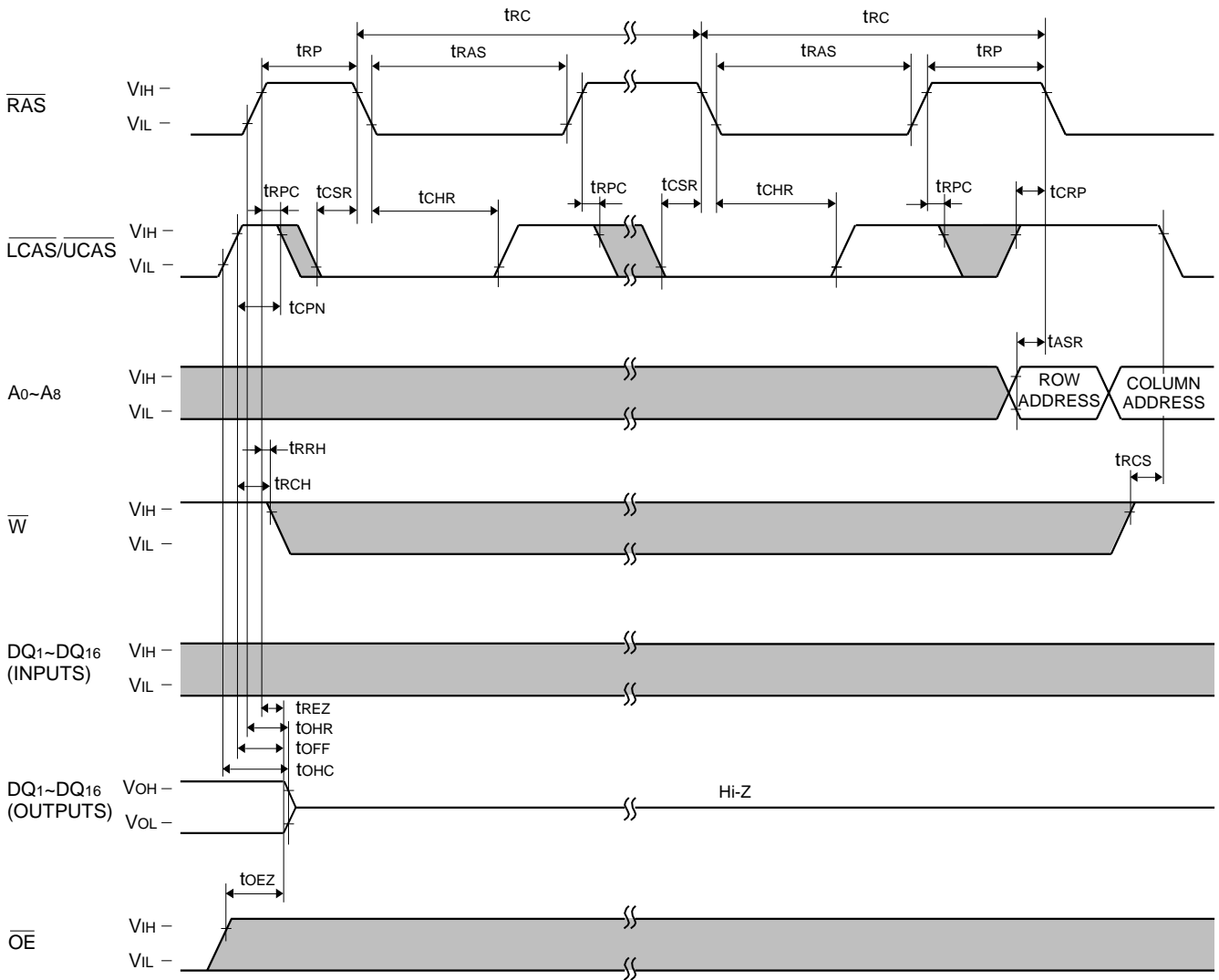
RAS-only Refresh Cycle



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

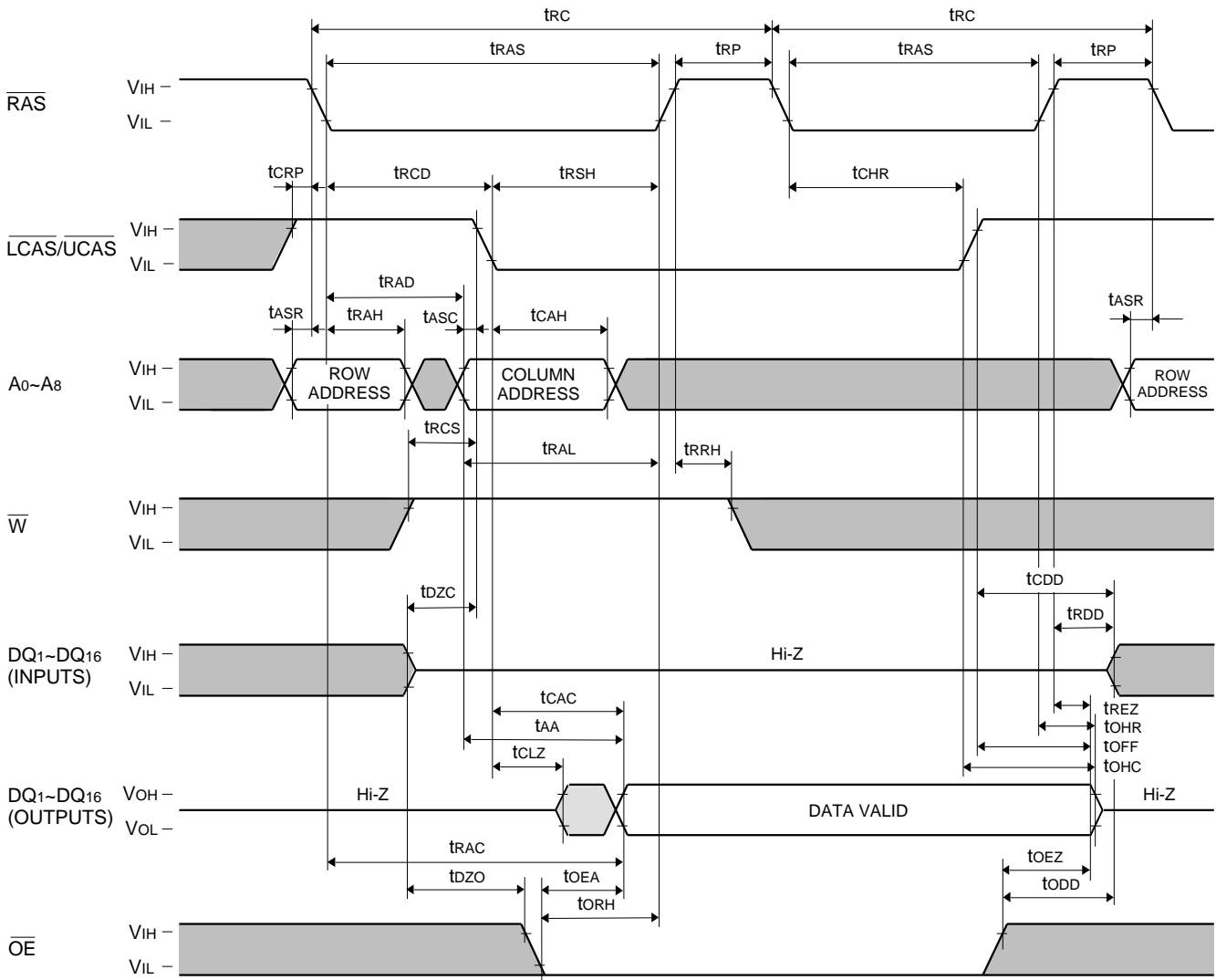
CAS before RAS Refresh Cycle, Extended Refresh Cycle *



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 32)

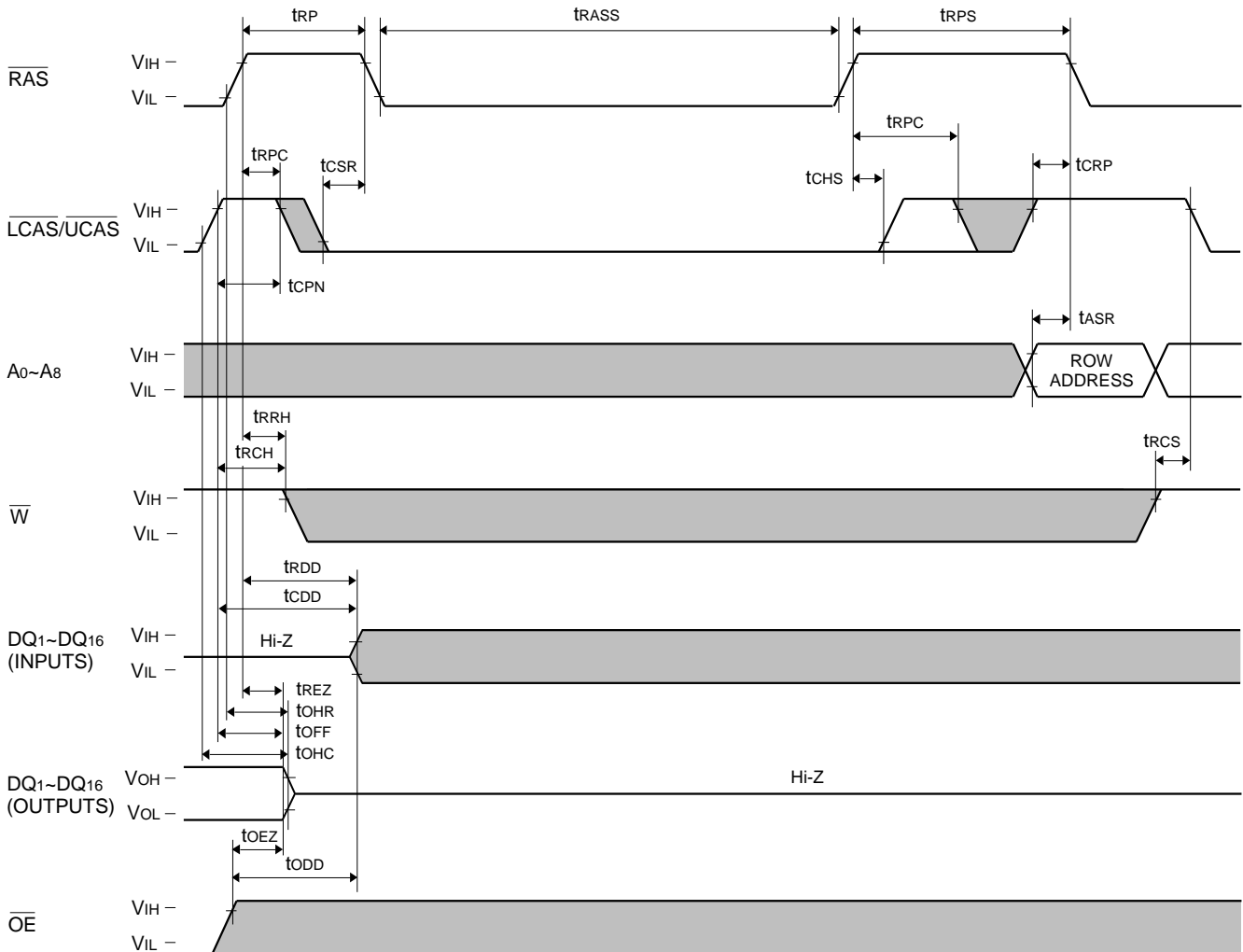


Note 32 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Self Refresh Cycle * (Note 30)



M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Note 30 : Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of \overline{RAS} signal during self refresh period.

1. Distributed refresh during Read/Write operation

(A) Timing Diagram

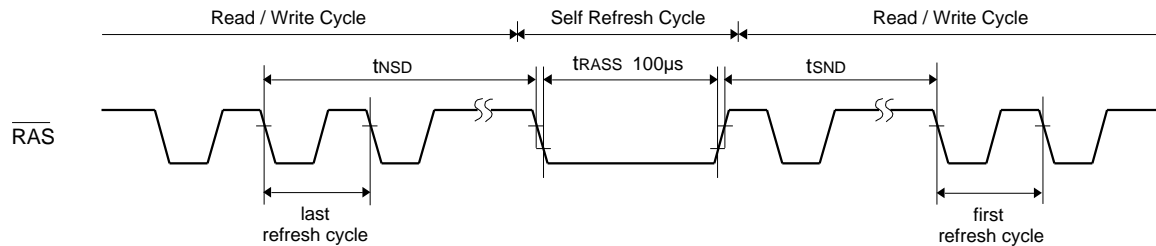
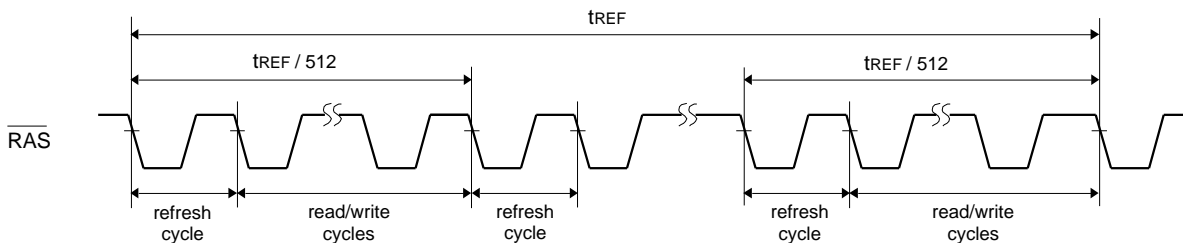


Table 2

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR distributed refresh	t_{NSD} 250µs	t_{SND} 250µs
\overline{RAS} only distributed refresh	t_{NSD} 16µs	t_{SND} 16µs

(B) Definition of distributed refresh



Definition of CBR distributed refresh

(Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250µs max.) CBR cycles within 128 ms.

Definition of \overline{RAS} only distributed refresh

All combinations of nine row address signals ($A_0 \sim A_8$) are selected during 512 constant period (16µs max.) \overline{RAS} only refresh cycles within 8.2 ms.

Note:

Hidden refresh may be used instead of CBR refresh.

$\overline{RAS}/\overline{CAS}$ refresh may be used instead of \overline{RAS} only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).

- Switching from self refresh operation to read/write operation.

The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.2 \overline{RAS} only distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16µs.

- Switching from self refresh operation to read/write operation.

The time interval t_{SND} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within 16µs.

M5M4V4265CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

2. Burst refresh during Read/Write operation

(A) Timing diagram

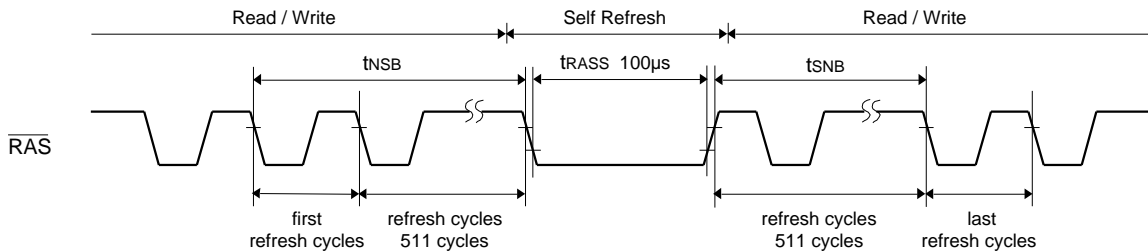
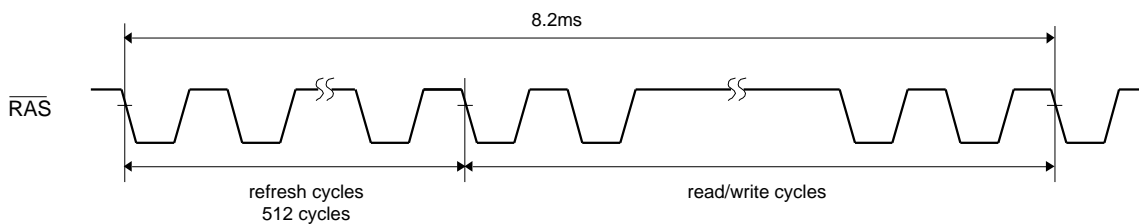


Table 3

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR burst refresh	tNSB 8.2ms	tNSB 8.2ms
$\overline{\text{RAS}}$ only burst refresh	tNSB+tNSB 8.2ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of $\overline{\text{RAS}}$ only burst refresh

All combination of nine row address signals (A_0 - A_8) are selected during 512 continuous $\overline{\text{RAS}}$ only refresh cycles within 8.2 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation.
The time interval tNSB from the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation.
The time interval tNSB from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read/write operation period should be set within 8.2 ms.

2.2 $\overline{\text{RAS}}$ only burst refresh

- Switching from read/write operation to self refresh operation.
The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the first $\overline{\text{RAS}}$ only refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within tNSB (shown in table 3).
- Switching from self refresh operation to read/write operation.
The time interval from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last $\overline{\text{RAS}}$ only refresh cycle during read/write operation period should be set within tNSB (shown in table 3).