

**KMM5362000B2/B2G**

**DRAM MODULES**

*2Mx36 DRAM SIMM Memory Module*

**FEATURES**

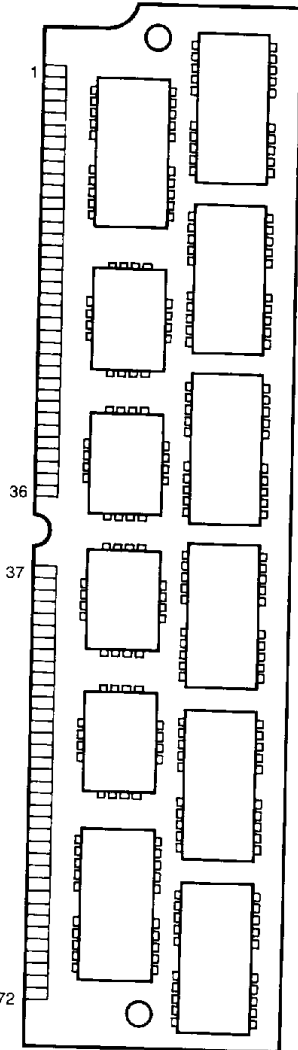
- Performance range:

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>
KMM5362000B2-6	60ns	15ns	110ns
KMM5362000B2-7	70ns	20ns	130ns
KMM5362000B2-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and output
- Single +5V ± 10% power supply
- 1024 cycles/16ms refresh
- JEDEC standard pinout

**PIN CONFIGURATIONS** (Front View)

Pin	Symbol	Pin	Symbol
1	V <sub>SS</sub>	37	DQ <sub>17</sub>
2	DQ <sub>0</sub>	38	DQ <sub>35</sub>
3	DQ <sub>18</sub>	39	V <sub>SS</sub>
4	DQ <sub>1</sub>	40	CAS <sub>0</sub>
5	DQ <sub>19</sub>	41	CAS <sub>2</sub>
6	DQ <sub>2</sub>	42	CAS <sub>3</sub>
7	DQ <sub>20</sub>	43	CAS <sub>1</sub>
8	DQ <sub>3</sub>	44	RAS <sub>0</sub>
9	DQ <sub>21</sub>	45	RAS <sub>1</sub>
10	V <sub>CC</sub>	46	NC
11	NC	47	W
12	A <sub>0</sub>	48	NC
13	A <sub>1</sub>	49	DQ <sub>9</sub>
14	A <sub>2</sub>	50	DQ <sub>27</sub>
15	A <sub>3</sub>	51	DQ <sub>10</sub>
16	A <sub>4</sub>	52	DQ <sub>28</sub>
17	A <sub>5</sub>	53	DQ <sub>11</sub>
18	A <sub>6</sub>	54	DQ <sub>29</sub>
19	NC	55	DQ <sub>12</sub>
20	DQ <sub>4</sub>	56	DQ <sub>30</sub>
21	DQ <sub>22</sub>	57	DQ <sub>13</sub>
22	DQ <sub>5</sub>	58	DQ <sub>31</sub>
23	DQ <sub>23</sub>	59	V <sub>CC</sub>
24	DQ <sub>6</sub>	60	DQ <sub>32</sub>
25	DQ <sub>24</sub>	61	DQ <sub>14</sub>
26	DQ <sub>7</sub>	62	DQ <sub>33</sub>
27	DQ <sub>25</sub>	63	DQ <sub>15</sub>
28	A <sub>7</sub>	64	DQ <sub>34</sub>
29	NC	65	DQ <sub>16</sub>
30	V <sub>CC</sub>	66	NC
31	A <sub>8</sub>	67	PD <sub>1</sub>
32	A <sub>9</sub>	68	PD <sub>2</sub>
33	RAS <sub>3</sub>	69	PD <sub>3</sub>
34	RAS <sub>2</sub>	70	PD <sub>4</sub>
35	DQ <sub>26</sub>	71	NC
36	DQ <sub>8</sub>	72	V <sub>SS</sub>



**GENERAL DESCRIPTION**

The Samsung KMM5362000B2 is a 1M bitsx36 Dynamic RAM high density memory module. The Samsung KMM5362000B2 consist of sixteen CMOS 1Mx4 bit DRAMs in 20-pin SOJ package and eight CMOS 1Mx1 bit DRAMs in 18-pin PLCC package mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5362000B2 is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

Pin Name	Pin Function
A <sub>0</sub> -A <sub>9</sub>	Address Inputs
DQ <sub>0</sub> -DQ <sub>35</sub>	Data In/Out
W	Read/Write Input
RAS <sub>0</sub> -RAS <sub>3</sub>	Row Address Strobe
CAS <sub>0</sub> -CAS <sub>3</sub>	Column Address Strobe
PD <sub>1</sub> -PD <sub>4</sub>	Presence Detect
V <sub>CC</sub>	Power (+5V)
V <sub>SS</sub>	Ground
NC	No Connection

**Presence Detect Pins (Optional)**

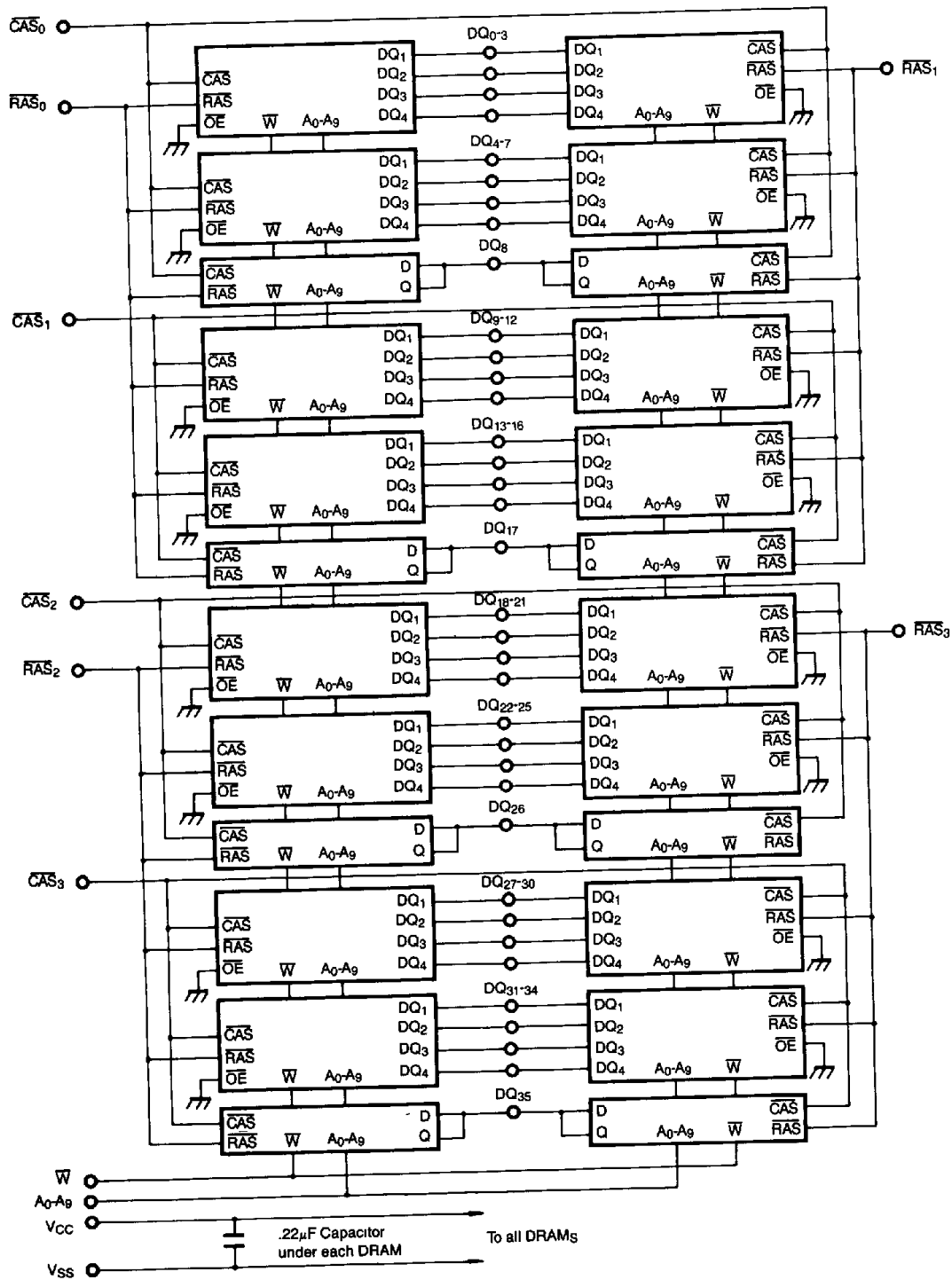
Pin	60ns	70ns	80ns
PD <sub>1</sub>	NC	NC	NC
PD <sub>2</sub>	NC	NC	NC
PD <sub>3</sub>	NC	V <sub>SS</sub>	NC
PD <sub>4</sub>	NC	NC	V <sub>SS</sub>

\* Pin Connection Changing Available

KMM5362000B2/B2G

DRAM MODULES

FUNCTIONAL BLOCK DIAGRAM



## KMM5362000B2/B2G

## DRAM MODULES

## ABSOLUTE MAXIMUM RATINGS\*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	- 1 to + 7.0	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	- 1 to + 7.0	V
Storage Temperature	$T_{STG}$	- 55 to + 150	°C
Power Dissipation	$P_D$	14.4	W
Short Circuit Output Current	$I_{OS}$	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to  $V_{SS}$ ,  $T_A = 0$  to  $70^\circ\text{C}$ )

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Ground	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	—	$V_{CC} + 1$	V
Input Low Voltage	$V_{IL}$	- 1.0	—	0.8	V

## DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* (RAS, CAS, Address Cycling @ $t_{RC} = \text{min.}$ )	KMM5362000B2-6	$I_{CC1}$	—	1024	mA
	KMM5362000B2-7		—	924	mA
	KMM5362000B2-8		—	824	mA
Standby Current (RAS=CAS= $V_{IH}$ )		$I_{CC2}$	—	48	mA
RAS-Only Refresh Current* (CAS= $V_{IH}$ , RAS Cycling @ $t_{RC} = \text{min.}$ )	KMM5362000B2-6	$I_{CC3}$	—	1024	mA
	KMM5362000B2-7		—	924	mA
	KMM5362000B2-8		—	824	mA
Fast Page Mode Current* (RAS= $V_{IL}$ , CAS Cycling: $t_{PC} = \text{min.}$ )	KMM5362000B2-6	$I_{CC4}$	—	804	mA
	KMM5362000B2-7		—	704	mA
	KMM5362000B2-8		—	604	mA
Standby Current (RAS=CAS= $V_{CC}-0.2V$ )		$I_{CC5}$	—	24	mA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @ $t_{RC} = \text{min.}$ )	KMM5362000B2-6	$I_{CC6}$	—	1024	mA
	KMM5362000B2-7		—	924	mA
	KMM5362000B2-8		—	824	mA
Input Leakage Current (Any input $0 < V_{IN} < 6.5V$ , all other pins not under test=0V)		$I_{IL}$	- 240	240	$\mu\text{A}$
Output Leakage Current (Data out is disabled, $0V < V_{OUT} < 5.5V$ )		$I_{OL}$	- 20	20	$\mu\text{A}$
Output High Voltage Level ( $I_{OH} = -5\text{mA}$ )		$V_{OH}$	2.4	—	V
Output Low Voltage Level ( $I_{OL} = 4.2\text{mA}$ )		$V_{OL}$	—	0.4	V

\* NOTE:  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  are dependent on output loading and cycle rates. Specified values are obtained with the output open.  $I_{CC}$  is specified as an average current.

## KMM5362000B2/B2G

## DRAM MODULES

CAPACITANCE ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Min	Max	Unit
Input Capacitance [ $A_0-A_9$ ]	$C_{IN1}$	—	161	pF
Input Capacitance [W]	$C_{IN2}$	—	168	pF
Input Capacitance [ $\overline{RAS}_0-\overline{RAS}_3$ ]	$C_{IN3}$	—	42	pF
Input Capacitance [ $\overline{CAS}_0-\overline{CAS}_3$ ]	$C_{IN4}$	—	36	pF
Input/Output Capacitance [ $DQ_{0-7}, 9-16, 18-25, 27-34$ ]	$C_{DQ1}$	—	29	pF
Input/Output Capacitance ( $DQ_{8, 17, 26, 35}$ )	$C_{DQ2}$	—	39	pF

AC CHARACTERISTICS ( $0^\circ\text{C} < T_A < 70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ . See notes 1, 2.)

Standard Operation	Symbol	KMM5362000B2-6		KMM5362000B2-7		KMM5362000B2-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	110		130		150		ns	
Access time from $\overline{RAS}$	$t_{RAC}$		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	$t_{CAC}$		15		20		20	ns	3, 4, 5
Access time from column address	$t_{AA}$		30		35		40	ns	3, 11
$\overline{CAS}$ to output in Low-Z	$t_{CLZ}$	0		0		0		ns	3
Output buffer turn-off delay	$t_{OFF}$	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	$t_{RP}$	40		50		60		ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	15		20		20		ns	
$\overline{CAS}$ hold time	$t_{CSH}$	60		70		80		ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	$t_{RAD}$	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5		5		5		ns	
Row address set-up time	$t_{ASR}$	0		0		0		ns	
Row address hold time	$t_{RAH}$	10		10		10		ns	
Column address set-up time	$t_{ASC}$	0		0		0		ns	
Column address hold time	$t_{CAH}$	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	$t_{AR}$	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	30		35		40		ns	
Read command set-up time	$t_{RCS}$	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	$t_{RCH}$	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	$t_{RRH}$	0		0		0		ns	9
Write command hold time	$t_{WCH}$	10		10		10		ns	
Write command hold referenced to $\overline{RAS}$	$t_{WCR}$	50		55		60		ns	6

## KMM5362000B2/B2G

## DRAM MODULES

## AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KMM5362000B2-6		KMM5362000B2-7		KMM5362000B2-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command pulse width	$t_{WP}$	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	15		20		20		ns	
Data in set up time	$t_{DS}$	0		0		0		ns	10
Data in hold time	$t_{DH}$	15		15		20		ns	10
Data in hold referenced to $\overline{RAS}$	$t_{DHR}$	50		55		60		ns	6
Refresh period	$t_{REF}$		16		16		16	ms	
Write command set-up time	$t_{WCS}$	0		0		0		ns	8
$\overline{CAS}$ set-up time ( $\overline{C}$ -B- $\overline{R}$ refresh)	$t_{CSR}$	10		10		10		ns	
$\overline{CAS}$ hold time ( $\overline{C}$ -B- $\overline{R}$ refresh)	$t_{CHR}$	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$		35		40		45	ns	3
Fast page mode cycle time	$t_{PC}$	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page)	$t_{CP}$	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	$t_{RASP}$	60	200,000	70	200,000	80	200,000	ns	

## NOTES

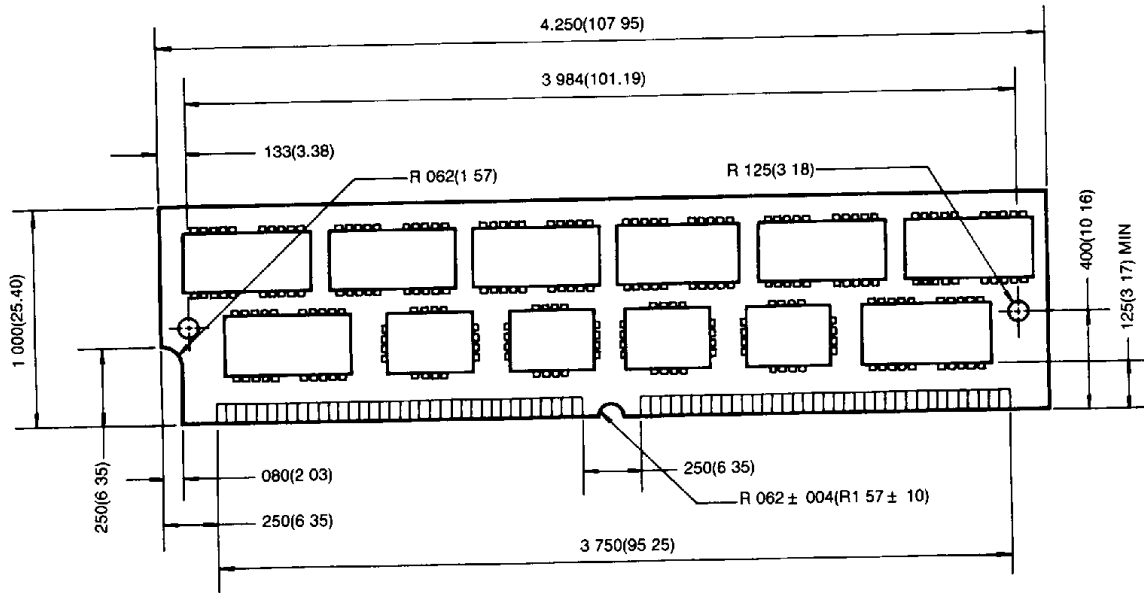
1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved.
2.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\min)$  and  $V_{IL}(\max)$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$ .
6.  $t_{AR}$ ,  $t_{WCR}$ ,  $t_{DHR}$  are referenced to  $t_{RAD}(\max)$ .
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{WCS}$  is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$  the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles.
11. Operation within the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled by  $t_{AA}$ .

**KMM5362000B2/B2G**

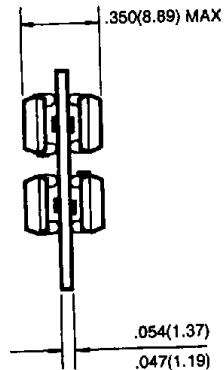
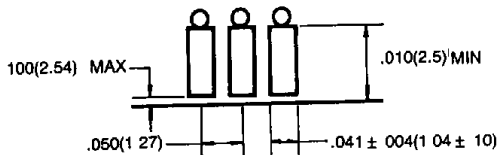
**DRAM MODULES**

**PACKAGE DIMENSIONS**

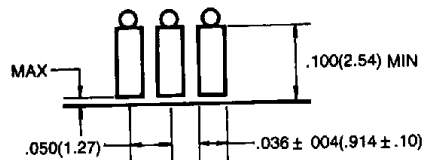
Units: Inches (millimeters)



KMM5362000B2G: DETAIL OF CONTACTS (Gold Plating Lead)



KMM5362000B2: DETAIL OF CONTACTS (Solder Plating Lead)



Tolerances: ± .005 (.13) unless otherwise specified