DATA SHEET

FXA 1012
Frame Transfer CCD Image Sensor

Objective specification
File under Image Sensors

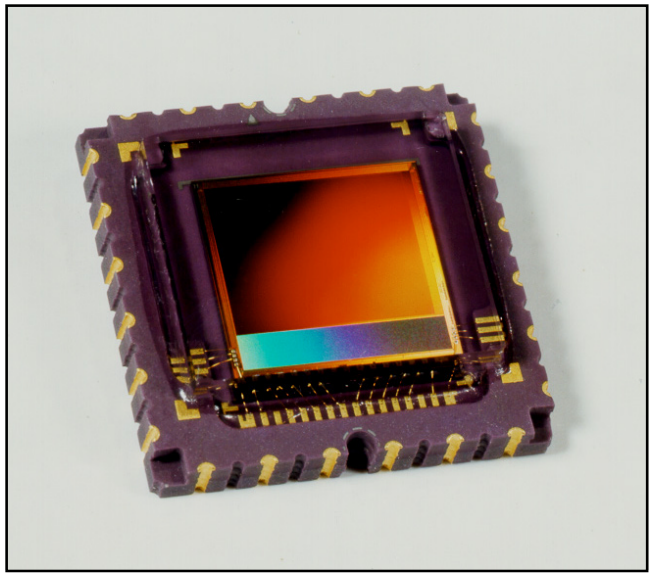
2000 January 7

Philips Semiconductors

PHILIPS

Frame Transfer CCD Image Sensor FXA 1012

- **2M active pixels (1616H x 1296V)**
- **2/3-inch type optical format**
- **Still and monitor modes**
- **RGB Bayer pattern colour filters**
- **Progressive scan**
- **Excellent anti-blooming (Vertical Overflow Drain)**
- **High dynamic range (>70dB)**
- **High sensitivity**
- **Low dark current and low fixed pattern noise**
- **Low read-out noise**
- **Variable electronic shuttering**
- **Data rate up to 25 MHz, 5 frames/s**
- **Small outline LCC package**
- **Low cost**



Description

The FXA 1012 is a colour frame-transfer CCD image sensor designed for consumer digital photography applications. The combination of high speed and a high linear dynamic range of over 10 true bits makes this device the perfect solution for use in compact high quality imaging applications. Two modes of operation provide both a monitoring image for LCD screens, and a full resolution, zero-smear still image with excellent colour rendition. The device structure is shown in figure 1.

Device structure

Optical size:	8.16 mm (H) x 6.53 mm (V)	
Chip size:	9.49 mm (H) x 9.32 mm (V)	
Pixel size:	5.1 µm x 5.1 µm	
Active pixels:	1616 (H) x 1296 (V)	
Total no. of pixels:	1688 (H) x 1324 (V)	
Optical black pixels:	Left: 2	Right: 70
Optical black lines:	Top: 12	Bottom: 12
Total no. of storage lines:	298	
Dummy register cells:	8	

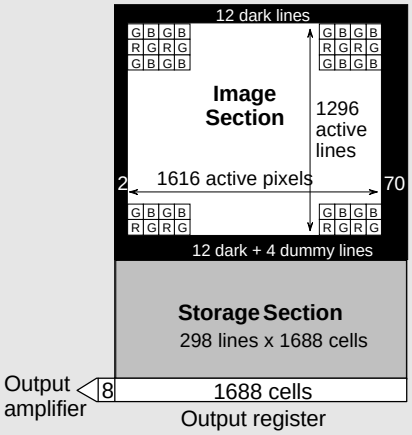


Figure 1 - Device structure

Architecture of the FXA 1012

The FXA 1012 consists of an open image section and a storage section with an optical light shield. An output register and amplifier are located below the storage section for read-out.

The optical centres of all pixels in the image section form a square grid. The image area has RGB Bayer colour filter pattern. The charge is generated and integrated in the image section. This section is controlled by four image clock phases (A1 to A4). After the integration time the image charge is shifted one line at a time to the storage section.

The storage section is controlled by four storage clock phases (B1 to B4). In the still mode the image information is transported straight through the storage section to the horizontal output register. In the monitoring mode subsampling of the image is performed at the image-to-storage transition and the subsampled image is stored in the storage section. The stored image is shifted one line at a time into the horizontal output register.

In the next active line time the pixels are transported towards the output amplifier. Four clock phases (C1 to C4) control the pixel transport in the output register. In the output amplifier the charge packets are dumped one by one on a floating diffusion area. The voltage of this area is sensed and buffered by a three-stage FET source-follower. Figure 2 shows the detailed internal structure.

IMAGE SECTION	
Image diagonal (active video only)	10.4 mm
Aspect ratio	5:4
Active image width x height	8.24 x 6.61 mm^2
Pixel width x height	5.1 x 5.1 μm^2
Image clock pins	A1, A2, A3, A4
Capacity of each clock phase	5.4 nF per pin
Number of active lines	1296
Number of black reference lines	24 (12+12)
Number of dummy lines	4
Total number of lines	1324
Number of active pixels per line	1616
Number of black reference pixels per line	72 (2+70)
Total number of pixels per line	1688

STORAGE SECTION	
Cell width x height	5.1 x 5.1 μm^2
Storage clock pins	B1, B2, B3, B4
Capacity of each clock phase	1.5 nF per pin
Number of cells per line x number of lines	1688 x 298

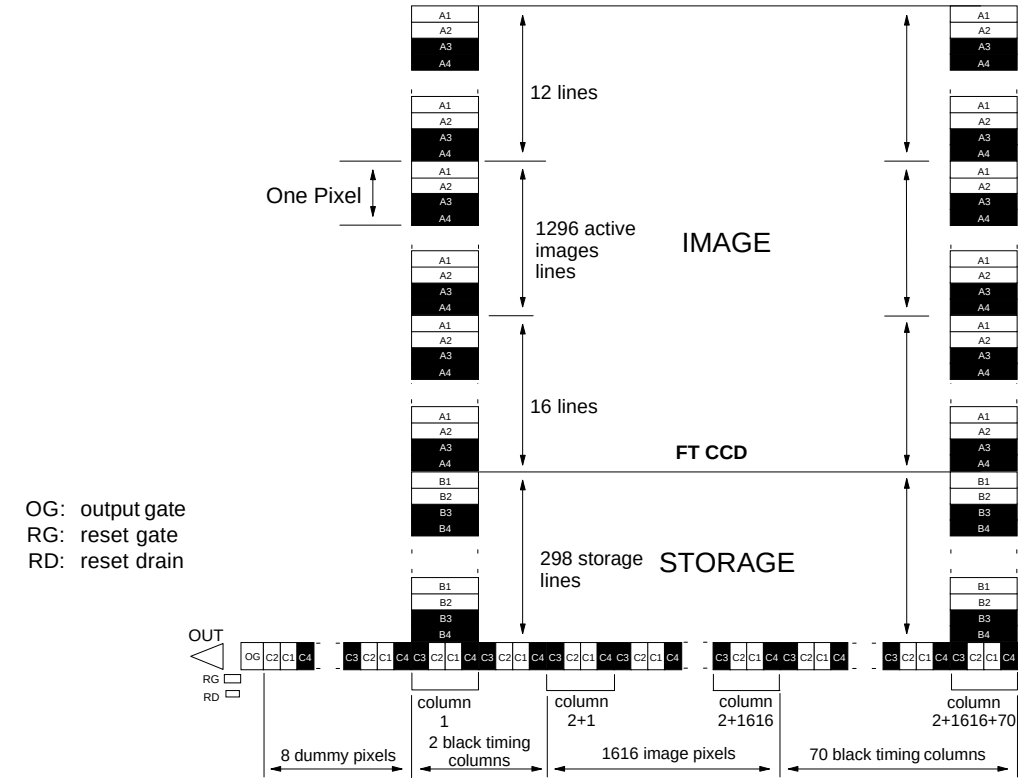
OUTPUT REGISTER	
Number of dummy cells	8
Total number of register cells	1696
Output register clock pins	C1, C2, C3, C4
Capacity of each clock phase	60 pF per pin
Reset Gate (RG) capacity	15 pF
Output stage	3-stage source follower (open source)

Operational modes

The FXA 1012 is designed for high-resolution digital photography with real time monitoring at reduced resolution. Two different modes of operation make this possible.

In the still picture mode the high-resolution image is read-out directly. A mechanical shutter ensures a 100% smear-free image with a resolution of 1600 (H) x 1280 (V).

In the monitoring mode, images with reduced vertical resolution are produced that are suitable for LCD displays. These images can have for example, 120, 240 or 256 lines at up to 40 images per second.



A1, A2, A3, A4: clocks of image section
B1, B2, B3, B4: clocks of storage section
C1, C2, C3, C4: clocks of horizontal register

Figure 2 - Detailed internal structure

Specifications

Absolute Maximum Ratings	Min.	Max.	Unit
GENERAL:			
storage temperature	-40	+80	°C
ambient temperature during operation	-20	+60	°C
voltage between any two gates	-20	+20	V
DC current through any clock phase (absolute value)	-0.2	+2.0	µA
OUT current (no short circuit protections)	0	4	mA
VOLTAGES IN RELATION TO VPS:			
VNS, RD	-0.5	+30	V
all other pins	-10	+25	V
VOLTAGES IN RELATION TO VNS:			
RD	-10	+0.5	V
VPS	-30	+0.5	V
all other pins	-30	+0.5	V

DC Conditions		Min. [V]	Typical [V]	Max. [V]	Max. current [mA]
VNS[1]	N substrate	20	24	28	2 [2]
VPS	P substrate	6	7	9	2
SFD	Source Follower Drain	19	20	21	5.5 [3]
SFS	Source Follower Source	0	0	0	1
OG	Output Gate	3.5	4	4.5	-
RD	Reset Drain	19	20	21	-
		Min.	**Typical**	**Max.**	**Pin**
	Number of adjustments	0	0	1	VNS

[1] To set the VNS voltage for optimal Anti-Blooming (vertical overflow drain), it should be adjustable between minimum and maximum values.
[2] Currents INS and IPS are specified at overexposure of 100 x Qmax.
[3] Measured with Rload = 3.3 kOhms.

AC Clock Level Conditions	Min.	Typical	Max.	Unit
IMAGE CLOCKS:				
A-clock amplitude	11	12	13	V
A-clock low level		0		V
STORAGE CLOCKS:				
B-clock amplitude	11	12	13	V
B-clock low level		0		V
HORIZONTAL AND RESET CLOCKS:				
C-clock amplitude	4.5	5	5.5	V
C-clock low level C1, C3		0		V
C-clock low level C2, C4	2.5	3	3.5	V
Reset Gate (RG) amplitude	4.5	5	5.25	V
Reset Gate (RG) high level	21	22	23	V
VNS PULSE:				
Charge Reset (CR) pulse on VNS	4.5	5	5.5	V

Timing diagrams (for default operation)

AC Characteristics	Min.	Typical	Max.	Unit
Horizontal frequency			25	MHz
Vertical frequency		1.56[1]		MHz
Charge Reset (CR) time	10	12	14	µs
Rise and fall times: image clocks (A)	10	20		ns
register clocks (C)[2]	3	5	Tp/8 [3]	ns
reset gate (RG)	3	5	Tp/8	ns

[1] Typical value for monitor mode.
[2] Duty cycle = 50%
[3] Tp is pulse period of C clocks

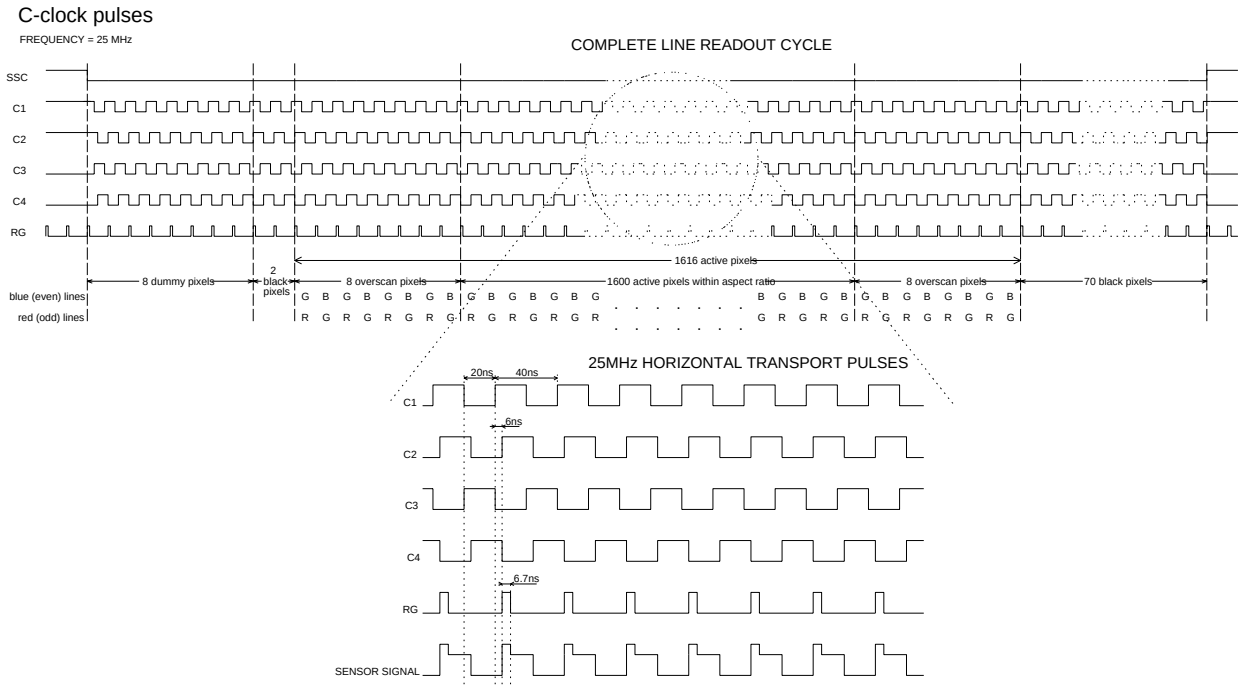


Figure 3 - Timing diagram for horizontal pulses

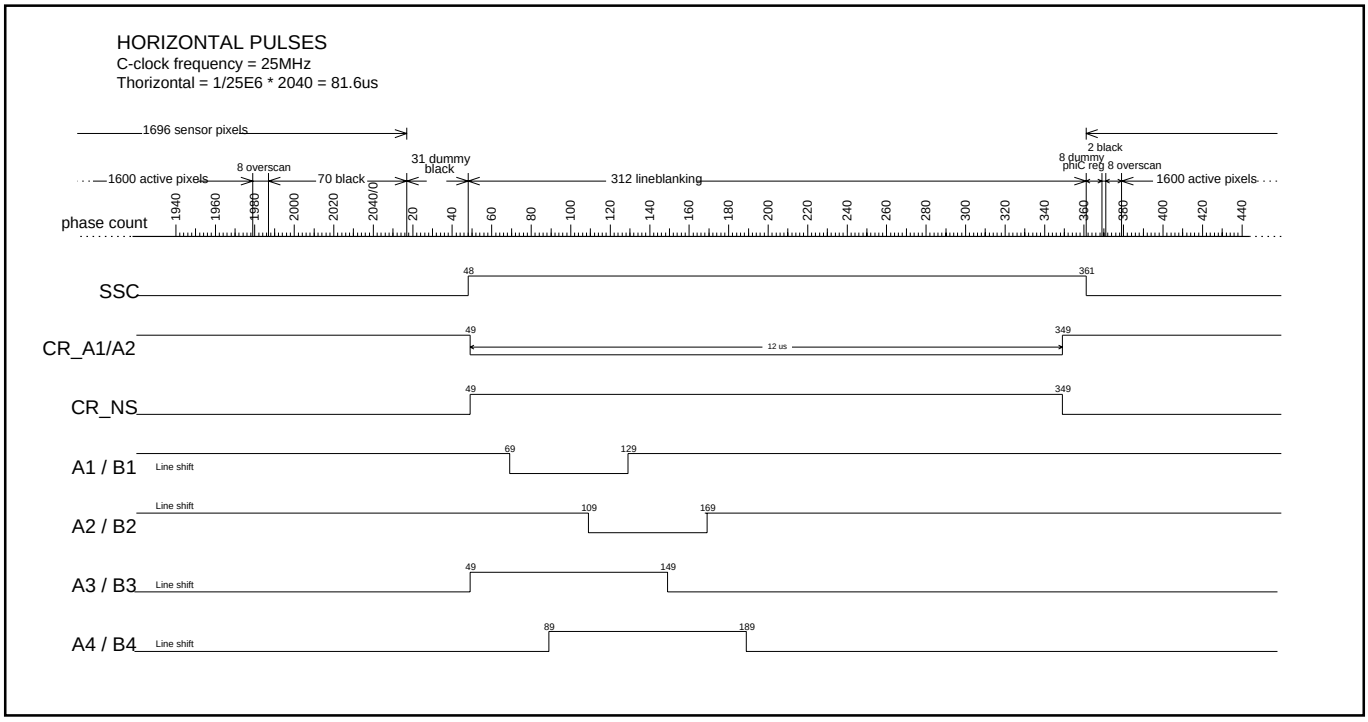


Figure 4 - Pulse timing diagrams for vertical clocks during line blanking

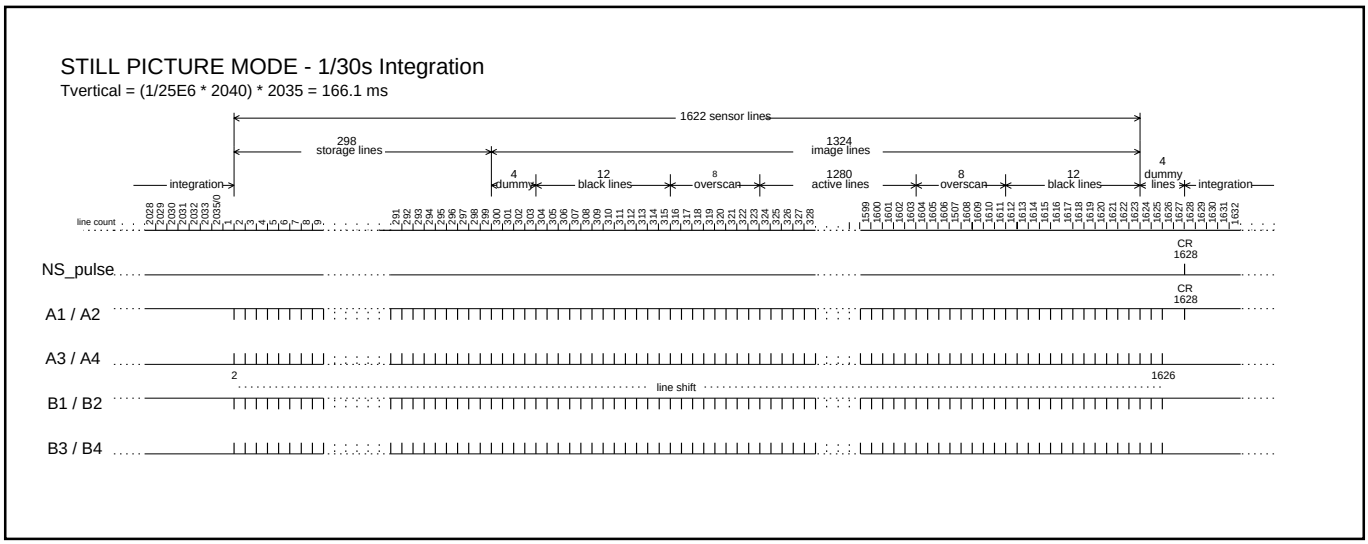


Figure 5 - Still picture mode timing diagrams

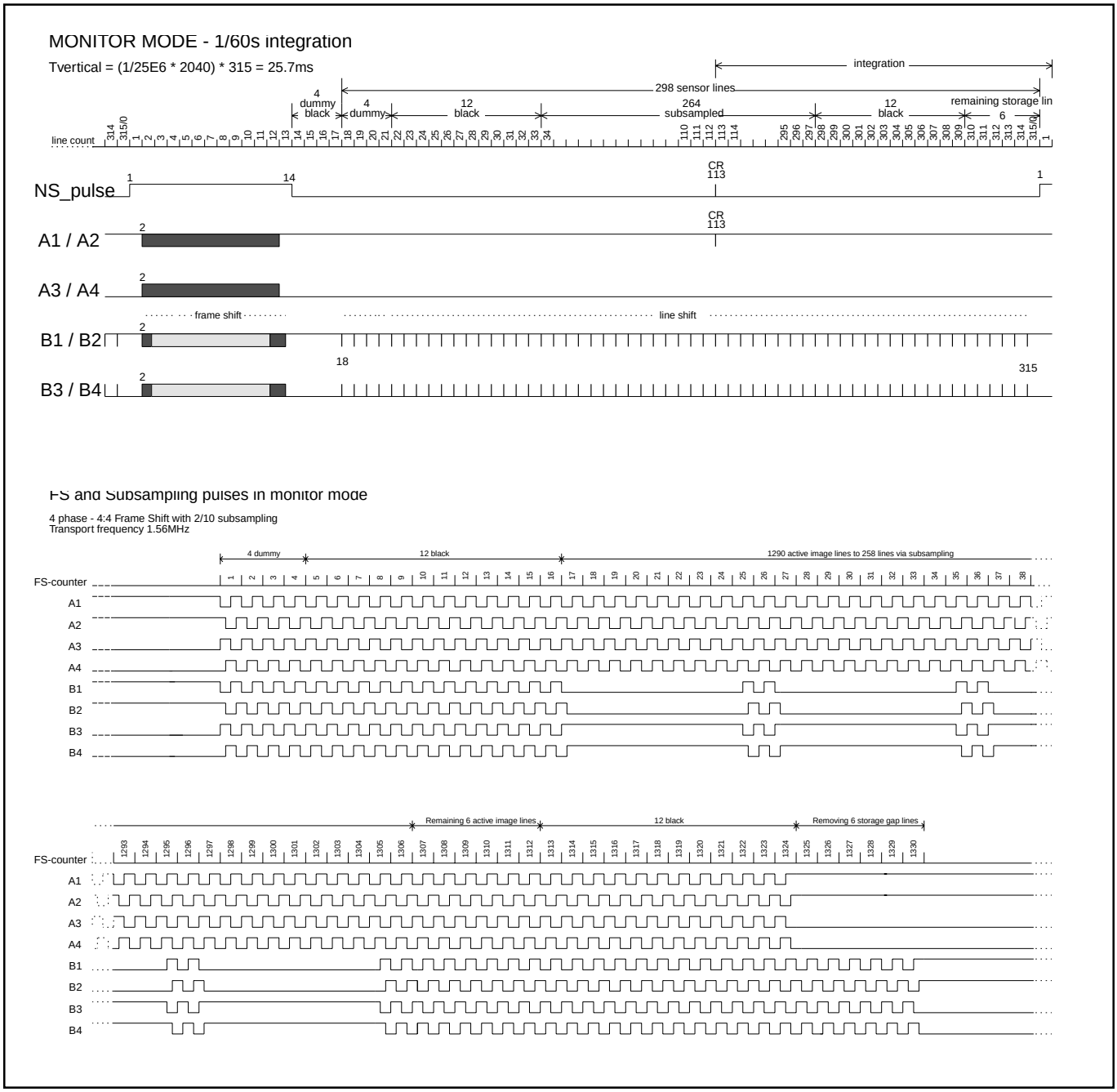


Figure 6 - Monitor mode timing diagrams

Pixel timing

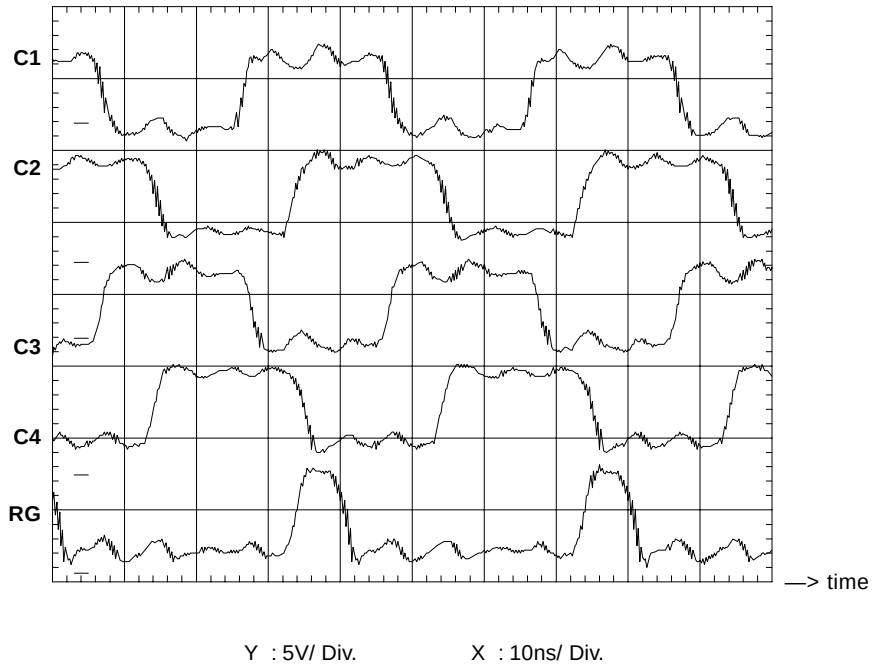


Figure 7 - Start horizontal readout

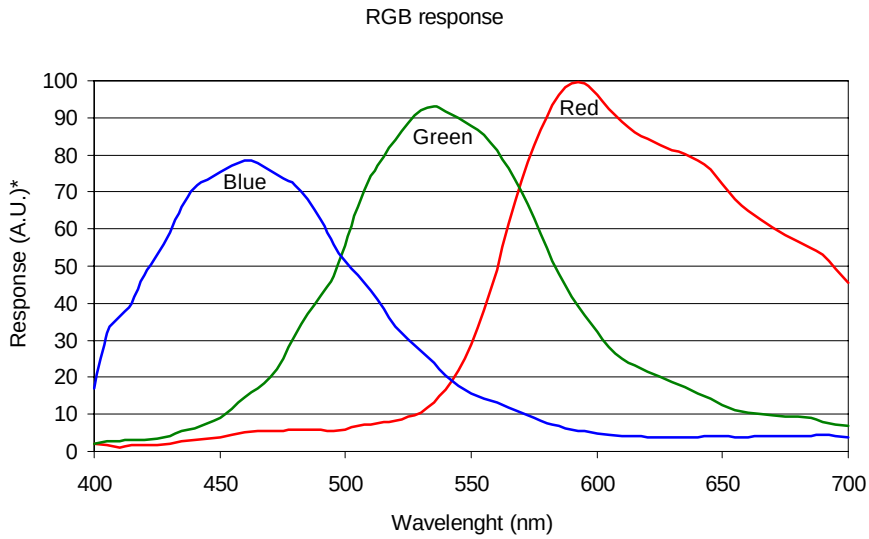
Performance

The test conditions for the performance characteristics in the still mode of operation are as follows:

- All values are measured using typical operating conditions.
- Integration time = 1/30 sec (unless specified otherwise).
- Test temperature = 60°C (333K).
- The light source is a 3200K lamp with a 1.7mm thick BG40 infrared cut-off filter; F=16.
- Vertical Anti-Blooming condition
- Horizontal transport frequency = 25MHz.

Performance Characteristics	Min.	Typical	Max.	Unit
Charge Transfer Efficiency [1] vertical		0.999997		
Charge Transfer Efficiency [1] horizontal		0.999997		
Image lag			0	%
Sensitivity, green S_G [2]		295		mV/lux.s
Sensitivity, red S_R [2]		240		mV/lux.s
Sensitivity, blue S_B [2]		175		mV/lux.s
Sensitivity Ratio S_G / S_R		1.25		
Sensitivity Ratio S_G / S_B		1.7		
Sensitivity Ratio S_R / S_B		1.4		
Shading per colour plane [3]		2		%
Differential colour shading [4]				%
PRNU per colour plane		0.8	2.5	%
Green–green difference [5]			5	%
Power consumption (Still mode)	40	50	60	mW
Power consumption (Monitoring mode)				mW
Full-well capacity saturation level (Q_{max}) [6]	35	45	55	x 10^3
Saturation signal	720	1000	1500	mV
Dynamic range at 20°C : 20log(Q_{max}/noise electrons)		72		dB
Overexposure [7] handling		100		x Q_{max} level

[1] Charge Transfer Efficiency values are expressed as the value per gate transfer.
[2] The sensitivity when a light source directly illuminates the CCD.
[3] Shading is defined as the one-σ value of the pixel output distribution expressed as a percentage of the mean value output (low-pass image).
[4] Difference in shading between the four colour planes, with standard imaging condition, still mode.
[5] Difference in average green signal between ‘green in red line’ and ‘green in blue line’, with standard imaging condition, still mode
[6] Q_{max} is determined from the lowpass filtered image.
[7] Overexposure over entire area while maintaining good Vertical Anti-Blooming (VAB). It is tested by measuring the dark line.



*Arbitrary units

Figure 8 - RGB response

Output Buffer	Min	Typical	Max	Unit
Conversion factor at output node	18	20	25	µV/el.
Supply current		4		mA
Bandwidth		95		MHz
RMS readout noise @ 5MHz bandwidth after CDS		12	15	el.

Dark Condition at 60°C [1]	Min.	Typical	Max.	Unit
Average no. of dark signal electrons per pixel after 1/30 sec integration		25		electrons
Dark signal shading		1		mV
Dark current level @ 60° C		0.3	0.6	nA/cm^2
Fixed Pattern Noise [2] (FPN) @ 60° C		15	25	electrons

[1] Typical operating conditions (Image capture mode; 60°C; 1/30s exp. time).
[2] FPN is the one-σ value of the highpass image.

Application information

Current handling

One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from over-exposure), free electrons are drained to VNS. No current should flow into VPS. During overexposures a total current 0.5 to 1mA through VPS may be expected. The PNP emitter follower in the circuit diagram (figure 9) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During overexposures a total current of 0.5 to 1mA through VNS may be expected. The NPN emitter follower in the circuit diagram meets these current requirements. The clamp circuit, consisting of the diode and electrolytic capacitor, enables the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages

All DC voltages (not VNS, which has additional CR pulses as described above) should be decoupled with a 100nF decoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons building up the charge packets that will reach the floating diffusion only add up to a small current, which will flow through VRD. Therefore a large series resistor in the VRD connection may be used.

Output

To limit the on-chip power dissipation, the output buffer is designed with open source output. The output should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 400 Ohm) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is prevented by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be decoupled properly to suppress the Miller effect from the base-collector capacitance. A CCD output load resistor of 3.3 kΩ typically results in a bandwidth of 95MHz.

Device protection

The output buffer or VNS of the FXA 1012 is likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 6mA. Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-substrate, we are dealing with some parasitic NPN transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 9.

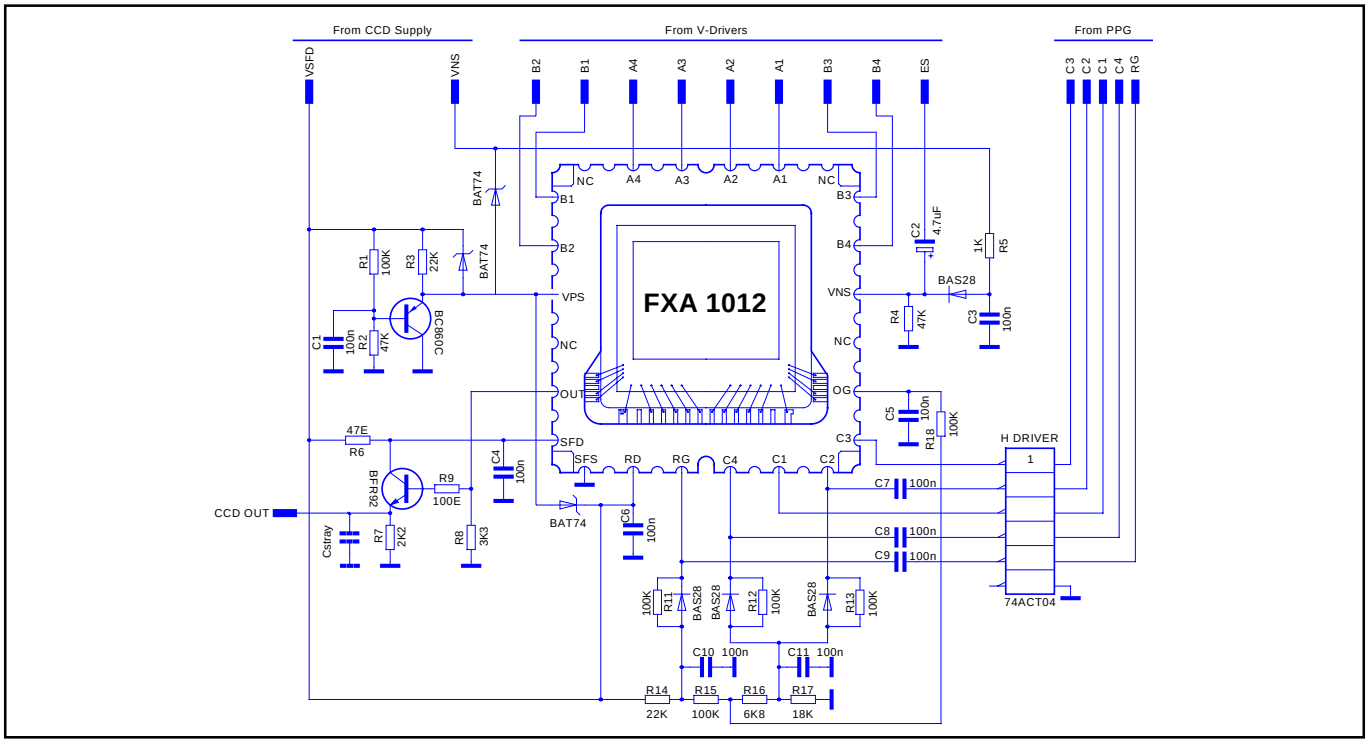


Figure 9 - Application diagram to protect the FXA 1012

Peripheral ICs
To allow compact and low-cost applications, use of the following peripheral circuits for the FXA 1012 is suggested:

- Pulse Pattern Generator
  The PPG (pulse pattern generator) delivers all the pulses, at logic level, to drive the vertical clocks of the CCD. For this sensor, the PPG is included in the DSP SAA8122 or separately in the Timing Generator SAA8103.

- Vertical Drivers + DC/DC Converter
  The vertical drivers convert the 3.3V or 5V logic pulses from the PPG to 12V analog pulses to drive the vertical clocks of the CCD. The recommended driver is the Philips TDA9991.

- CDS - AGC - ADC
  The combined CDS (correlated double sampling) - AGC (automatic gain control) and ADC (10 bit analog-to-digital convertor) is the easiest way to link the output of the CCD to a DSP (digital signal processor). Philips Semiconductors # TDA8783

- DSP
  A dedicated DSP has been developed that can handle the image format and different modes of the FXA 1012. Philips Semiconductors # SAA8122.

Special modes of operation
Monitor mode with 240 lines vertical resolution is achieved with 1:5 subsampling, yielding 1200/5 = 240 lines. When 1:4 subsamlping is applied, an image with 288 lines vertical resolution is obtained.

Device Handling

An image sensor is a MOS device which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in a CCD image sensor is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remain undamaged. When handling the sensor, use fingercots.

To remove the protective tape from the cover glass, use the following procedure:
- do not scratch or tear off the protective tape before mounting.
- peel off the tape slowly.
- the use of an ionised air blower is recommended when peeling off the tape.
- once peeled off, do not reuse the tape.

To clean stains from the package surface, use a cotton stick soaked in ethanol. Wipe carefully in order not to scratch the glass surface.

Dry rubbing of the cover glass may cause electro-static discharges which can destroy the device.

Soldering information
The CCD package temperature must not exceed 150°C. Soldering iron temperature should be under 300°C when mounting a CCD on a printed circuit board. Aim for a soldering time of 3 seconds per pad. Use a soldering iron that has an adjustable temperature control function (that is grounded) that holds the soldering iron tip at a constant temperature.

Pin configuration

Pin Number	Symbol
1	a3
2	a4
3	NC
4	b1
5	b2
6	vps
7	NC
8	out
9	sfd
10	sfs
11	rd
12	rg

Pin Number	Symbol
13	c4
14	c1
15	c2
16	c3
17	og
18	NC
19	vns
20	b4
21	b3
22	NC
23	a1
24	a2

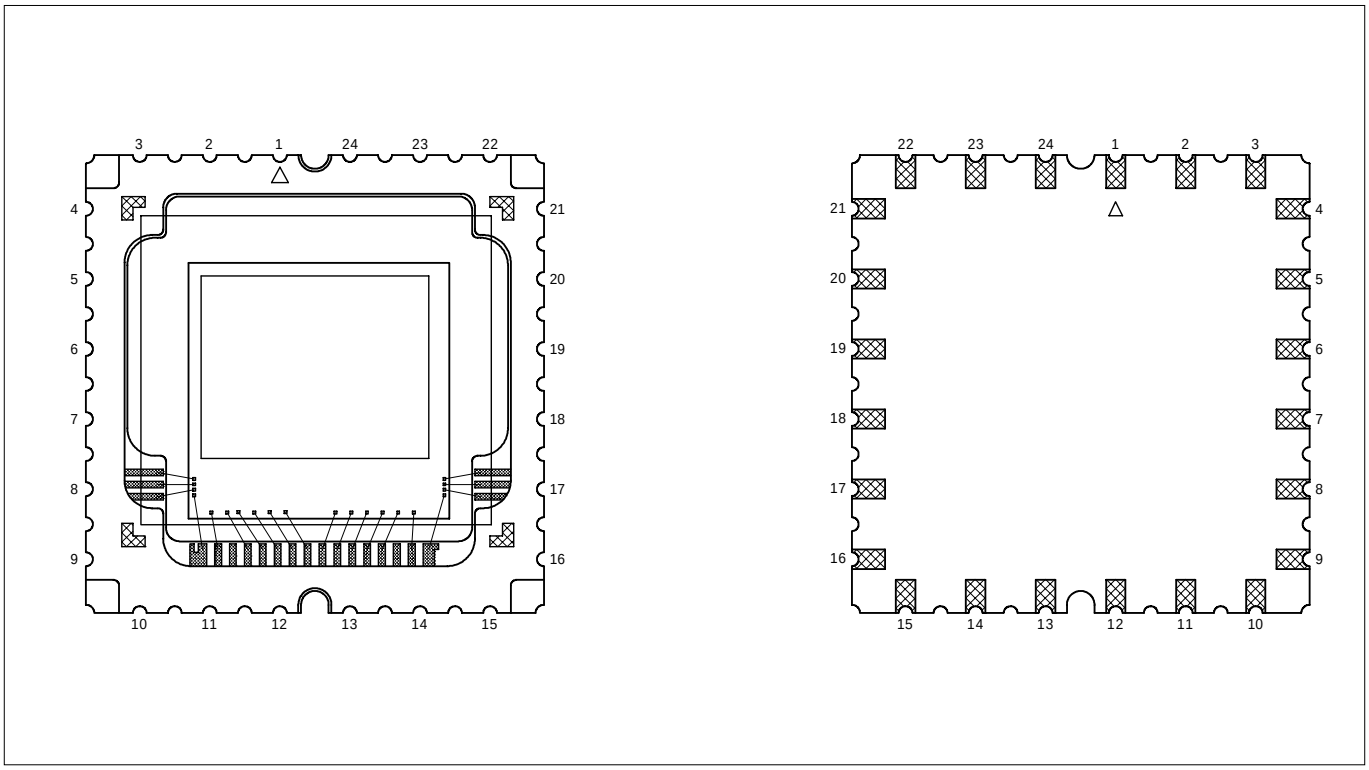
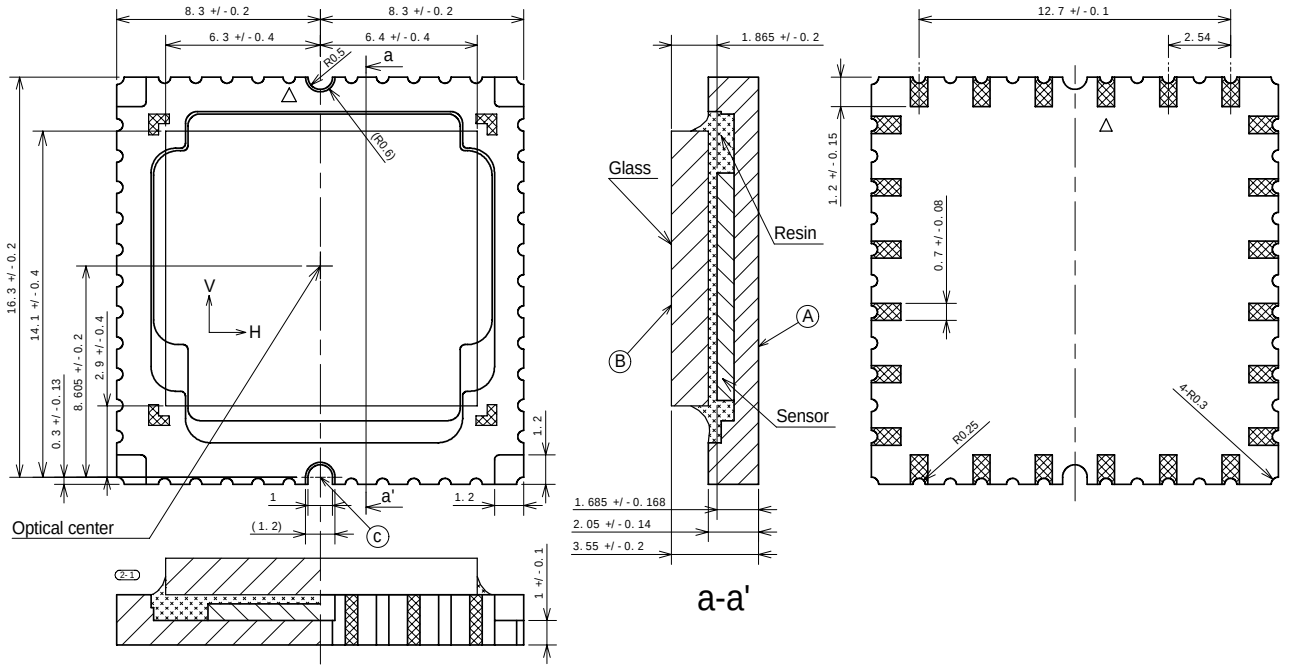


Figure 10 - Pin configuration

Package information



1. The bottom of the package [A] is the height reference.
2. The height from the bottom [A] to the effective image area is 1.685 +/-0.168mm.
   The height from the top of the cover glass [B] to the effective image area is 1.865 +/-0.2mm.
3. The tilt of the effective image area relative to the height reference is less than 0.095mm.
4. The thickness of the Au plating is more than 1.0um.
   The thickness of the Au plating is less than 3.0um.
5. The point [C] is the origin of H&V direction.
6. The center of effective image area relative to [C] is (V,H)=(8.605,0)+/-0.2mm.
7. The rotation angle of the effective image area relative to H and V is less than +/-1.5 degrees.
8. The rotation angle of the cover glass relative to H and V is less than +/-2degrees.
9. The thickness of the cover glass is 1.5 +/-0.05mm, and the refractive index 1.5.
10. The refractive index of the resin is 1.5.
11. The tolerances that are not shown are +/-0.13mm.
12. D=2.18 +/-0.44mm
    D: Distance between left edge of imaging area and left edge of cover glass.
    +/-0.44mm means 4sgm = 0.44mm.
13. No horizontal force is allowed to cover glass lid.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

Figure 11 - Mechanical drawing of the FXA 1012 package

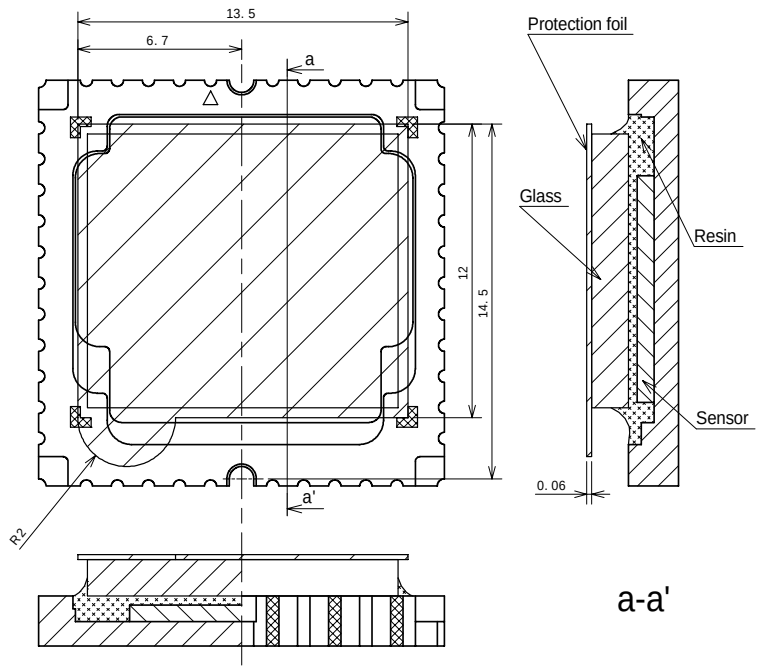


Figure 12 - Protective foil on top of cover glass

Order codes

The sensor can be ordered using the following code:

FXA 1012 sensor	
Description	**Order Code**
FXA 1012 WC	9352 670 10117

You can contact the Image Sensors division of Philips Semiconductors at the following address:

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