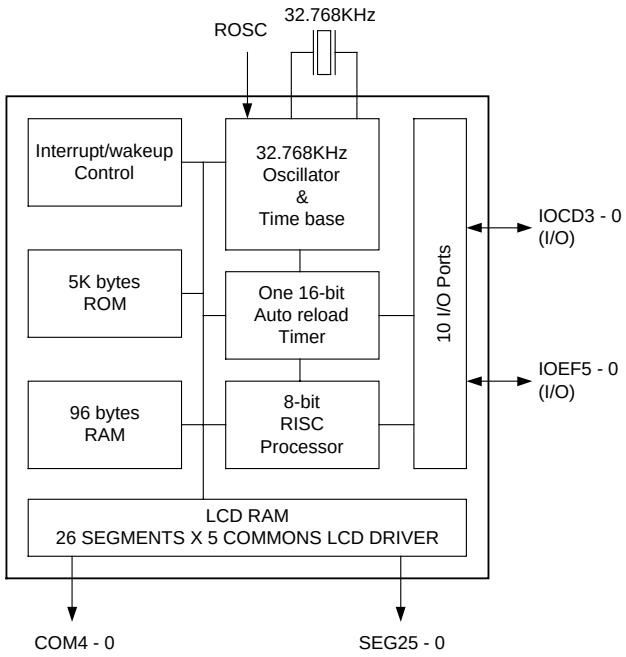
GENERAL DESCRIPTION

The SPL09A is a CMOS 8-bit single chip microprocessor, which contains RAM, ROM, I/Os, interrupt/wakeup controller, timer and automatic display controller/driver for LCD. This chip is designed not only low power consumption but also provides standby mode controlled by software for power saving. It is very suitable for LCD hand-held products.

FEATURES

- Built-in 8-bit CPU
  - 96 bytes SRAM
  - 5K bytes ROM
  - Max. CPU frequency: 2.0MHz @ 3V
  - CPU clock frequency is programmable, 1/2,1/4,1/8,or 1/16 of RC oscillator frequency
  - Wide operating voltage : 2.4V - 3.4V
    3.6V - 5.5V
  - Provide 6 INT sources
- Built-in 32.768KHz crystal oscillator
  - Crystal oscillator switches from strong to weak mode automatically
  - Internal time base generator
- Built-in RC oscillator
  - Only one resistor is needed
- One 16 bits timer / counter
- LCD controller
  - Max. 26 segments x 5 commons
  - 1/2, 1/3 bias ; 1/2, 1/3, 1/4,1/5 duty
  - Provides useful display operation mode
- Low Voltage Reset
  - Provides 2.2V low Voltage reset
- Low power consumption
  - Operating current: 300μA/1.0MHz @ 3V
  - Provides standby function (stop all oscillators)
  - Very low current in Halt mode
    In Halt mode: I_{HALT} < 1μA @ 3V
- 10 general purpose I/Os
  - 6 IO pins support Key wake-up mode
  - 2 IO pins are shared with LCD segments
  - 1 IO pin is shared with LCD common

BLOCK DIAGRAM



FUNCTION DESCRIPTION

SPL09A provides 5K byte ROM with a LCD driver, which is capable to control 5 commons and 26 segments. The power consumption of SPL09A is very low in both Standby mode and Halt mode. It is very appropriate for LCD type hand-held product.

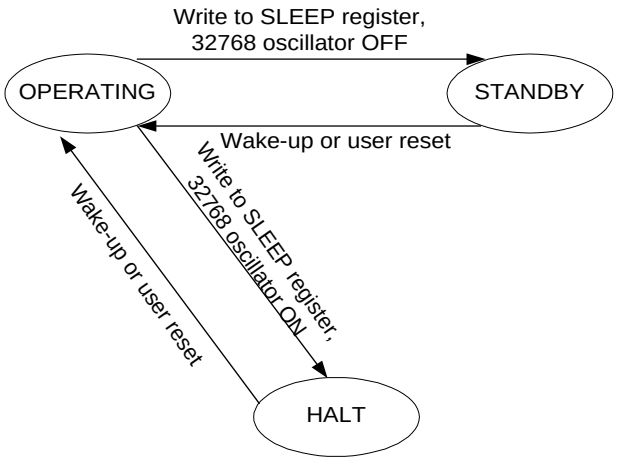
■ OPERATING STATES

The SPL09A provides three operating states: standby, halt, and operating. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating state, all modules (CPU, 32768 oscillator, timer/counter, LCD driver…) are activated. Writing the SLEEP register ($09) enters the Halt/standby State. There are four wake-up sources in SPL09A: port IOEF wake-up, TIMR0 wake-up, 4Hz/8Hz/16Hz/32Hz wake-up and 2Hz/1Hz wake-up. If any wake-up event occurs, execution of the next instruction continues in the operating state.

In standby mode, all modules will be shut down, and RAM and I/Os remain in their previous states. The current consumption is minimized. By writing to SLEEP register but keeps 32768 oscillator running, the system is in HALT State. CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up in HALT State. The 32768 related modules (timer/counter, LCD driver…) may remain active in the halt state. Following figure is a state diagram for the SPL09A.



State Diagram of SPL09A

After the chip is awakened from Halt/standby State, CPU will continue to execute the next instruction. The RAM and I/O will not be affected by wake-up.

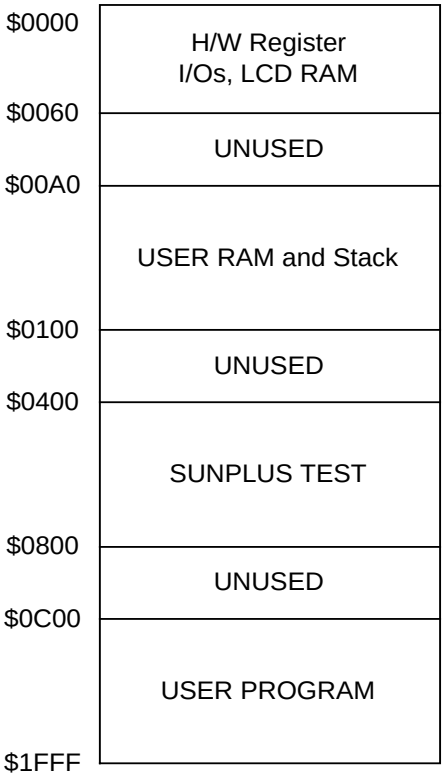
■ MAP OF MEMORY AND I/Os

* I/O PORT:
  - PORT IOCD $0004
    IOEF $0005
  - I/O CONFIG $0000
    $0035
    $0006

* NMI SOURCE
  - INT1 (from TIMER 0)

* INT SOURCE
  - INT0 (from TIMER 0)
  - 2KHz
  - T16Hz (4Hz/8Hz/16Hz/32Hz)
  - 128Hz
  - EXT INT (from IOCD0 pin)
  - T2 Hz (2Hz/1Hz)

*MEMORY MAP (From ROM view)



■ TIME-SETTING REGISTER RELATED

Writing to TIME-SETTING register can program the time source of CPU wake-up and interrupt. For example, the programmer can change 2Hz wake-up and interrupt into 1Hz wake-up and interrupt by writing 80H into $0A. Thus, the system will wake up to service every second. Also, T16Hz (one of counter's clock source and wake-up & interrupt) can be one of 4Hz, 8Hz, 16Hz or 32Hz by setting bit0 and bit1 of TIME-SETTING register ($0A). At power on state, the default value of T16Hz is 4Hz and T2Hz is 2Hz.

■ WATCHDOG TIMER (WDT)

An on chip watchdog timer is available on SPL09A. The WDT is designed for recovering from system abnormal operation. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. Writing the specified value 0FH to port $0F can clear the WDT. Note that the WDT only works when 32768 Hz clock is available.

■ TIMER/COUNTER

SPL09A contains one 16-bit timer/counter, TM0 respectively. In the timer mode, TM0 are auto-reload up-counters. When the timer overflows from $FFFF to $0000, the carry signal will generate the INT signal if the corresponding bit is enabled in INT ENABLE register ($0D). The timer will automatically reload the value assigned by the program and up count continuously. If TM0 is specified as a counter, the user can reset the counter by loading 0 into register $10 and $11 and loading 0 into the counter by writing to $12. After the counter is activated, the counter's value can also be read from above registers ($10 and $11) and the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter are selected as the following:

TIMER/COUNTER		ADDR.	CLOCK SOURCE
TM0	16-BIT TIMER	$0010 $0011 $0012	R-oscillator Output, VDD (0Hz)
	16-BIT COUNTER	$0010 $0011 $0012	Clock source 1: IOCD1, VDD,T16Hz,128Hz Clock source 2: IOCD0, VDD, Crystal oscillator, R-oscillator Output. Note:T16Hz can be one of 4Hz,8Hz,16Hz or 32Hz by setting $0A (time-setting register)
MODE SELECT REGISTER		$000B	Select TM0 configuration

■ LCD CONTROLLER/DRIVER

SPL09A contains a total of 130 dots LCD controller and driver. Programmers can set the LCD configuration (bias, duty, display mode) by writing to LCD control register ($18). Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. For the power saving mode, programmer can set the LCD display option to turn the LCD display off by writing to control register ($18). The LCD driver in SPL09A is designed to fit most LCD's specifications. It can either be programmed as 1/2 or 1/3 bias. The duty is also programmable as 1/2, 1/3, 1/4 or 1/5 duty.

MASK OPTIONS

■ 32768 CRYSTAL OSCILLATOR

— X'TAL

— R-oscillator

■ **LOW VOLTAGE RESET (2.2V)**

— Enable

— Disable

■ **LCD CHARGE PUMP CLOCK RATE**

— 32KHz

— 4KHz

■ **I/O AND LCD DRIVER**

There are some examples shown as below:

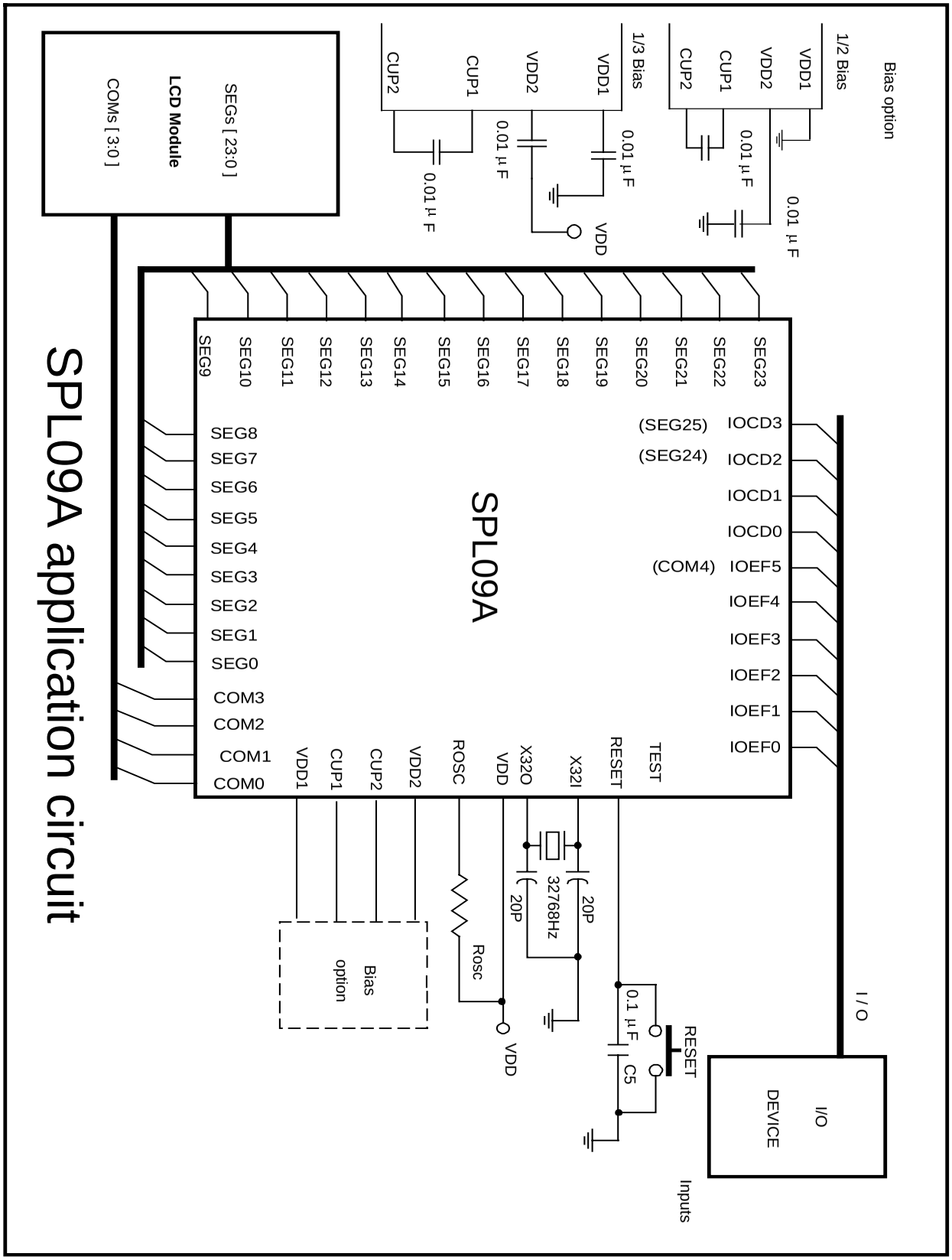
LCD Dots	Segment	Common	Input/Output	Input/Output
130	26	5	IOCD1 - 0	IOEF4 - 0
125	25	5	IOCD2 - 0	IOEF4 - 0
96	24	4	IOCD3 - 0	IOEF5 - 0

Each of input/output ports IOCD3 - 2 can be optioned to LCD segments independently, and IOEF5 can be optioned to LCD commons.

PIN DESCRIPTION

Mnemonic	Type	Description
SEG23 – 0	O	LCD driver segment output
COM3 – 0	O	LCD driver common output
IOEF5 – 0	I/O	I/O port (IOEF5 can be optioned to COM4)
IOCD3 – 0	I/O	I/O port (IOCD3 can be optioned to SEG24, and IOCD2 can be optional to SEG25)
ROSC	I	R-Oscillator input, connect to VDD through resistor
RESET	I	System reset input
X32I	I	32.768KHz crystal input (provide LCD frequency)
X32O	O	32.768KHz crystal output
TEST	I	TEST MODE
VDD	I	Positive supply voltage input
VSS	I	Ground Input
VDD1, VDD2	I	Inputs for setting LCD Bias
CUP1, CUP2	I	Inputs for setting LCD Bias
LPWR	O	Regulated voltage output terminal for oscillators

APPLICATION NOTE



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