Wireless Components

Dual LNA

PMB 2362 Version 1.1

Specification January 2000

preliminary

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Product Info

General Description

The PMB2362 is a dual band LNA circuit with excellent performance and minimum component count for GSM900 and GSM1800.

Package

Features

- Worldclass B6HF technology, f_T = 25GHz
- Lowest external component count
- Extreme small outline P-TSSOP-10-2 package with heat sink for grounding
- Both LNAs with prematched input, only 2 external matching components required
- GSM900 LNA output matched to 50 Ohm
- Both LNAs with switchable gain, 20dB gain step
- LNA1: 17dB gain, 1.5dB noise figure @ 0.95GHz
- LNA2: 19dB gain, 2.0dB noise figure @ 1.85GHz
- Supply voltage range from 2.7V to 3.6V
- Power down function
- Temperature range -40° to 85°C

Application

- Dual band wireless frontends GSM900/1800
- Excellent combination with Infineon GSM single chip SMARTi PMB 6250

Ordering Information

Type	Ordering Code	Package
PMB 2362 V1.1	T2362-XV11-P1-7600	P-TSSOP-10-2

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2 Product Description

Contents of this Chapter

2.1 General Description

The PMB2362 is a dual band LNA circuit with excellent performance and minimum component count for GSM900 and GSM1800.

2.2 Features

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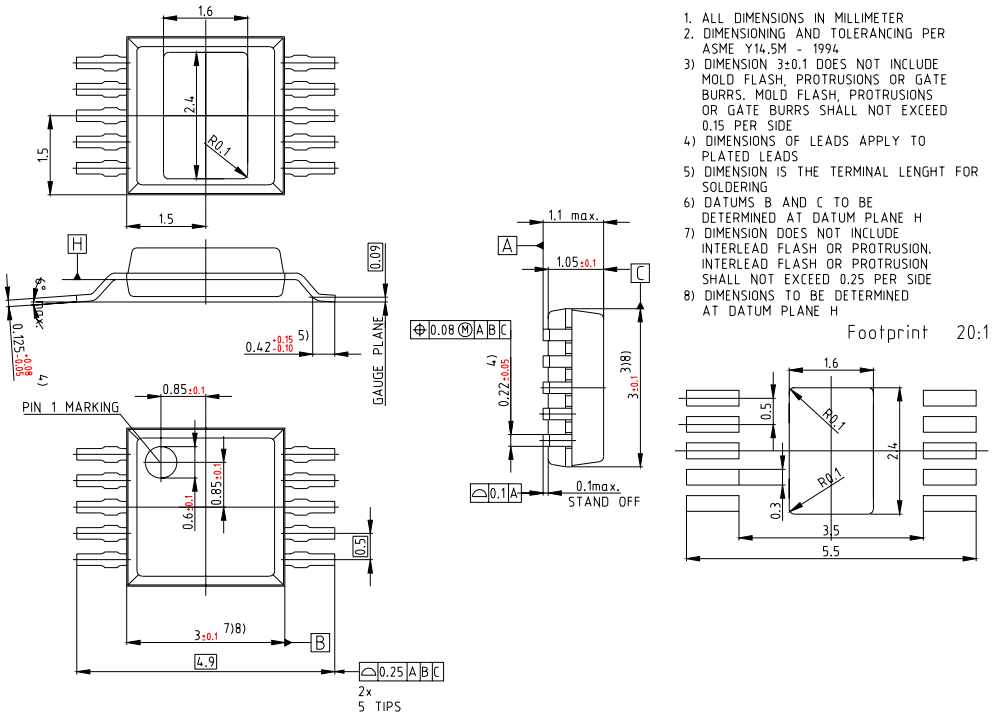
2.3 Application

- Dual band wireless frontends GSM900/1800
- Excellent combination with Infineon GSM single chip SMARTi PMB6250

2.4 Package Outlines

P-TSSOP-10 (with Heat Sink):



3 Functional Description

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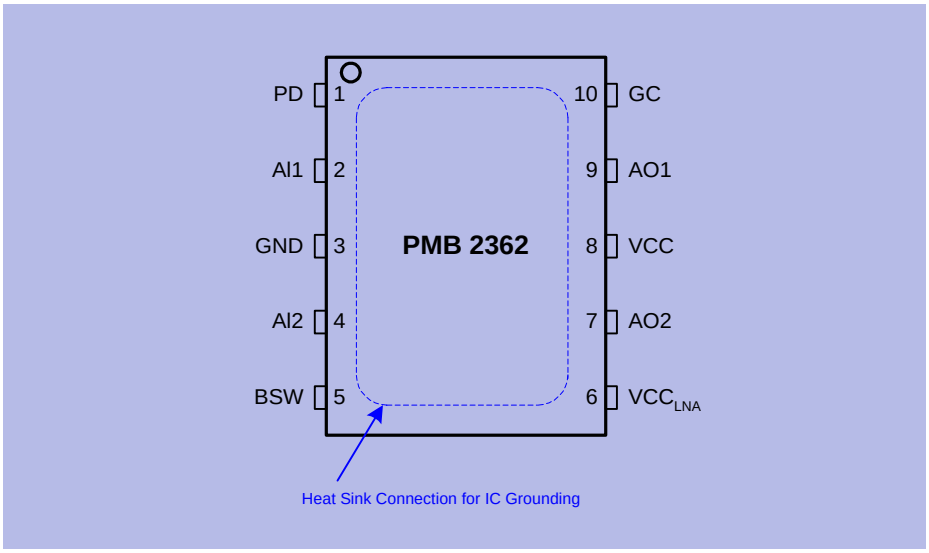
3.1 Pin Configuration



Pin_config.wmf

Figure 3-1 Pin Configuration

3.2 Pin Definition and Function

Table 3-1 Pin Definition and Function

Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	PD		Power down total circuit
2	AI1		LNA1 GSM900 signal base input
3	GND		Internal not connected, external GND connection recommended
4	AI2		LNA2 GSM1800 signal base input
5	BSW		Band switch, LNA1/LNA2
6	VCC_{LNA}		RF shunt open collector output LNA1/2
7	AO2		LNA2 amplifier output, open collector
8	VCC		Supply voltage total circuit
9	AO1		LNA1 amplifier output, matched
10	GC		LNA1/2 gain control
Heat Sink			Ground total circuit

3.3 Functional Block Diagram

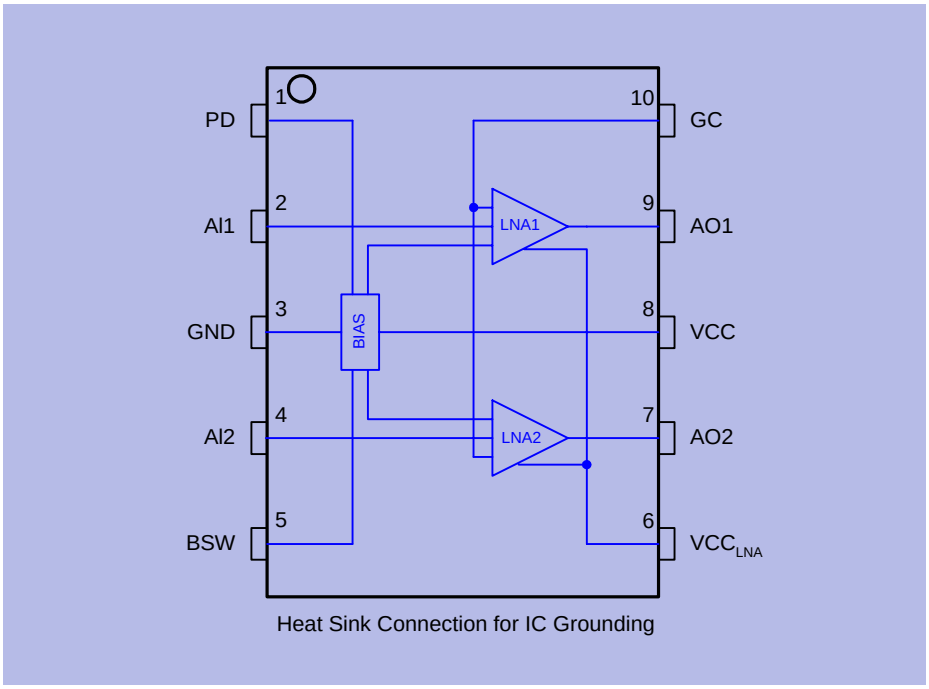


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Figure 3-2 Functional Block Diagram

3.4 Circuit Description

1. General Description

The PMB2362 is a dual band LNA circuit designed for dual band wireless front-tends with excellent performance.

2. LNA1

The LNA1 is designed for input frequencies between 0.9 and 1.0GHz. Entering the IC at the base input pin AI1 the RF input signal is amplified in the LNA1 stage. The gain of this LNA stage is controlled by the DC level at pin GC and can be adjusted in a 20 dB step. The LNA output is internal matched and at pin AO1 the amplified and matched signal is available for further use.

3. LNA2

The LNA2 is designed for input frequencies between 1.8 and 1.9GHz. Entering the IC at the base input pin AI2 the RF input signal is amplified in the LNA2 stage. The gain of this LNA stage is also controlled by the DC level at pin GC and can be adjusted in a fixed gain step. The open collector LNA output at pin AO2 has to be connected to VCC and external matching elements.

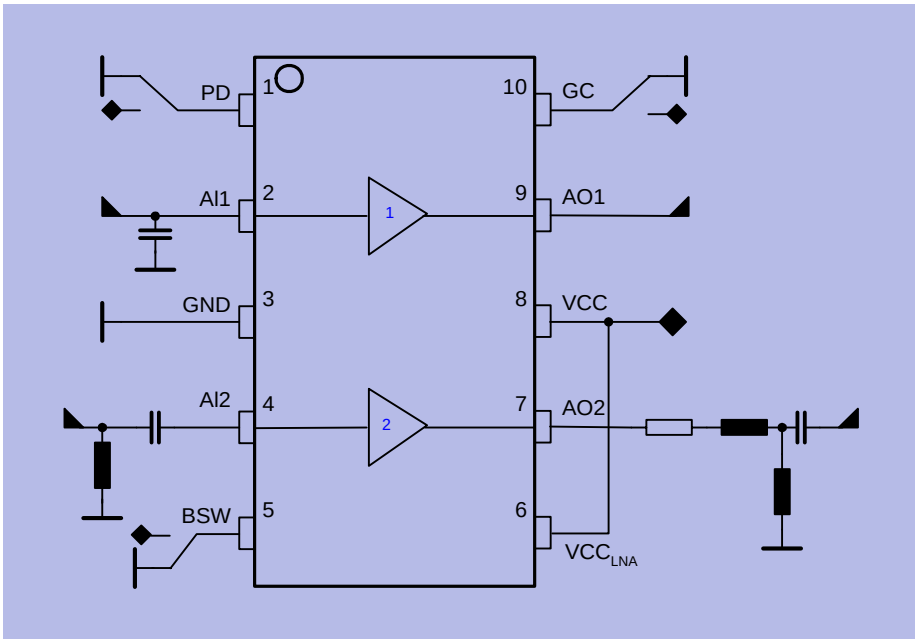
4. COMMON

VCC is the supply voltage for both LNAs. The grounding is done with the heat sink at the bottom side of the package. An internal bias driver generates supply voltage and temperature compensated reference voltages. The PD pin allows the circuit to be switched in a low power consuming (sleeping) mode. All pins with the exception of GND are ESD protected.

4 Applications

Contents of this Chapter

4.1 Circuits



Appl_circuit.wmf

Figure 4-1 Application Circuit

LNA 1:925 MHz - 960 MHz

LNA 2:1805 MHz - 1880 MHz

Refer to PMB2362 Application Note

5 Reference

Contents of this Chapter

5.1 Absolute Maximum Range

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Range, Ambient temperature T_{AMB}= -40°C ... + 85°C

Parameter	Symbol	Limit Values min	Limit Values max	Unit	Remarks
Supply Voltage	V_{VCC}	-0.3	5.0	V	
Input Voltage	V_{PD}	-0.3	V_S +0.3, 5.0max.	V	
Input Voltage	V_{BSW}	-0.3	V_S +0.3, 5.0max.	V	
Input Voltage	V_{GC}	-0.3	V_S +0.3, 5.0max.	V	V_{PD}>0.5V
Input Voltage	V_{GC}	-0.3	3.8	V	V_{PD}=0V
Input Voltage (AC Peak, Freq.>1MHz)	$V_{AI1/2}$	V_S -5.5, -2.0min.		V	V_{PD}=0V $I_{AI1/2}$<*nA*
Open Collector Output Voltage	$V_{AO2/VCCLNA}$	V_S -5.5, -0.3min	V_S +2.0, 5.0max.	V	
Input Current	$I_{AI1/2}$		6.0	mA	DC and AC
Junction Temperature	T_j		125	°C	
Storage Temperature	T_S	-40	125	°C	
Thermal Resistance	R_{thJA}		100	K/W	Junction to Ambient
Thermal Resistance	R_{thJL}		12	K/W	*Junction to Lead
ESD integrity	V_{ESD}	-1000	+1000	V	**

*

* Heat Sink Temperature Fixed At 25 ° Celsius

** According to MIL STD 883D, method 3015.7 and ESD Assn. Standard S5.1 - 1993.

5.2 Operating Ratings

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed.

Supply voltage V_S = 2.7V...3.6V, Ambient temperature T_{amb} = -40°C...85°C

Table 5-2 Operating Ratings

Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
		min	max				
AI1 Input Frequency LNA1	f_{AI1}	0.9	1.0	GHz			
AI2 Input Frequency LNA2	f_{AI2}	1.8	1.9	GHz			
Total Circuit On	V_{PD}	1.5	V_S	V			
Total Circuit Off	V_{PD}	0	0.5	V			
Gain Control Low Gain	V_{GC}	1.5	V_S	V			
Gain Control High Gain	V_{GC}	0	0.5	V			
Bandswitch LNA1 On	V_{BSW}	0	0.5	V			
Bandswitch LNA2 On	V_{BSW}	1.5	V_S	V			

■ This value is guaranteed by design

Power levels refer to 50 Ohms impedance

5.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply voltage V_{VCC} = 2.7V...3.6V, Ambient temperature T_{amb} = +25°C

Table 5-3 AC/DC Characteristics

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Supply Current								
Supply current, 0.95GHz	$I_{6,8,9}$	6.6	9.5	13	mA	V_{PD} high, V_{BSW} low		1.1
Supply current, 1.85GHz	$I_{6,7,8}$	5.5	8.5	11.5	mA	V_{PD} high,V_{BSW} high		1.2
Supply current, sleep	I_8		<5	<20	µA	V_{PD} low		1.3
LNA1, Signal Input AI1, high gain								
Input impedance vs. freq.	S_{11}		Table 1			Diagramm1	■	2.1**
Max. input level, 1db comp.	P_{AI1}	-20.5	-18.5		dBm	f=0.95GHz	■	2.2
Input intercept, third order	$IICP_{AI1}$	-12	-10		dBm	f=0.95GHz	■	2.3*
Noise figure	F_{AI1}		1.5	2.2	dB	f=0.95GHz	■	2.4*
LNA1, Signal Input AI1, low gain								
Input impedance vs. freq.	S_{11}		Table 1			Diagramm1	■	2.5
Max. input level, 1db comp.	P_{AI1}	-20.5	-18.5		dBm	f=0.95GHz	■	2.6
Input intercept, third order	$IICP_{AI1}$	-12	-10		dBm	f=0.95GHz	■	2.7*
Noise figure	F_{AI1}		8.0	10.0	dB	f=0.95GHz	■	2.8*
LNA1, Signal Output AO1, high gain								
Output impedance	VSWR		1.5			f=0.95GHz		2.9
Output impedance vs. freq.	S_{22}		Table 1			Diagramm1	■	2.10**
Power gain	S_{21}	16	17		dB	f=0.95GHz	■	2.11*
LNA1, Signal Output AO1, low gain								
Output impedance	VSWR		1.5			f=0.95GHz	■	2.12
Output impedance vs. freq.	S_{22}		Table 1			Diagramm1	■	13
Power Gain	S_{21}	-4	-3		dB	f=0.95GHz	■	2.14*

■ This value is guaranteed by design.

** S21 low/high gain; S11, S22 @f = 950 MHz measured in production

Table 5-3 AC/DC Characteristics (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
LNA2, Signal Input AI2, high gain								
Input impedance vs. freq.	S_{11}		Table 2			Diagramm2	■	3.1**
Max. input level, 1db comp.	P_{AI2}	-19	-17		dBm	f=1.85GHz	■	3.2
Input intercept, third order	$IICP_{AI2}$	-9.5	-7.5		dBm	f=1.85GHz	■	3.3*
Noise figure	F_{AI2}		2.0	2.7	dB	f=1.85GHz	■	3.4*
LNA2, Signal Input AI2, low gain								
Input impedance vs. freq.	S_{11}		Table 2			Diagramm	■	3.5
Max. input level, 1db comp.	P_{AI2}	-19	-17		dBm	f=1.85GHz	■	3.6
Input intercept, third order	$IICP_{AI2}$	-9.5	-7.5		dBm	f=1.85GHz	■	3.7*
Noise figure	F_{AI2}		11	13	dB	f=1.85GHz	■	3.8*
LNA2, Signal Output AO2, Open Collector, high gain								
Output impedance vs. freq.	S_{22}		Table 2			Diagramm	■	3.9**
Power gain	S_{21}	17	19		dB	f=1.85GHz	■	3.10*
LNA2, Signal Output AO2, Open Collector, low gain								
Output impedance vs. freq.	S_{22}		Table 2			Diagramm	■	3.11
Power gain	S_{21}	-3	-3		dB	f=1.85GHz	■	3.12*

■ This value is guaranteed by design.

* Measured with Application Circuit (Matched In- and Output)

** S21 low/high gain; S11, S22 @f=1.85GHz measured in production

Remark: IICP3 Measured with 800kHz differential tone

5.4 Diagrams

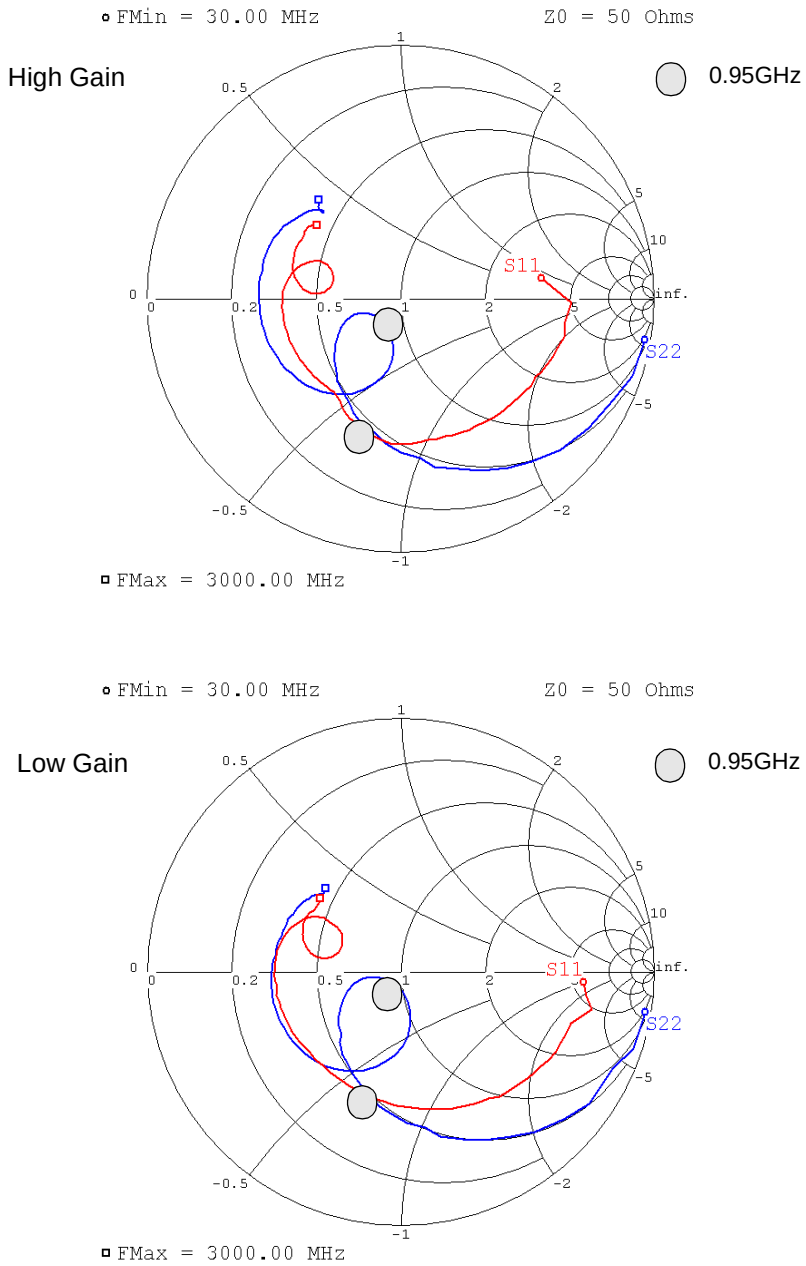


Figure 5-1 Diagramm1: S11 / S22 LNA1

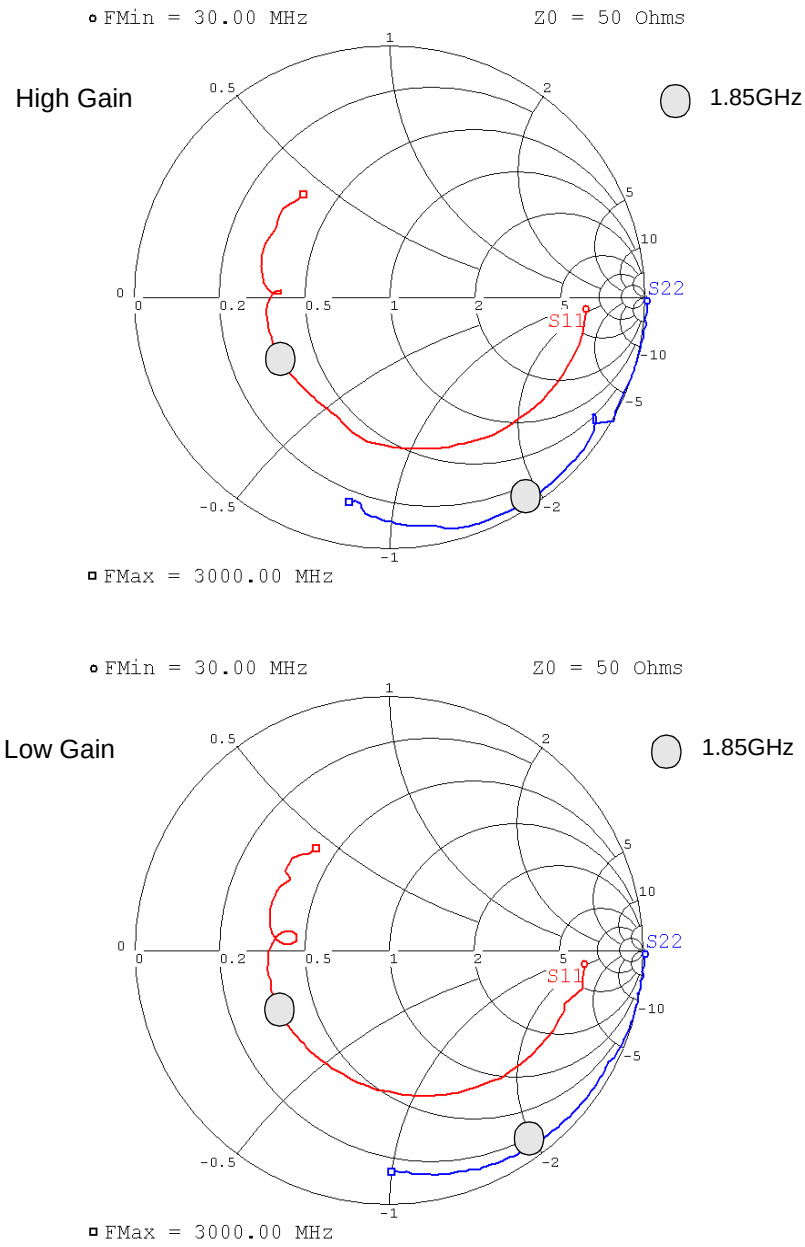
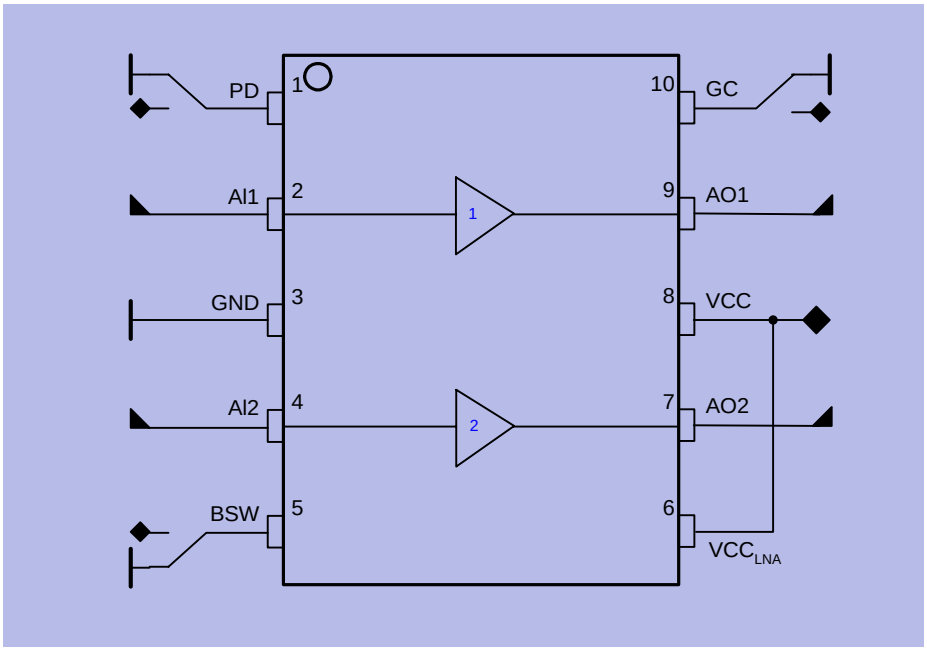


Figure 5-2 Diagramm2: S11 / S22 LNA2

5.5 Test Circuits

1. S-Parameter Test Circuit



Test_circuit_1_2.wmf

Figure 5-3 S-Parameter Test Circuit

Test Circuit 1: 925 MHz - 960 MHz

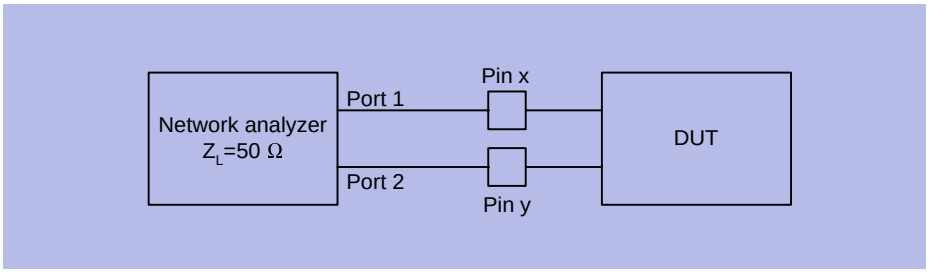
Test Circuit 2: 1805 MHz - 1880 MHz

Component values for blocking capacitors 10p @ VCC, 27p else

Blocking capacitors at Pin: 1, 5, 6, 8 and 10

DC Biasing LNA2 via Network Analyzer

2. S-Parameter Measurement Conditions



Test_circuit_3.wmf

Figure 5-4 S-Parameter Measurement of LNA1/2 : S11, S12, S21, S22

The S-Parameters are tested at the indicated frequency on Duroid 5880 Teflon Boards.

Via the NWA the capacitive coupling is done.

The output levels at port1 and 2 for pin x and y are -30dbm.

S11 and S22 have to be considered as design hints and are measured with Infineon testboards

All S-Parameters are measured

Table 5-4

Test	Test frequency [MHz]	Pin X	Pin Y
Amp. S11, S12, S21, S22	30 - 3000	AI 1/2	AO 1/2
Amp. S11, S12, S21, S22	900 - 1000	AI 1	AO 1
Amp. S11, S12, S21, S22	1800 - 1900	AI 2	AO 2

5.6 S-Parameters / Noise Parameters / Diagramms

1. Table 1: S-Parameter LNA1
   S-Parameters are available on 3.5” disk or by E-mail

High Gain

Frequency [GHz]	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
0.81	0.57468	-89.9	6.91583	131.3	0.003029	108.8	0.19661	-161
0.84	0.57036	-94.4	7.13553	126.7	0.003754	109.1	0.16465	-160.3
0.87	0.55963	-98.7	7.29022	121.9	0.005167	91.5	0.13922	-155.6
0.9	0.54796	-103.2	7.39837	116.7	0.006071	78.7	0.12151	-146.3
0.93	0.52863	-106.7	7.45604	112	0.006278	88.5	0.11372	-134.4
0.96	0.5219	-109.5	7.40121	107	0.007097	82.7	0.12553	-125.5
0.99	0.51085	-113.3	7.32031	102.8	0.007674	71.5	0.13011	-122.2
1.02	0.49465	-116.4	7.25988	98.8	0.007487	66.2	0.13604	-116.5
1.05	0.48186	-118.7	7.21209	95.2	0.007213	65	0.14442	-110.5
1.08	0.46918	-120.9	7.21321	91.4	0.007444	55.4	0.15835	-104.7
1.11	0.45961	-122.8	7.2465	87.4	0.007427	61.9	0.17981	-100.4

Low Gain

Frequency [GHz]	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
0.81	0.5257	-92	0.67474	133.8	0.00148	129.6	0.19295	-166.1
0.84	0.51998	-94.9	0.69912	130.1	0.00291	152.6	0.15726	-170.7
0.87	0.51502	-97.9	0.70104	124.8	0.002866	142.9	0.12124	-171.1
0.9	0.51035	-100.7	0.70771	121.5	0.00296	127.3	0.08884	-165.8
0.93	0.50507	-103.5	0.71506	117.2	0.003721	129.3	0.06165	-152.2
0.96	0.50343	-106.5	0.71056	113	0.004777	127	0.05343	-123.2
0.99	0.50052	-109.4	0.70932	109	0.005215	115.4	0.06368	-96.2
1.02	0.49629	-112.1	0.70358	104.8	0.005844	112.1	0.08836	-83
1.05	0.49323	-114.9	0.69611	100.9	0.005821	107.1	0.11838	-78
1.08	0.48924	-117.4	0.69115	96.8	0.006178	102.7	0.1497	-77.3
1.11	0.48684	-120	0.68395	92.7	0.006651	97.5	0.18416	-78.6

Noise Parameters @ 920MHz:

Fmin = 1.33dB	Rn = 6.17	Γopt: Mag: 0.132	Ang: 132.9

2. Table 2: S-Parameter LNA2
   S-Parameters are available on 3.5” disk or by E-mail

High Gain

Frequency [GHz]	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
1.71	0.49242	-152.6	6.88619	44	0.009319	106.7	0.97152	-52.6
1.74	0.49159	-154.5	6.78958	42.2	0.010126	112.5	0.97075	-53.6
1.77	0.49287	-156.5	6.67339	40.3	0.010619	107.5	0.96835	-54.9
1.8	0.49257	-158.1	6.54866	38.5	0.010952	103.6	0.96761	-55.9
1.83	0.49122	-160	6.44234	36.8	0.011616	109.8	0.97078	-57.1
1.86	0.4897	-161.9	6.35383	34.8	0.012092	100.5	0.97236	-58.1
1.89	0.49049	-163.8	6.22605	33	0.011617	104.6	0.97083	-59.5
1.92	0.49163	-165.6	6.11839	31.3	0.013675	102.4	0.96812	-60.6
1.95	0.48904	-167.1	6.01005	29.5	0.013032	101.7	0.96681	-61.6
1.98	0.48789	-169	5.90915	27.7	0.013869	99.9	0.96768	-62.7
2.01	0.48725	-171.3	5.81244	25.9	0.01401	99.3	0.96638	-63.9

Low Gain

Frequency [GHz]	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
1.71	0.49151	-156.7	0.61223	43.4	0.005883	137.2	0.95592	-49.2
1.74	0.49043	-158.9	0.59784	41.5	0.006472	130.3	0.95576	-50.2
1.77	0.49071	-161	0.58151	39.8	0.006974	127.6	0.95311	-51.3
1.8	0.48723	-162.9	0.56316	38.4	0.007237	127.7	0.95262	-52.2
1.83	0.4821	-164.6	0.5627	37.7	0.008687	123.6	0.95109	-53.2
1.86	0.48296	-166.4	0.5553	34.4	0.008648	126.1	0.94994	-54.2
1.89	0.48488	-168.5	0.53698	32.1	0.009628	121.2	0.94908	-55.2
1.92	0.48525	-170.6	0.52048	30.1	0.008635	119.8	0.94747	-56.1
1.95	0.48228	-172.4	0.50395	28	0.009701	116.5	0.94531	-57
1.98	0.47885	-174.6	0.48973	26.3	0.009804	117.5	0.94528	-57.9
2.01	0.47693	-177	0.47446	24.4	0.009466	111.3	0.94391	-58.8

Noise Parameters @ 1.82GHz:

Fmin = 1.86dB	Rn = 6.76	Γopt: Mag: 0.197	Ang: -164.4