

MC44802A

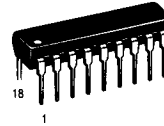
**PLL Tuning Circuit with 1.3 GHz
Prescaler**

The MC44802A is a tuning circuit for TV applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler (which can be bypassed by software control) and thus can handle frequencies up to 1.3 GHz.

The MC44802A is manufactured on a single silicon chip using Motorola's high density bipolar, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits) process.

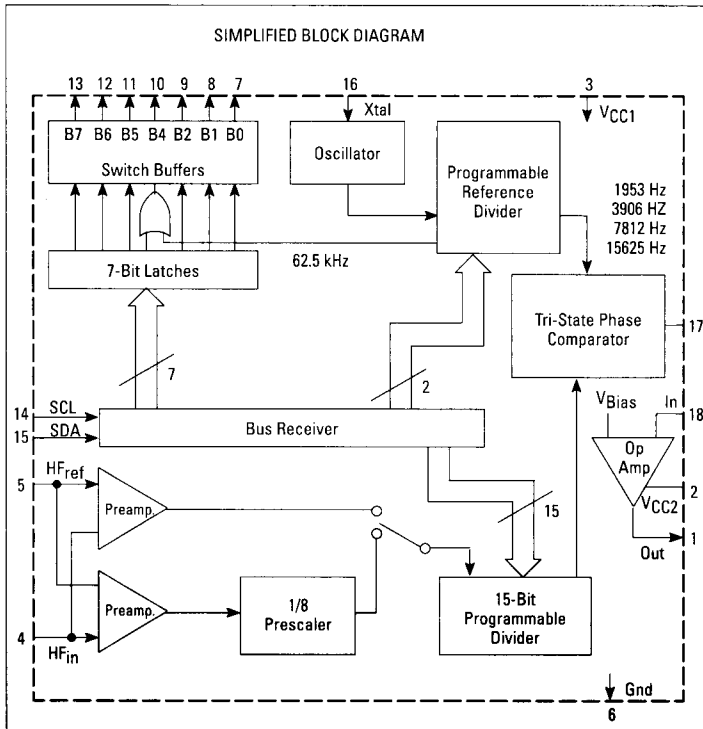
- Complete Single-Chip System for MPU Control (I²C Bus)
- Selectable Divide-by-8 Prescaler accepts Frequencies up to 1.3 GHz
- 15-Bit Programmable Divider accepts Input Frequencies up to 165 MHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output (33 V)
- Seven High Current Output Buffers (10 mA, 12 V)
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with MC44810

**PLL TUNING CIRCUIT
WITH 1.3 GHz PRESCALER**

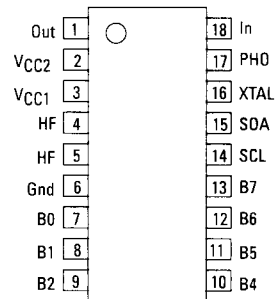


**P SUFFIX
PLASTIC PACKAGE
CASE 707**

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC44802AP	0° to +70°C	Plastic DIP

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MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Ratings	Pin	Value	Unit
Power Supply Voltage V_{CC1}	3	6.0	V
Band Buffer "OFF" Voltage	7 to 13	15	V
Band Buffer "ON" Current	7 to 13	15	mA
Op Amp Power Supply Voltage V_{CC2}	2	36	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1	Continuous	V
Storage Temperature		-65 to +150	$^\circ\text{C}$
Operating Temperature Range		0 to +70	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC1} = 5.0\text{ V}$, $V_{CC2} = 32\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristics	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	3	4.5	5.0	5.5	V
V_{CC1} Supply Current ($V_{CC1} = 5.0\text{ V}$) (Note 1)	3	—	45	65	mA
V_{CC2} Supply Voltage Range	2	25	30	35	V
V_{CC2} Supply Voltage Current (Output Open)	2	—	0.8	2.0	mA
Band Buffer Leakage Current when "OFF" at 12 V	7 to 13	—	0.01	1.0	μA
Band Buffer Saturation Voltage when "ON" at 10 mA	7 to 13	—	0.6	1.0	V
Data/Clock Current at 0 V	14, 15	-10	—	0	μA
Clock Current at 5.0 V	14	0	—	1.0	μA
Data Current at 5.0 V Acknowledge "OFF"	15	0	—	1.0	μA
Data Saturation Voltage at 15 mA Acknowledge "ON"	15	—	—	1.0	V
Data/Clock Input Voltage Low	14, 15	—	—	1.5	V
Data/Clock Input Voltage High	14, 15	3.0	—	—	V
Clock Frequency Range	14	0	—	100	kHz
Oscillator Frequency Range	—	3.5	4.0	4.1	MHz
Phase Detector Tri-State Current	17	-15	0	15	nA
Phase Detector High-State Source Current (@ 1.5 V)	17	-2.0	—	-0.5	mA
Phase Detector Low-State Sink Current (@ 3.5 V)	17	0.2	—	1.7	mA
Op Amp Internal Reference Voltage	—	2.1	2.75	3.0	V
Op Amp Input Current	18	-15	0	15	nA
DC Open Loop Gain	—	2000	5000	—	
Gain Bandwidth Product ($R_L = 10\text{ k}$, $C_L = 20\text{ pF}$)	—	0.3	—	—	MHz
Phase Margin ($R_L = 10\text{ k}$, $C_L = 20\text{ pF}$)	—	50	—	—	Deg.
V_{out} Low, Sinking 50 μA	1	—	0.1	0.3	V
V_{out} High, Sourcing 50 μA , $V_{out} - V_{CC2}$	1	-4.0	-3.0	—	V
V_{CC1} Supply Ripple Rejection (See Figure 1a)	—	—	-54	-45	dB

HF CHARACTERISTICS (See Figure 1b)

HF In/Ref DC Bias	4, 5	—	1.6	—	V
HF Voltage Range Prescaler "OFF" 10 to 150 MHz	5	20	—	315	mVrms
HF Voltage Range Prescaler "ON" 50 to 900 MHz	5	20	—	315	mVrms
HF Voltage Range Prescaler "ON" 900 to 1300 MHz	5	50	—	315	mVrms

NOTES:

1. When prescaler "OFF", typical supply current is decreased by 20 mA.

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FIGURE 1a — RIPPLE REJECTION — MEASUREMENT SCHEMATIC

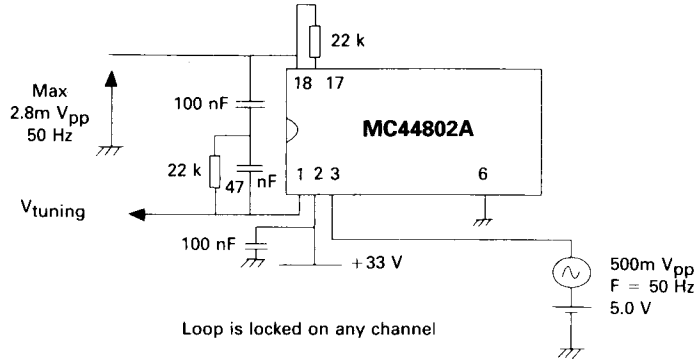


FIGURE 1b — HF SENSITIVITY TEST CIRCUIT

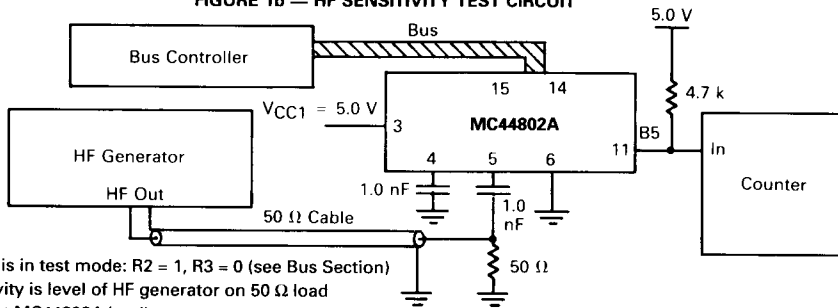
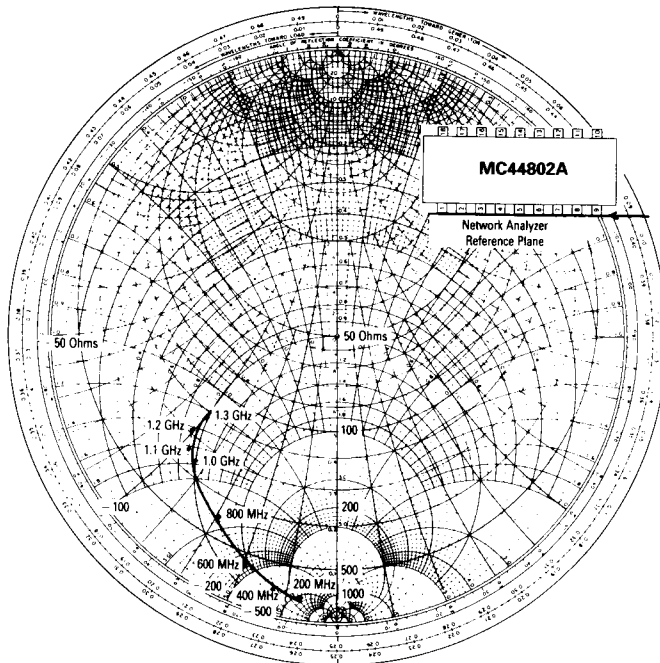


FIGURE 2 — PIN 5 INPUT IMPEDANCE (TYP)



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FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion

of the features and function of each of the internal blocks is given below.

FIGURE 4 — BLOCK DIAGRAM

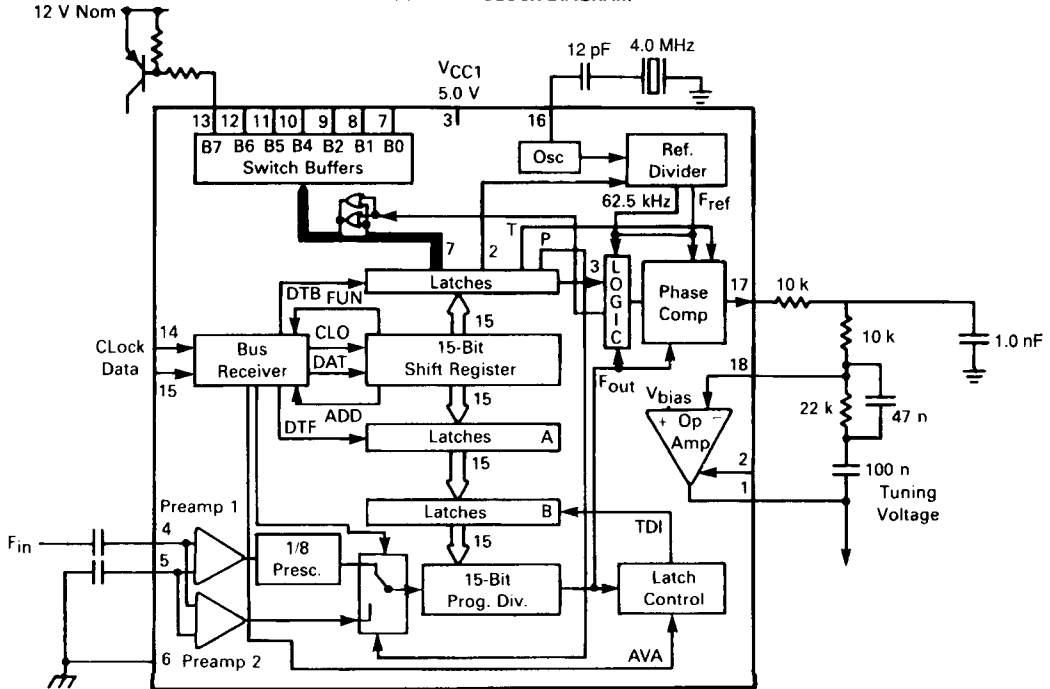
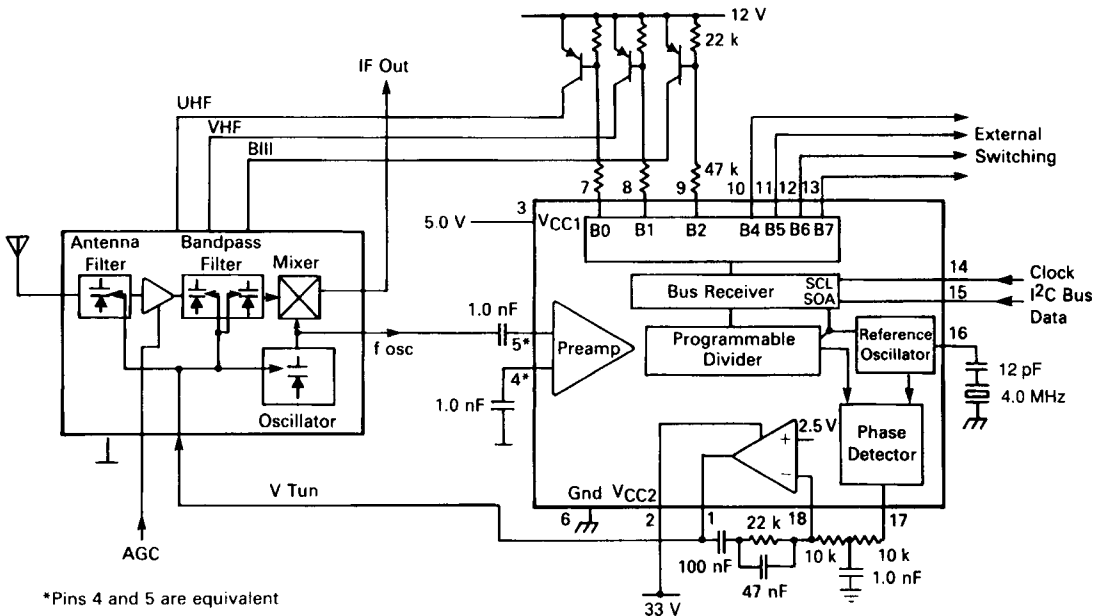


FIGURE 5 — TYPICAL TUNER APPLICATION



*Pins 4 and 5 are equivalent

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DATA FORMAT AND BUS RECEIVER

The circuit receives the information for tuning and control via the I²C Bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I²C Bus receiver. The definition of the permissible bus protocol is shown below:

```

1__STA  CA  CO  BA  STO
2__STA  CA  FM  FL  STO
3__STA  CA  CO  BA  FM   FL  STO
4__STA  CA  FM  FL  CO   BA  STO
    
```

STA = Start Condition
 STO = Stop Condition
 CA = Chip Address Byte
 CO = Data Byte for Control Information
 FM = Data Byte for Frequency Information (MSBs)
 FL = Data Byte for Frequency Information (LSBs)
 BA = Band Information

Frequency information is preceded by a Logic "0." If the function bit is Logic "1" the two following bytes contain control and band information where the bits have the following functions:

- Bit R0 and R1
Define the reference divider division ratio. Four ratios are available (see Table 1).
- Bit R2 and R3
Are used to switch internal signals to the buffer outputs. Pin 10 and 11 (see Table 2).
- Bit R2, R6 and T
Are used to control the phase comparator output stage (see Table 3).
- Bit P
Switches the prescaler in and out. At Logic "1" the prescaler is bypassed and the power supply of the prescaler is switched off.

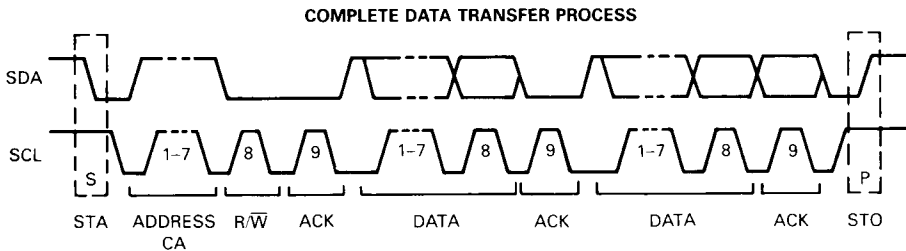


Figure 6 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ingored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allow the IC to distinguish between frequency information and control plus band information.

FIGURE 6 — DEFINITION OF BYTES

CA_Chip Address	1 1 0 0 0 0 1 0 ACK
CO_Information	① R6 T P R3 R2 R1 R0 ACK
BA_Band Info.	B7 B6 B5 B4 X B2 B1 B0 ACK
FM_Frequency Info.	① N14 N13 N12 N11 N10 N9 N8 ACK
FL_Frequency Info.	N7 N6 N5 N4 N3 N2 N1 B0 ACK

TABLE 1

Input Data		Reference Divider
R1	R0	Division Ratio
0	0	2048
0	1	1024
1	0	512
1	1	256

TABLE 2

Input Data		Test Outputs on Buffers	
R2	R3	Pin 10	Pin 11
0	0	—	—
0	1	62.5 kHz	—
1	0	F _{ref}	FBY2
1	1	—	—

Bit B4 has to be "zero" when Pin 10 is used to output 62.5 kHz.

Bit 4 and B5 have to "zero" to output F_{ref} and FBY2. FBY2 is the programmable divider output frequency divided by two.

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TABLE 3

Input Data			Output State of the Phase Comparator
R2	R6	T	
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off
1	1	0	Normal Operation
1	1	1	Off

THE BAND BUFFERS

BA_Band Information

20 Pin Version

B7	B6	B5	B4	B3	B2	B1	B0	ACK
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18 Pin Version

B7	B6	B5	B4	X	B2	B1	B0	ACK
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The band buffers are open collector transistors and are active "low" at $B_n = 1$. They are designed for 10 mA with a typical on-resistance of 70 ohms. These buffers are designed to withstand relative high output voltage in the off-state.

B4 and B5 buffers (Pins 10 and 11) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for tests purposes.

Buffer B4 may also be used to output a 62.5 kHz frequency for an intermediate stage of the reference divider. The bit B4 and/or B5 have to be zero if the buffers are used for these additional functions.

THE PROGRAMMABLE DIVIDER

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$$N = 16384 \times N14 + 8132 \times N13 + \dots + 4 \times N2 + 2 \times N1 + N0$$

Max Ratio 32767

Min Ratio 17

Where $N0, \dots, N14$ are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the IIC bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of $N = 256$ or higher.

THE PRESCALER

The prescaler has a preamplifier which guarantees high input sensitivity. The prescaler may be bypassed (Bit P) and the signal then passes through preamp 2.

THE PHASE COMPARATOR

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

THE OPERATIONAL AMPLIFIER

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 31 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 1 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.);

As a starting point for optimization, the components values in Figure 1 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

THE OSCILLATOR

The oscillator uses a 4.0 MHz crystal tied to ground or V_{CC1} through a capacitor, used in the series resonance mode. The frequency range of the oscillator is 3.5 to 4.1 MHz.

The voltage at Pin 16 (crystal) has low amplitude and low harmonic distortion.

SYSTEM APPLICATION

Table 4 is a summary of the circuit applications using a 4.0 MHz crystal.

TABLE 4

Input Data R1 R0		Reference Divider Div. Ratio	Reference Frequency Hz (1)	With Internal Prescaler P = 0		Without Internal Prescaler P = 1	
				Frequency Steps kHz	Max. Input Frequency MHz	Frequency Steps kHz	Max. Input Frequency MHz
0	0	2048	1953.125	15.625	512	1.953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300(2)	7.8125	165(3)
1	1	256	15625.0	125	1300(2)	15.625	165(3)

(1) With 4.0 MHz Crystal

(2) Limit of Prescaler

(3) Limit of Programmable Divider