

PRELIMINARY

Notice: These are not a final specification. Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M50933-XXXFP M50934-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50933-XXXFP and the M50934-XXXFP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 80-pin plastic molded QFP. These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

These microcomputers are also suitable for applications which require controlling LCDs.

The differences between M50933-XXXFP and the M50934-XXXFP are noted below.

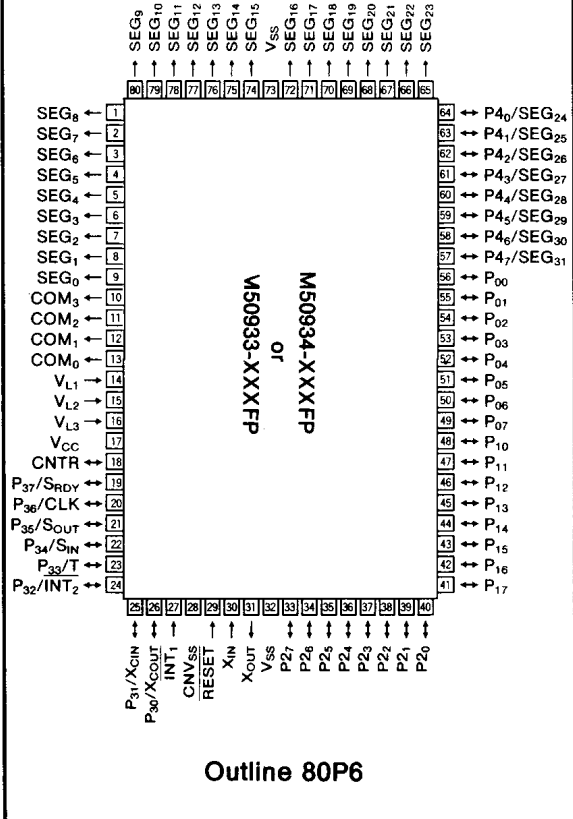
Type name	ROM size	RAM size
M50933-XXXFP	6144 bytes	192 bytes
M50934-XXXFP	8192 bytes	256 bytes

The differences between the M50933-XXXFP, M50934-XXXFP and the M50932-XXXFP are some electrical characteristics and the fact that these microcomputers work only in the single-chip mode. Other functions are explained in the M50932-XXXFP's section in detail.

FEATURES

- Number of basic instructions..... 69
- Instruction execution time
..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply
f(X_{IN})=4MHz 3.8~5.5V
f(X_{IN})=2MHz 2.7V ≤ V_{CC} ≤ 5.5V(Typ.)
- Power dissipation
normal operation mode (at 4MHz frequency)
..... 15mW(V_{CC}=5V, Typ.)
low-speed operation mode (at 32kHz frequency for clock function)
..... 225μW (V_{CC}=5V, Typ.)
stop mode(at 25°C) 5μW (V_{CC}=5V, Max.)
- RAM retention voltage (stop mode)
..... 2.0V ≤ V_{RAM} ≤ 5.5V
- Subroutine nesting 64 levels (Max.)
- Interrupt 8 types, 5 vectors
- 8-bit timer 3 (2 when used as serial I/O)
- 16-bit timer 1 (Two 8-bit timers make one set)
- Programmable I/O ports
(Ports P0, P1, P2, P3) 32
- Input port (Port P4) 8
- Serial I/O (8-bit) 1
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
segment output 32
common output 4
- Two clock generator circuits
(One is for main clock, the other is for clock function)

PIN CONFIGURATION (TOP VIEW)



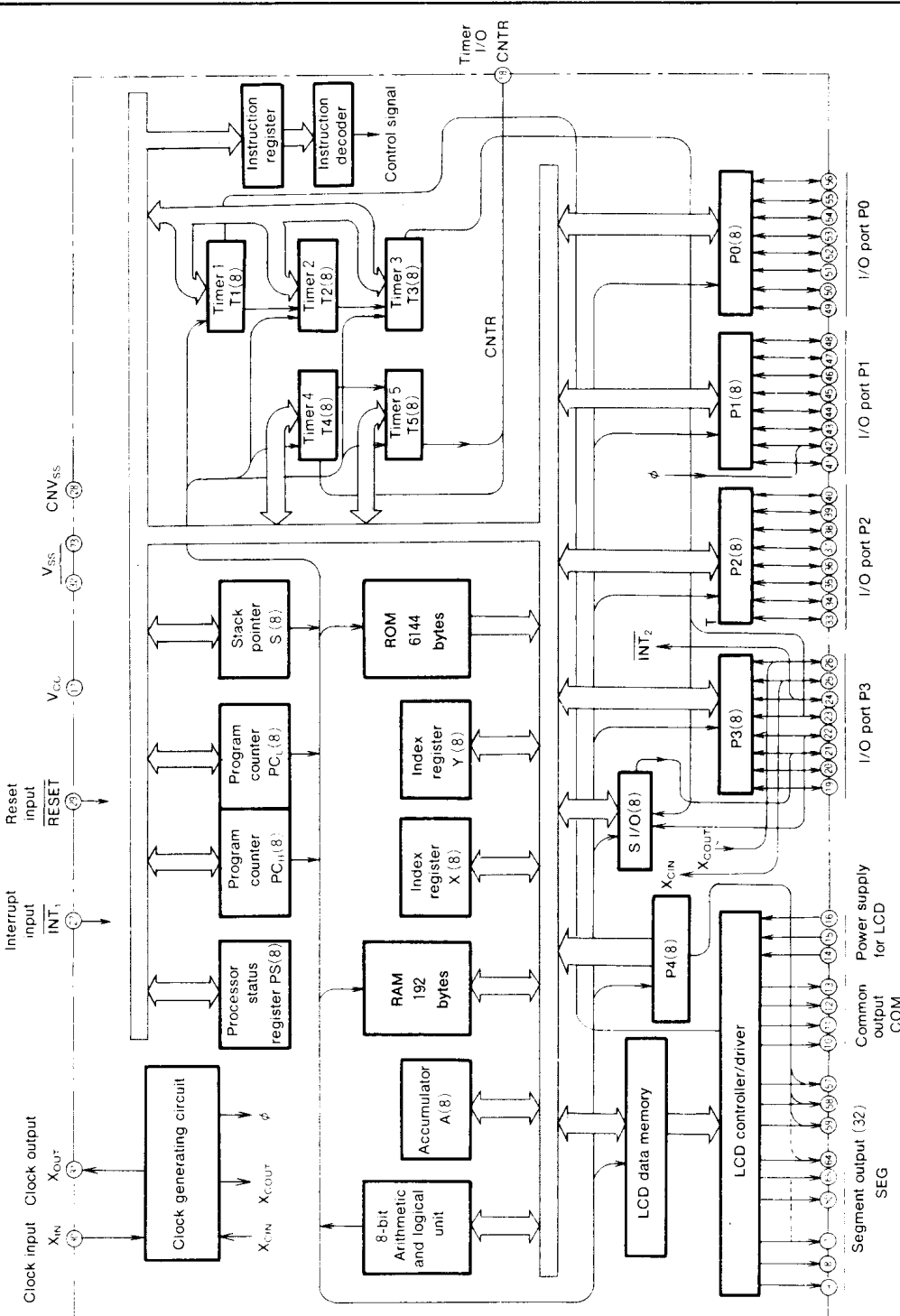
APPLICATION

- Office automation equipment
- VCR, Tuner, Audio-visual equipment
- Telephone

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M50933-XXXFP BLOCK DIAGRAM



Note
 1 : Program counter PC_{H} is only 6 bits long.
 2 : M50934 has 8192 bytes ROM.
 3 : M50934 has 256 bytes RAM.

FUNCTIONS OF M50933-XXXFP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency).
Clock frequency		4.3MHz
Memory size	ROM	6144 bytes (8192 bytes for M50934-XXXFP)
	RAM	192 bytes (256 bytes for M50934-XXXFP)
	RAM for display LCD	16 bytes
Input/Output ports	P0, P1, P2, P3	I/O 8-bitX4
	P4	Input 8-bitX1 (Port P4 are in common with SEG)
	SEG	LCD output 32-bitX1
	COM	LCD output 4-bitX1
Serial I/O		8-bitX1
Timers		8-bit timerX3 (2 when serial I/O is used) 16-bit timerX1 (combination of two 8-bit timers)
LCD controller/driver	Bias	1/2, 1/3 bias selectable
	Duty ratio	1/2, 1/3, 1/4 duty selectable
	Common output	4
	Segment output	32 (SEG ₂₄ ~SEG ₃₁ are in common with port P4)
Subroutine nesting		64 (max.)
Interrupt		Two external interrupts, Three timer interrupts (or two timer, one serial I/O)
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage		2.7~5.5V (RAM retention voltage at clock stop is 2~5.5V)
Power dissipation	At high-speed operation V _{CC} =5V	15mW (at clock frequency X _{IN} =4MHz, typ.)
	At low-speed operation V _{CC} =5V	225 μ W (at clock frequency X _{CIN} =32kHz, typ.)
	At STOP mode	5 μ W (at clock stop, max.)
Input/Output characteristics	Input/Output voltage	5V
	Output current	I _{OH} =-2mA (V _{OH} =3V) I _{OL} =10mA (V _{OL} =2V) Pull-up current : Min. -30 μ A, max. -140 μ A, typ -70 μ A (V _{CC} =5V input voltage 0V)
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate
Package		80-pin plastic molded QFP

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS} .
CNV _{SS}	CNV _{SS}		This is usually connect to V _{SS} .
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
$\overline{\text{INT}}_1$	Interrupt input	Input	This is the highest order interrupt input pin.
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{\text{SRDY}}$, CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{\text{INT}}_2$ pin, X _{CIN} and X _{COUT} pins, respectively.
P4 ₀ ~P4 ₇	Input port P4	I/O	Port P4 is an 8-bit input port and can be used as segment output pins.
V _{L1} ~V _{L3}	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as 0V≤V _{L1} ≤V _{L2} ≤V _{L3} ≤V _{CC} . 0V~V _{L3} is supplied to LCD.
COM ₀ ~ COM ₃	Common output	Output	These are LCD common output pins. At 1/2 duty, COM ₂ and COM ₃ pins are not used. At 1/3 duty, COM ₃ is not used.
SEG ₀ ~ SEG ₂₃	Segment output	Output	These are LCD segment output pins.
CNTR	Timer I/O	I/O	This is an output pin for the timer 4 and 5.

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BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50933-XXXFP is shown in Figure 1. Address 2800₁₆ to 3FFF₁₆ are assigned for the built-in ROM area which consists of 4096 bytes (Addresses 2000₁₆ to 3FFF₁₆ are assigned for the built-in ROM area which consists of 8192 bytes for M50934-XXXFP). Addresses 3F00₁₆ to 3FFF₁₆ are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses 3FF4₁₆ to 3FFF₁₆ are vector addresses used for the reset and interrupts (See interrupts chapter).

Addresses 0000₁₆ to 00FF₁₆ are the zero page address area. By using zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000₁₆ to 007F₁₆ and 0100₁₆ to 013F₁₆ are assigned for the built-in RAM which consists of 192 bytes (Addresses 0000₁₆ to 007F₁₆ and 0100₁₆ to 017F₁₆ are assigned for the built-in RAM which consists of 256 bytes for M50934-XXXFP). This RAM except the area in the page 1 is used as the stack during sub-routine calls and interrupts, in addition to data storage.

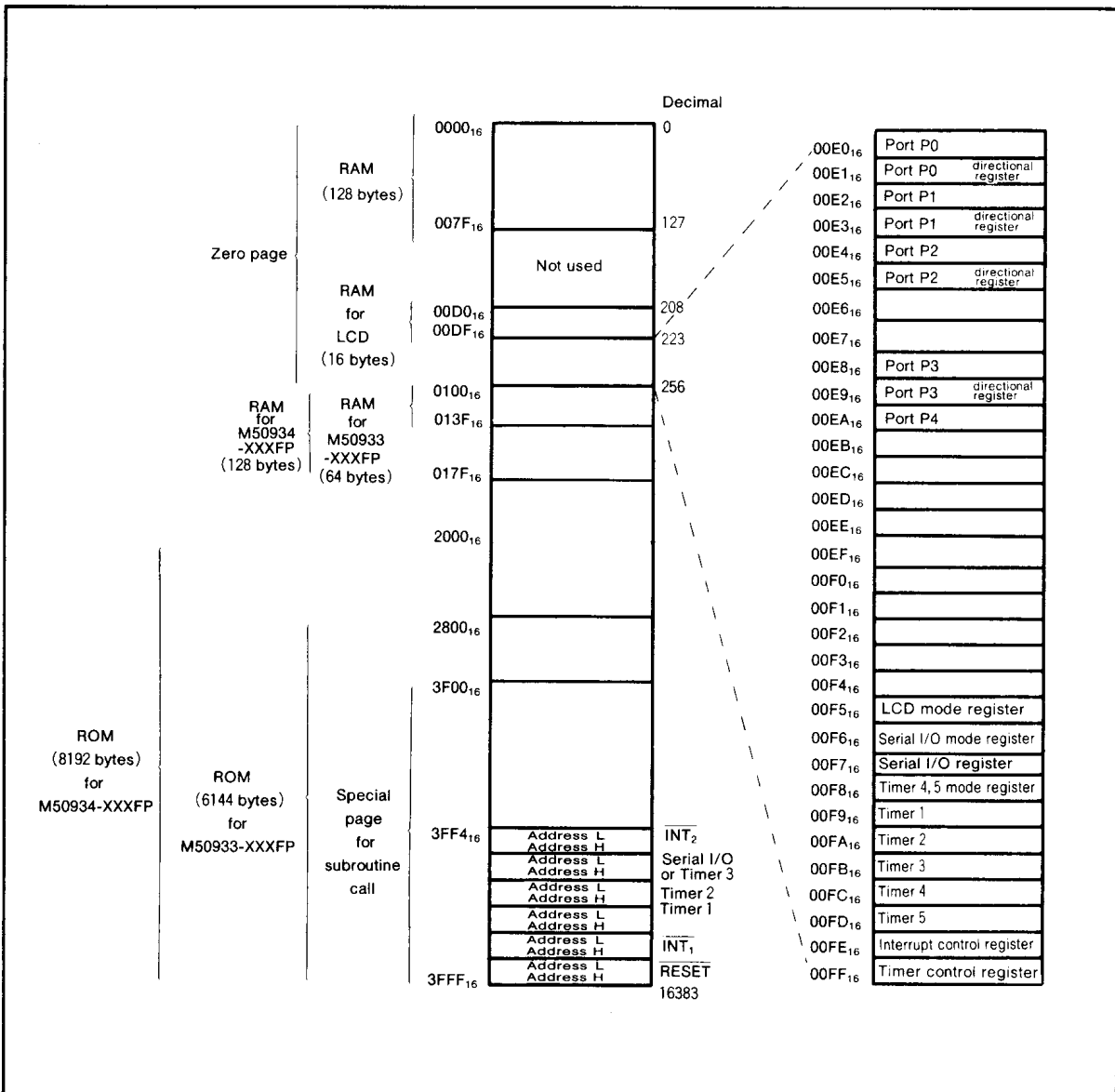


Fig.1 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**PROGRAMMING NOTES**

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address 00F8₁₆) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC,CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) When LCD turn-on bit (bit 3 of address 00F5₁₆) of the LCD mode register is "1", don't stop the timers or count source for timers.
- (7) The serial I/O counter must be initialized (write to 00F7₁₆) after switching the transfer clock source.
- (8) When using an external clock as the transfer clock source, the serial I/O counter must be initialized while the external clock is at "H" level.
- (9) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.
- (10) When using pins P3₀ and P3₁ as clock I/O pins, the pull-up option must not be used.
- (11) Notes on controlling the clock generation circuit
 - ① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set LM₇ to "1" after oscillation is stable by the software in side of clock X_C.
 - ② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set LM₇ to "0" after oscillation is stable by the software in side of clock X.
 - ③ When SM₅ is "0" or when LM₇ is "0" and SM₆ is "0", LM₆ is automatically set to "0" by the hardware.
 - ④ When system clock selection bit (bit 7 of address 00F5₁₆) of the LCD mode register is "1", don't set SM₅ to "0".
 - ⑤ In single-chip mode, the X_{OUT} pin uses as X_{OUT} output except setting value of LM₅.
 - ⑥ The other than single-chip mode and the input voltage for $\overline{\text{RESET}}$ pin is 10V, X_{OUT} pin uses as SYNC output except setting value of LM₅.

- (12) Bit 1 and 0 of the timer control register must be set to [00] because M50933 and M50934 work only in single-chip mode. Also, bit 5 of the LCD mode register must not to be set to "1".

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P3₅/S_{OUT} output format
- CNTR pin pull-up transistor

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~7	V
V _I	Supply voltage for LCD V _{L1} ~V _{L3}		-0.3~V _{CC} +0.3	V
V _I	Input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₇ , X _{IN}	Output transistor are "off"	-0.3~V _{CC} +0.3	V
V _I	Input voltage INT ₁ , CNV _{SS}		-0.3~7	V
V _I	Input voltage RESET, CNTR		-0.3~13	V
V _O	Output voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , COM ₀ ~COM ₃ , SEG ₀ ~SEG ₃₁ , X _{OUT}		-0.3~V _{CC} +0.3	V
V _O	Output voltage CNTR		-0.3~7	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage (Note 1)	f(X _{IN})=4.3MHz	3.8		5.5	V
		f(X _{IN})=2MHz	2.7		5.5	
V _{SS}	Supply voltage			0		V
V _{IH}	"H" input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₃ ₀ , P ₃ ₁ (Note 2), P ₃ ₃ ~P ₃ ₇ (Note 3), P ₄ ~P ₄₇ , RESET, X _{IN} , CNV _{SS}		0.7V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₂ ~P ₂₇ , P ₃ ₂ , P ₃ ₆ (Note 4) INT ₁ , CNTR		0.74V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₃ ₀ , P ₃ ₁ (Note 2), P ₃ ₃ ~P ₃ ₇ (Note 3), P ₄ ~P ₄₇ , CNV _{SS}		0		0.3V _{CC}	V
V _{IL}	"L" input voltage P ₂ ~P ₂₇ , P ₃ ₂ , P ₃ ₆ (Note 4) INT ₁ , CNTR		0		0.26V _{CC}	V
V _{IL}	"L" input voltage RESET		0		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN}		0		0.16V _{CC}	V
I _{OH}	"H" output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ₀ ~P ₃ ₇ (Note 5), X _{OUT}				-2	mA
I _{OL(peak)}	"L" peak output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ₀ ~P ₃ ₇ , CNTR, X _{OUT} (Note 6)				10	mA
I _{OL(avg)}	"L" average output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ₀ ~P ₃ ₇ , CNTR, X _{OUT} (Note 7)				5	mA
f(X _{IN})	Clock oscillating frequency (Note 8)	V _{CC} =3.8~5.5V	64		4300	kHz
		V _{CC} =2.7~5.5V	64		2000	
f(X _{CIN})	Clock oscillating frequency for clock function (Note 8)		32		50	kHz

- Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V.
 2 : When using port P₃, as X_{CIN}, 0.85V_{CC} ≤ V_{IH} ≤ V_{CC}, 0 ≤ V_{IL} ≤ 0.15V_{CC} for port P₃.
 3 : In this case of using port P₃₆ as normal input.
 4 : In this case of using port P₃₆ as CLK input.
 Especially when the input oscillation frequency is more than 50kHz, recommend the following :
 0.8V_{CC} ≤ V_{IH} ≤ V_{CC}, 0 ≤ V_{IL} ≤ 0.2V_{CC}
 5 : The total of I_{OH} of port P₀, P₁, P₂, P₃ and X_{OUT} should be 35mA max.
 6 : The total of I_{OL} (peak) of port P₀, P₁, P₂, P₃ should be 55mA max, and the total of I_{OL} (peak) of port P₃, CNTR, and X_{OUT} should be 45mA max.
 7 : I_{OL} (avg) is the average current in 100ms.
 8 : When changing the contents of the most significant bit at address 00F5₁₆, f(X_{IN}) needs the following range : f(X_{IN}) > 3f(X_{CIN}).

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ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min.	Typ.	Max.			
V_{OH}	"H" output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7$ (Note 9) (Note10)	$V_{CC}=5V, I_{OH}=-2mA$	3			V		
		$V_{CC}=3V, I_{OH}=-0.7mA$	2					
V_{OH}	"H" output voltage X_{OUT}	$V_{CC}=5V, I_{OH}=-1.5mA$ $V_{CC}=3V, I_{OH}=-0.3mA$	3 2			V		
V_{OL}	"L" output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7$ (Note10), CNTR	$V_{CC}=5V, I_{OL}=10mA$			2	V		
		$V_{CC}=3V, I_{OL}=0.3mA$			1			
V_{OL}	"L" output voltage X_{OUT}	$V_{CC}=5V, I_{OL}=1.5mA$			2	V		
		$V_{CC}=3V, I_{OL}=0.3mA$			1			
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT}_1, \overline{CNTR}$	$V_{CC}=5V$	0.25		1	V		
		$V_{CC}=3V$	0.15		0.7			
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input $V_{CC}=5V$ $V_{CC}=3V$			0.5 0.4	V		
		When used as X_{CIN} input $V_{CC}=5V$ $V_{CC}=3V$			0.7 0.5			
$V_{T+}-V_{T-}$	Hysteresis $P3_1$	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.4			
$V_{T+}-V_{T-}$	Hysteresis $P2_0\sim P2_7, P3_2$	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.4			
$V_{T+}-V_{T-}$	Hysteresis \overline{RESET}	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.35			
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.35			
I_{IL}	"L" input current $P4_0\sim P4_7$ (except reset state) $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, \overline{CNTR}$ without pull-up Tr. $\overline{INT}_1, \overline{RESET}, X_{IN}$	$V_{CC}=5V, V_i=0V$			-5	μA		
		$V_{CC}=3V, V_i=0V$			-4			
		$V_{CC}=5V, V_i=0V$ $V_{CC}=3V, V_i=0V$	-30 -6	-70 -25	-140 -45			
I_{IL}	"L" input current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, \overline{CNTR}$ with pull-up Tr.	$V_{CC}=5V, V_i=0V$	-30	-70	-140	μA		
		$V_{CC}=3V, V_i=0V$	-6	-25	-45			
I_{IL}	"L" input current $P4_0\sim P4_7$ (at reset state)	$V_{CC}=5V, V_{L3}=5V, V_i=0V$	-30		-140	μA		
		$V_{CC}=3V, V_{L3}=3V, V_i=0V$	-6		-45			
I_{IH}	"H" input current $P4_0\sim P4_7$ (except reset state) $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, \overline{CNTR}, \overline{INT}_1, \overline{RESET}, X_{IN}$	$V_{CC}=5V, V_i=5V$			5	μA		
		$V_{CC}=3V, V_i=3V$			4			
		$V_{CC}=5V, V_{L3}=5V, V_i=5V$ $V_{CC}=3V, V_{L3}=3V, V_i=3V$			5 4			
R_{COM}	Output impedance $COM_0\sim COM_3$	$V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC}$ Other COM, SEG pins are open.	$V_{CC}=5V$ $V_{CC}=3V$	30 70	200 500	2000 4000	Ω	
		$V_{CC}=5V$ $V_{CC}=3V$			2 3	k Ω		
R_s	Output impedance $SEG_0\sim SEG_3$	$V_{CC}=5V$ $V_{CC}=3V$			3 0.4	6 0.8	mA	
I_{CC}	Supply current (at operation)	Output pin are opened. $\overline{RESET}, P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7$ are connected to V_{CC} . Except the above pins are connected to V_{SS} . However, X_{IN} and X_{CIN} are input signal according to the conditions.	$T_a=25^\circ C, X_{IN}=0V, f(X_{CIN})=32.8kHz$ at low power mode ($LM_6=1$) $V_{CC}=5V$ $V_{CC}=3V$			45 18	85 26	μA
I_{CC}	Supply current (at wait state)	Output pin are opened. $\overline{RESET}, P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7$ are connected to V_{CC} . Except the above pins are connected to V_{SS} . However, X_{IN} and X_{CIN} are input signal according to the conditions.	$T_a=25^\circ C, X_{IN}=0V, f(X_{CIN})=32.8kHz$ at low power mode ($LM_6=1$) $V_{CC}=5V$ $V_{CC}=3V$			1 0.2	2 0.6	mA
I_{CC}	Supply current	Output pin are opened. $\overline{RESET}, P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7$ are connected to V_{CC} . Except the above pins are connected to V_{SS} . However, X_{IN} and X_{CIN} are input signal according to the conditions.	$f(X_{IN})=0, f(X_{CIN})=0, V_{CC}=5V$ $T_a=25^\circ C$ $T_a=70^\circ C$			0.1 1	10	μA
V_{RAM}	RAM retention voltage	$f(X_{IN})=0, f(X_{CIN})=0$		2		5.5	V	

Note 9 : Except when the output type of $P3_5$ is N-channel open drain (mask option).

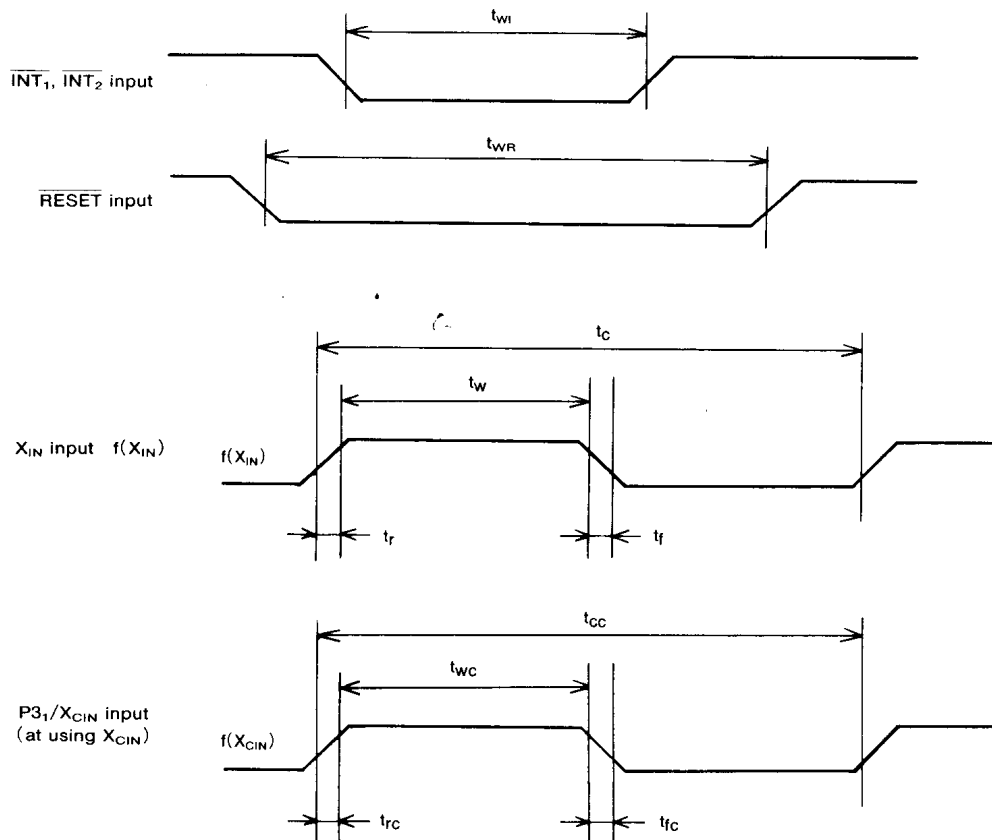
10 : If $P3_0$ is used as X_{COUT} , capability of load driving is lower than the above.

TIMING REQUIREMENTS

Memory expanding mode and microprocessor mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WI}	$\overline{INT}_1, \overline{INT}_2$ external clock input pulse width	$V_{CC}=2.7V$	1			μS
			4			
t_{WR}	RESET external clock input pulse width (Note 13)	$V_{CC}=2.7V$	2			μS
			8			
t_C	External clock input cycle time (X_{IN} pin)		250			ns
t_W	External clock input pulse width (X_{IN} pin)		75			ns
t_r	External clock rising edge time (X_{IN} pin)				25	ns
t_f	External clock falling edge time (X_{IN} pin)				25	ns
t_{CC}	External clock input cycle time ($P3_1/X_{CIN}$ pin, X_{CIN})		20			μS
t_{WC}	External clock input pulse width ($P3_1/X_{CIN}$ pin, X_{CIN})		5			μS
t_{rC}	External clock rising edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μS
t_{fC}	External clock falling edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μS

Note 13 : Hold RESET to "L" level while eight or more rise pulses are input from X_{IN} .



MITSUBISHI MICROCOMPUTERS

M37412M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37412M4-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic molded QFP.

This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

FEATURES

- Number of basic instructions..... 69
- Memory size ROM 8192 bytes
RAM 160 bytes
- Instruction execution time
..... 2 μ s (minimum instruction, at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting 80 levels (Max.)
- Interrupt..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P7)
..... 46
- Input port (Port P5) 8
- Output port (Port P6) 5
- Serial I/O (8-bit) 1
- 8-bit A-D converter 1
- 5-bit D-A converter 1
- 8-bit PWM function..... 1
- Watchdog timer 1

APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)

