LH5P1632

CMOS 512K (32K × 16) Pseudo-Static RAM

FEATURES

- 32,768 × 16 bit organization
- Access time: 80/150 ns (MAX.)
- Cycle time: 140/210 ns (MIN.)
- Single +5 V power supply
- Power consumption (MAX.):
  Operating: 467.5/327.5 mW
  Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycles/4 ms (MAX.)
- Available for auto-refresh mode
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP

DESCRIPTION

The LH5P1632 is a 512K-bit Pseudo-Static RAM organized as 32,768 × 16 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

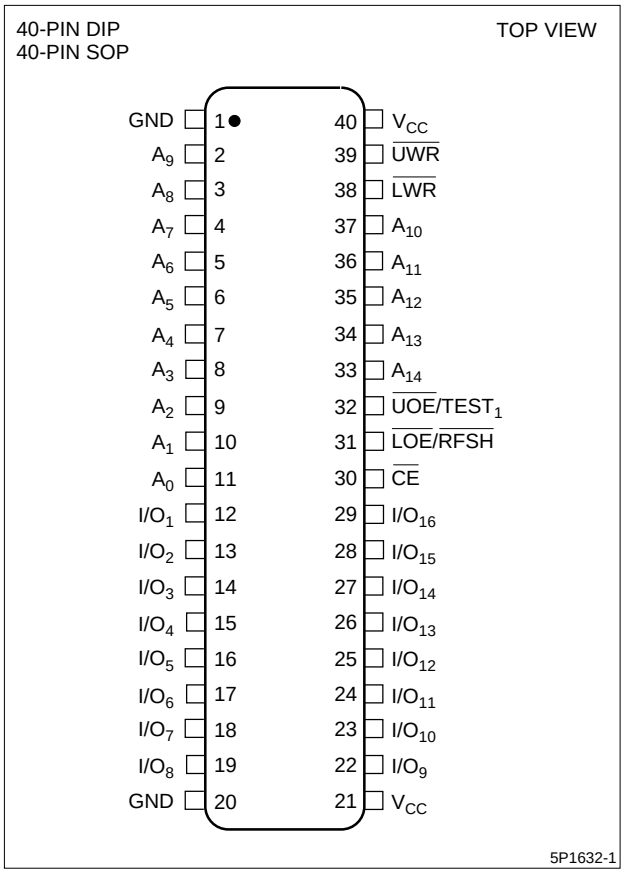


Figure 1. Pin Connections for DIP and SOP Packages

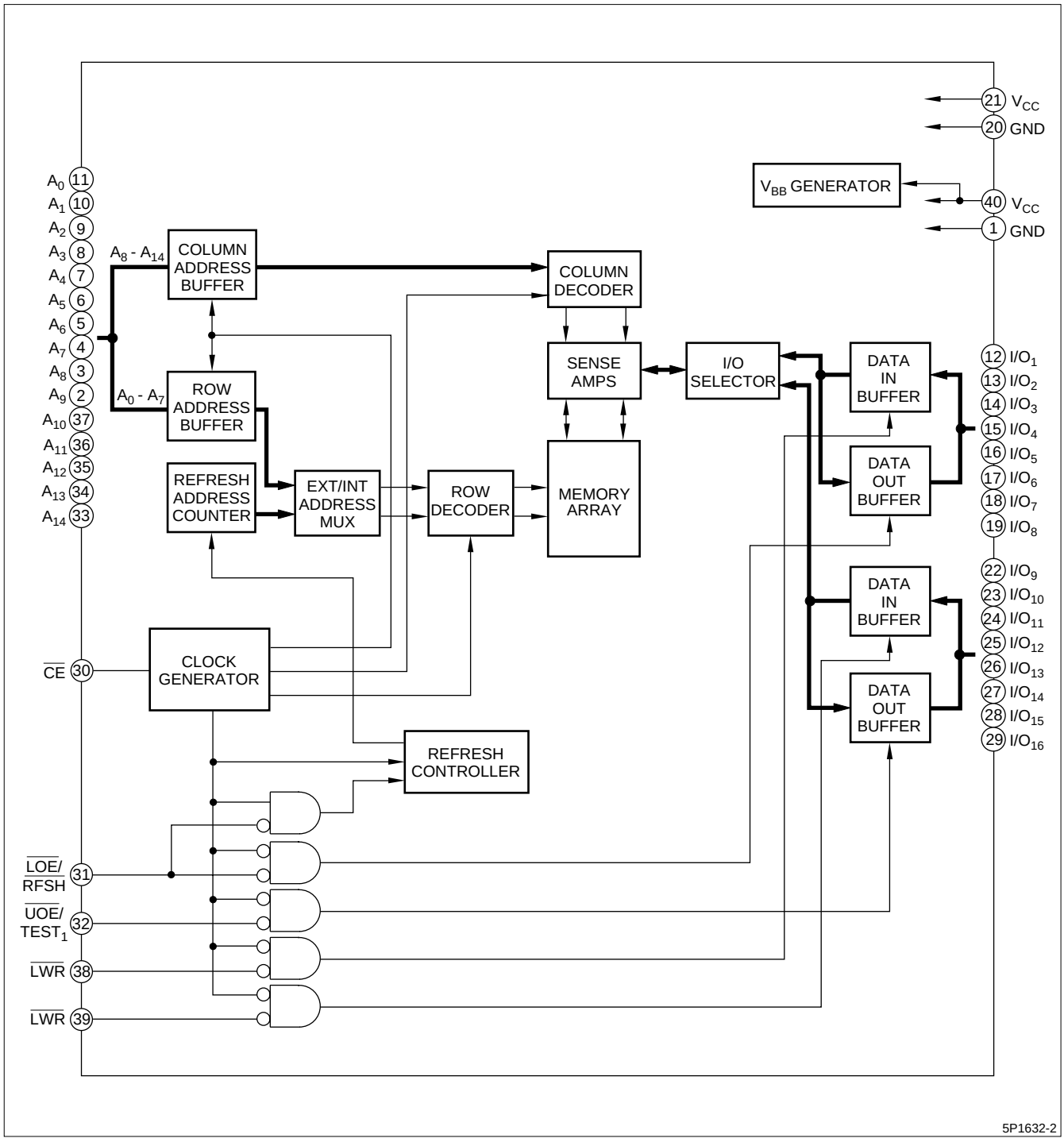


Figure 2. LH5P1632 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
$A_0 – A_{14}$	Address input
$\overline{LWR}$, $\overline{UWR}$	Write enable
$\overline{LOE}$/$\overline{RFSH}$, $\overline{UOE}$	Output enable/Refresh input
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
$I/O_1 – I/O_{16}$	Data input/output
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on all pins	V_T	–1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V	
	V_{IL}	–0.3		0.8	V	1

NOTE:
1. V_{IL} (MIN.) = –1.0 V when the pulse width is less than 20 ns.

CAPACITANCE (T_A = 0 to +70°C, f = 1 MHz, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 – A_{14}	C_{IN1}		8	pF
	$\overline{LWR}$, $\overline{UWR}$	C_{IN2}		5	pF
	$\overline{CE}$	C_{IN3}		5	pF
	$\overline{LOE}$/RFSH, $\overline{UOE}$	C_{IN4}		5	pF
Input/Output capacitance	I/O_1 – I/O_{16}	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation t_{RC} = t_{RC} (MIN)	I_{CC1}	LH5P1632-80		85	mA	1, 2
		LH5P1632-15		65		
Supply current in standby mode	I_{CC2}			3.0	mA	1, 3
Average supply current in CPU internal cycle ($\overline{LWR}$ = $\overline{UWR}$ = $\overline{LOE}$/RFSH = $\overline{UOE}$ = V_{IH})	I_{CC3}	LH5P1632-80		85	mA	1, 2
		LH5P1632-15				
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V, 0 V except on test pins	–10	10	µA	
I/O leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V, Outputs in high-impedance state	–10	10	µA	
Output HIGH voltage	V_{OH}	I_{OUT} = –1.0 mA	2.4		V	
Output LOW voltage	V_{OL}	I_{OUT} = 4.0 mA		0.4	V	

NOTES:
1. Specified values are with outputs open.
2. I_{CC1} and I_{CC3} depend on the cycle time.
3. $\overline{CE}$ = High, $\overline{LOE}$/RFSH = High.

AC CHARACTERISTICS [1, 2, 3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	–80 ns		–150 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
READ OR WRITE CYCLE							
Random read, write cycle time	t_{RC}	140		210		ns	
Read modify write cycle time	t_{RMW}	205		280		ns	
$\overline{CE}$ pulse width	t_{CE}	80	10,000	150	10,000	ns	
$\overline{CE}$ precharge time	t_P	50		60		ns	
Address setup time	t_{AS}	0		0		ns	4
Address hold time	t_{AH}	20		30		ns	4
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
$\overline{CE}$ access time	t_{CEA}		80		150	ns	5
$\overline{OE}$ access time	t_{OEA}		30		70	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	10		10		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		ns	
$\overline{OE}$ setup time for $\overline{WR}$	t_{OSW}	0		0		ns	
Output disable time from $\overline{CE}$	t_{CHZ}	0	25	0	35	ns	
Output disable time from $\overline{OE}$	t_{OHZ}	0	25	0	35	ns	
Output disable time from $\overline{WR}$	t_{WHZ}	0	25	0	35	ns	
$\overline{OE}$ setup time	t_{OES}	10		10		ns	
$\overline{OE}$ hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ lead time	t_{OEL}	10		10		ns	
Write command pulse width	t_{WCP}	60		85		ns	
Write command setup time	t_{WCS}	60		85		ns	
Write command hold time	t_{WCH}	60		85		ns	
Data setup time from $\overline{WR}$	t_{DSW}	30		50		ns	
Data setup time from $\overline{CE}$	t_{DSC}	30		50		ns	
Data hold time from $\overline{WR}$	t_{DHW}	0		0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		0		ns	
Transition time (rise and fall)	t_T	3	35	3	35	ns	
Refresh time interval	t_{REF}		4		4	ms	
REFRESH CYCLE							
Auto refresh cycle time	t_{FC}	140		190		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	50		60		ns	
Refresh pulse width (Auto Refresh)	t_{FAP}	30	8,000	80	8,000	ns	
Refresh precharge time (Auto Refresh)	t_{FP}	40		30		ns	
$\overline{CE}$ delay time from Refresh active (Auto Refresh)	t_{FCE}	160		225		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}$ and $\overline{OEL}$/$\overline{RFSH}$ should be kept V_{IH} for 200 µs after power on and followed by at least 8 dummy cycles.
2. AC characteristics shall be tested with t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE}$.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data for the lower byte (I/O_1 to I/O_8) is latched at the positive edge of LWR or the positive edge of $\overline{CE}$. Data for the upper byte (I/O_9 to I/O_{16}) is latched at the positive edge of UWR or the positive edge of $\overline{CE}$.

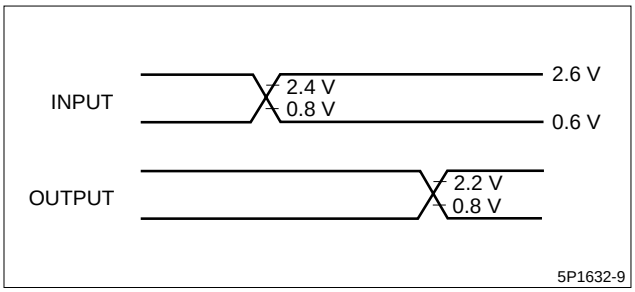


Figure 3. AC Characteristics

TRUTH TABLE

INPUT					OUTPUT		MODE		NOTE
$\overline{CE}$	$\overline{UOE}$	$\overline{LOE}/\overline{RFSH}$	$\overline{UWR}$	$\overline{LWR}$	$I/O_9 - I/O_{16}$	$I/O_1 - I/O_8$	UPPER BYTE	LOWER BYTE	
H	D	D	D	D	High-Z	High-Z	Standby		
L	L	L	H	H	D_{OUT}	D_{OUT}	Read	Read	
L	H	L	H	H	High-Z	D_{OUT}	$\overline{CE}$ only refresh	Read	
L	L	H	H	H	D_{OUT}	High-Z	Read	$\overline{CE}$ only refresh	
L	H	H	H	H	High-Z	High-Z	$\overline{CE}$ only refresh	$\overline{CE}$ only refresh	
L	D	D	L	L	D_{IN}	D_{IN}	Write	Write	
L	D	H	L	H	D_{IN}	High-Z	Write	$\overline{CE}$ only refresh	
L	H	D	H	L	High-Z	D_{IN}	$\overline{CE}$ only refresh	Write	
L	D	L	L	H	D_{IN}	D_{OUT}	Write	Read	Inhibit
L	L	D	H	L	D_{OUT}	D_{IN}	Read	Write	Inhibit
H	D	⊓_⊓	D	D	High-Z	High-Z	Auto Refresh		

NOTES:
D = Don't care.
High-Z = High impedance.

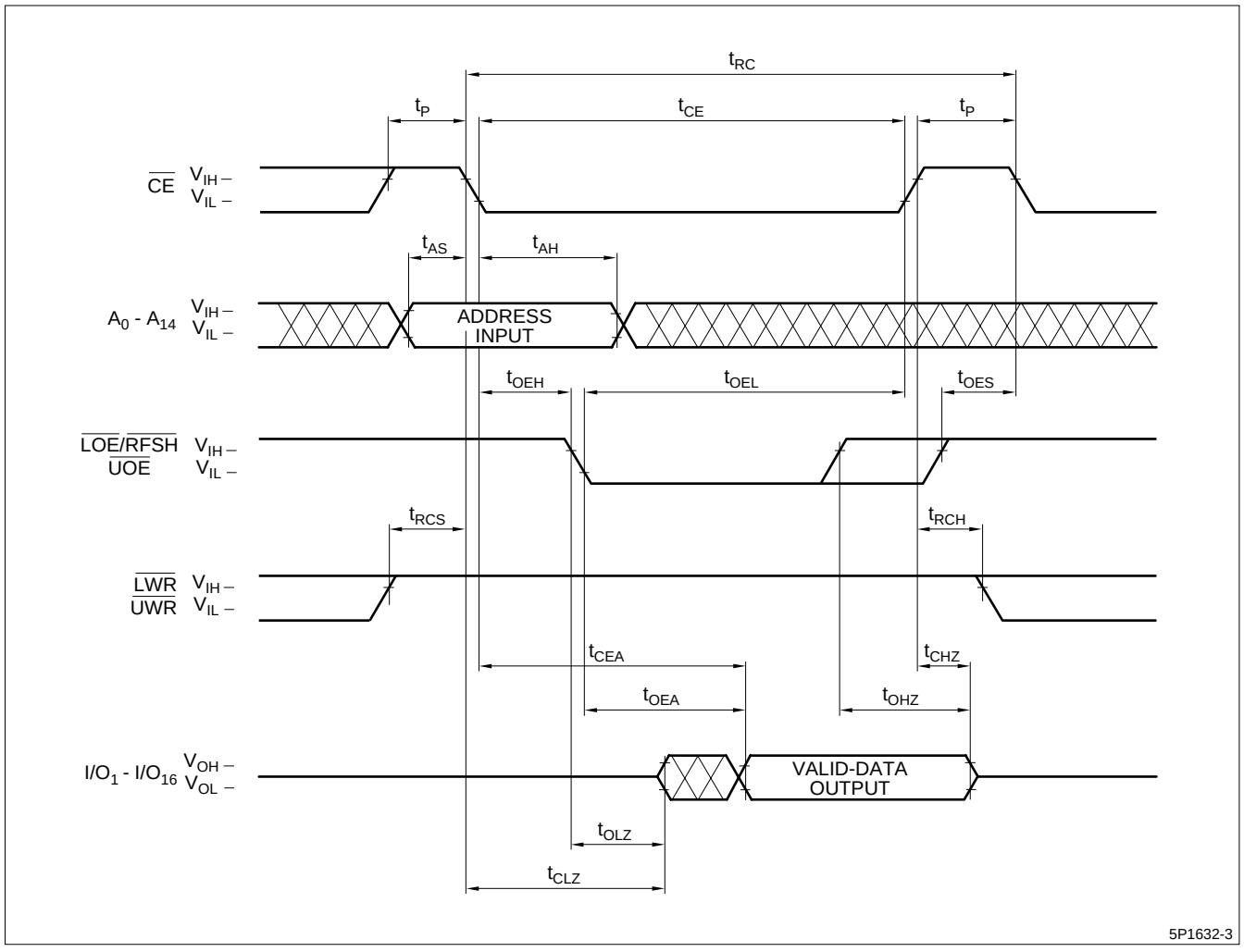


Figure 4. Read Cycle

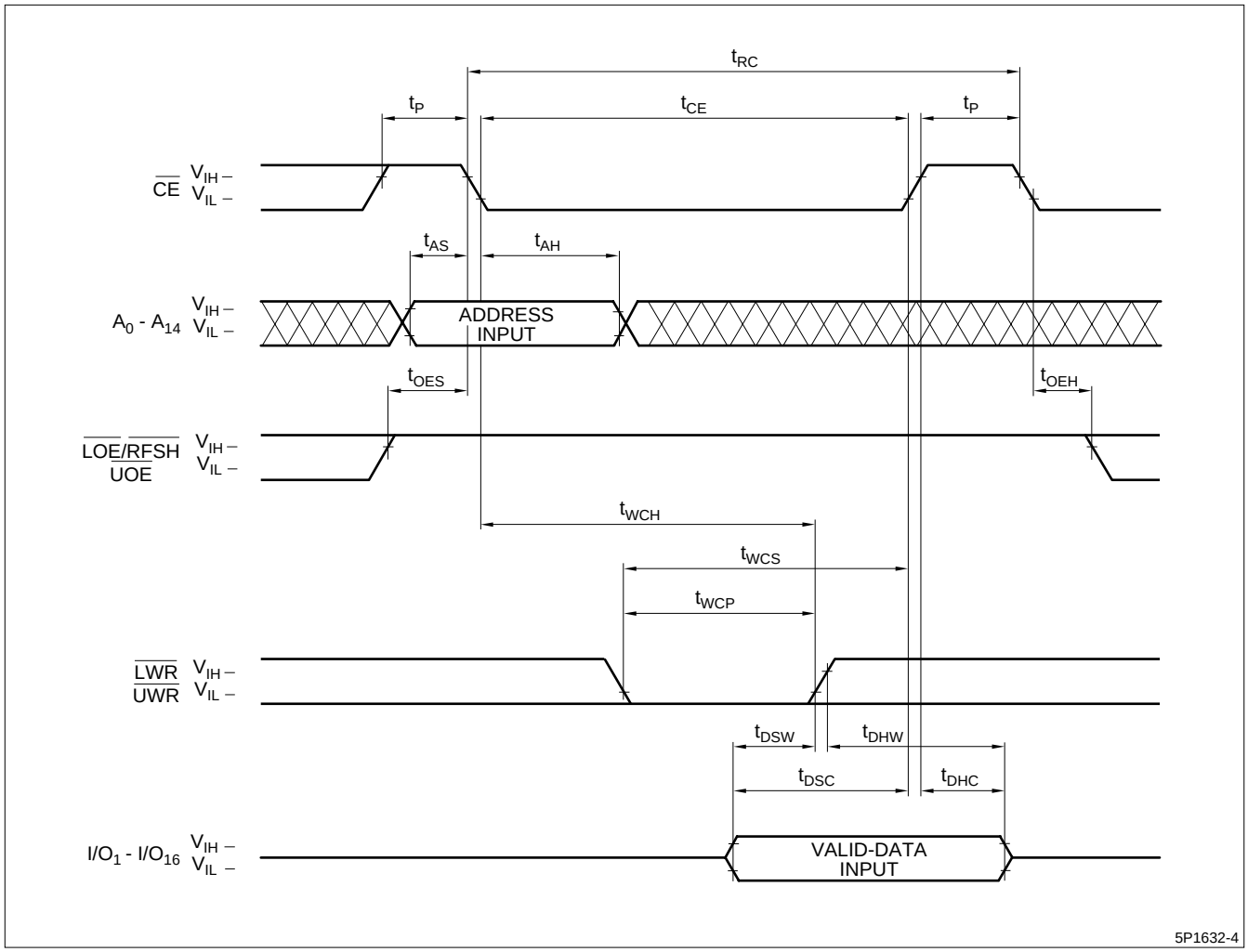


Figure 5. Write Cycle

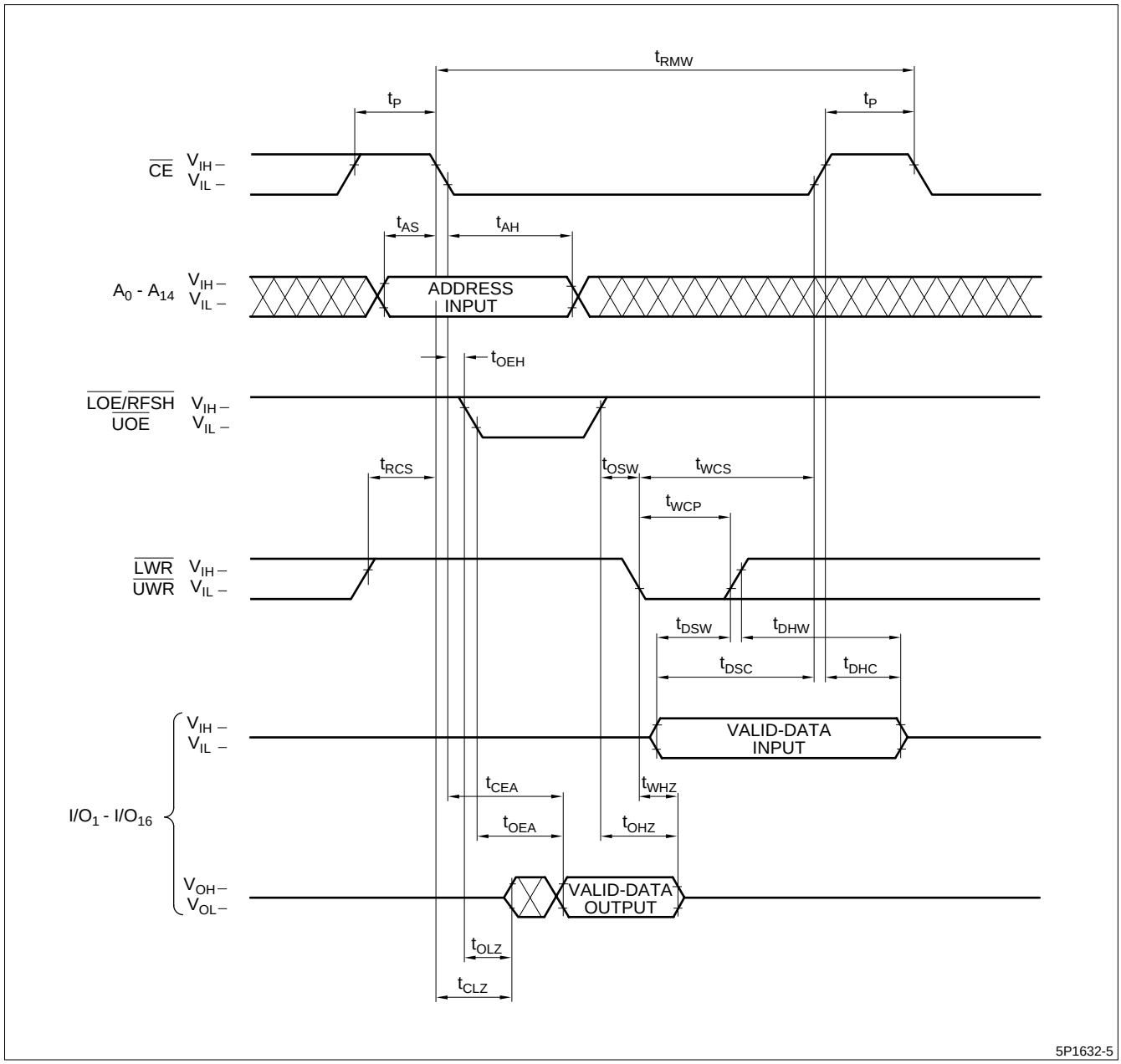


Figure 6. Read-Write Cycle

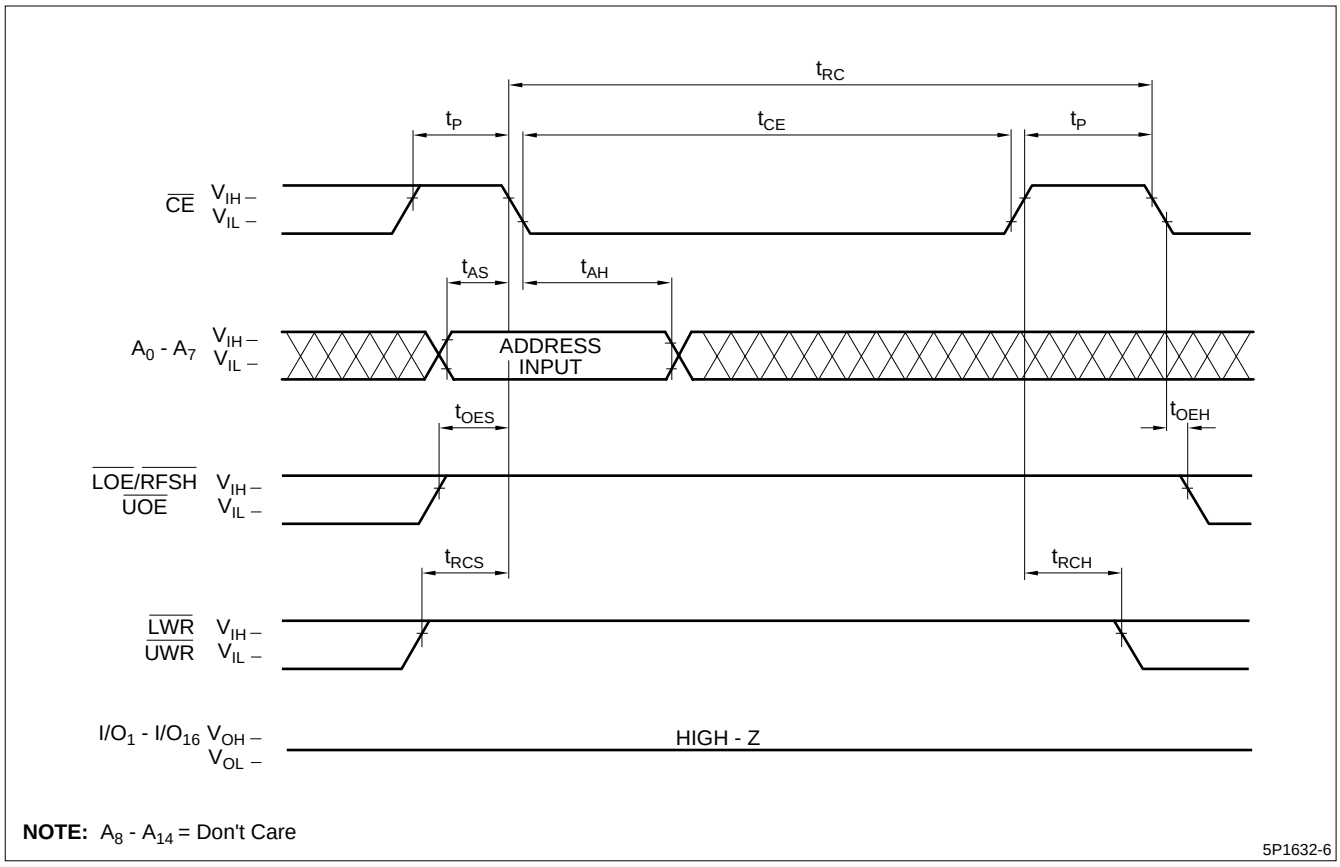


Figure 7. $\overline{CE}$ Only Refresh Cycle

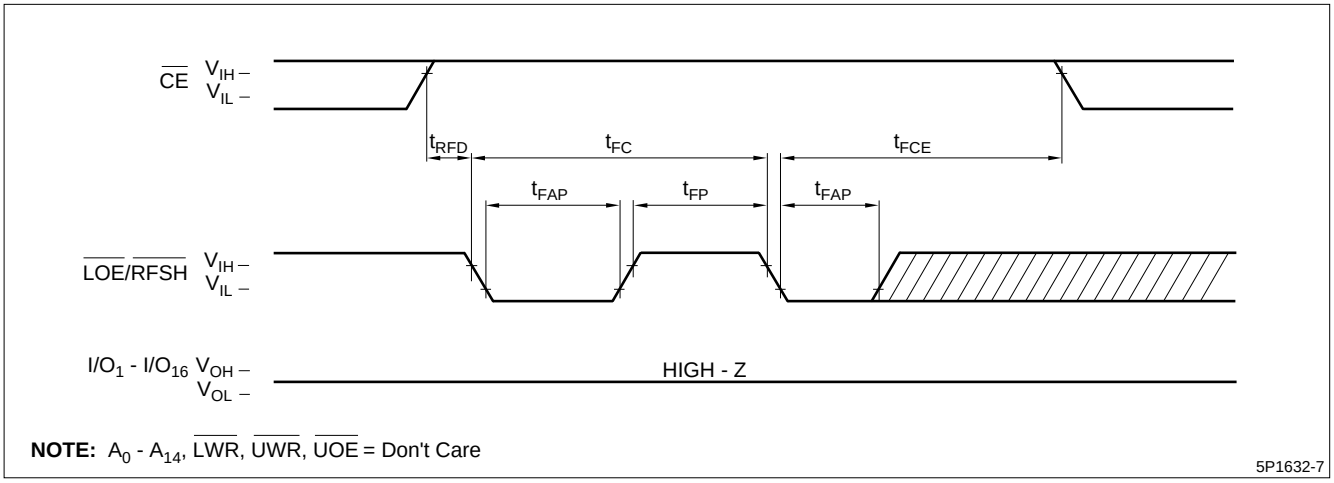
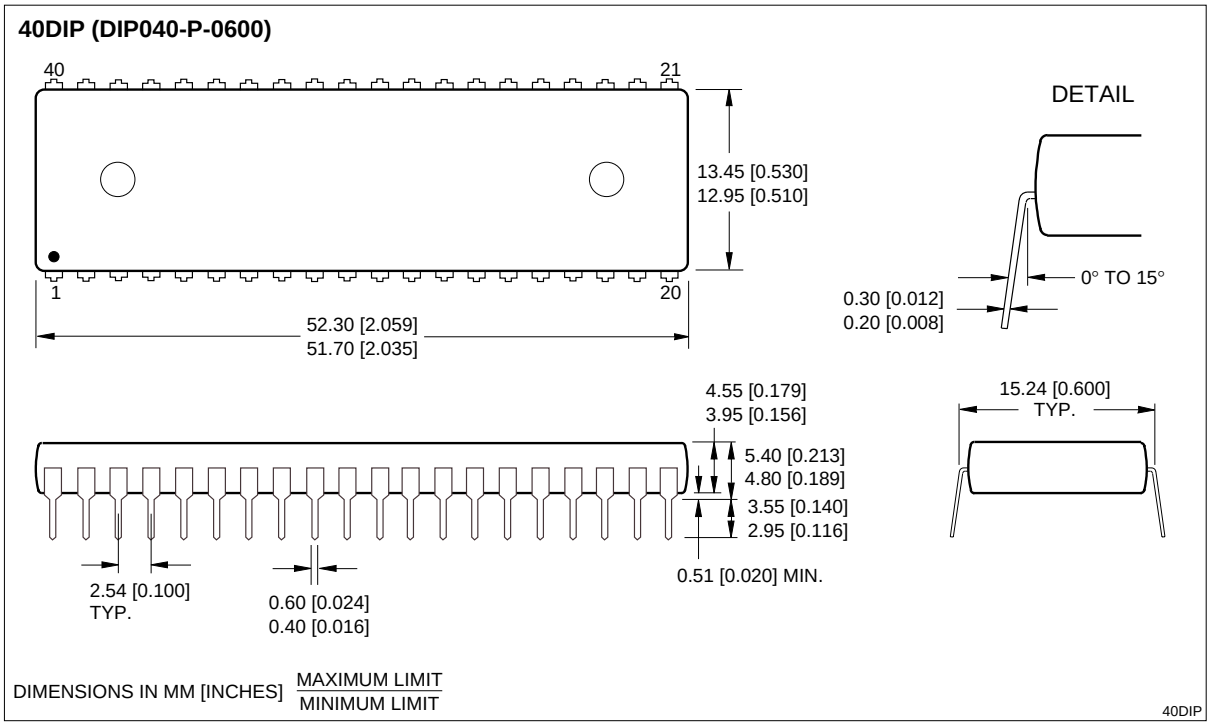
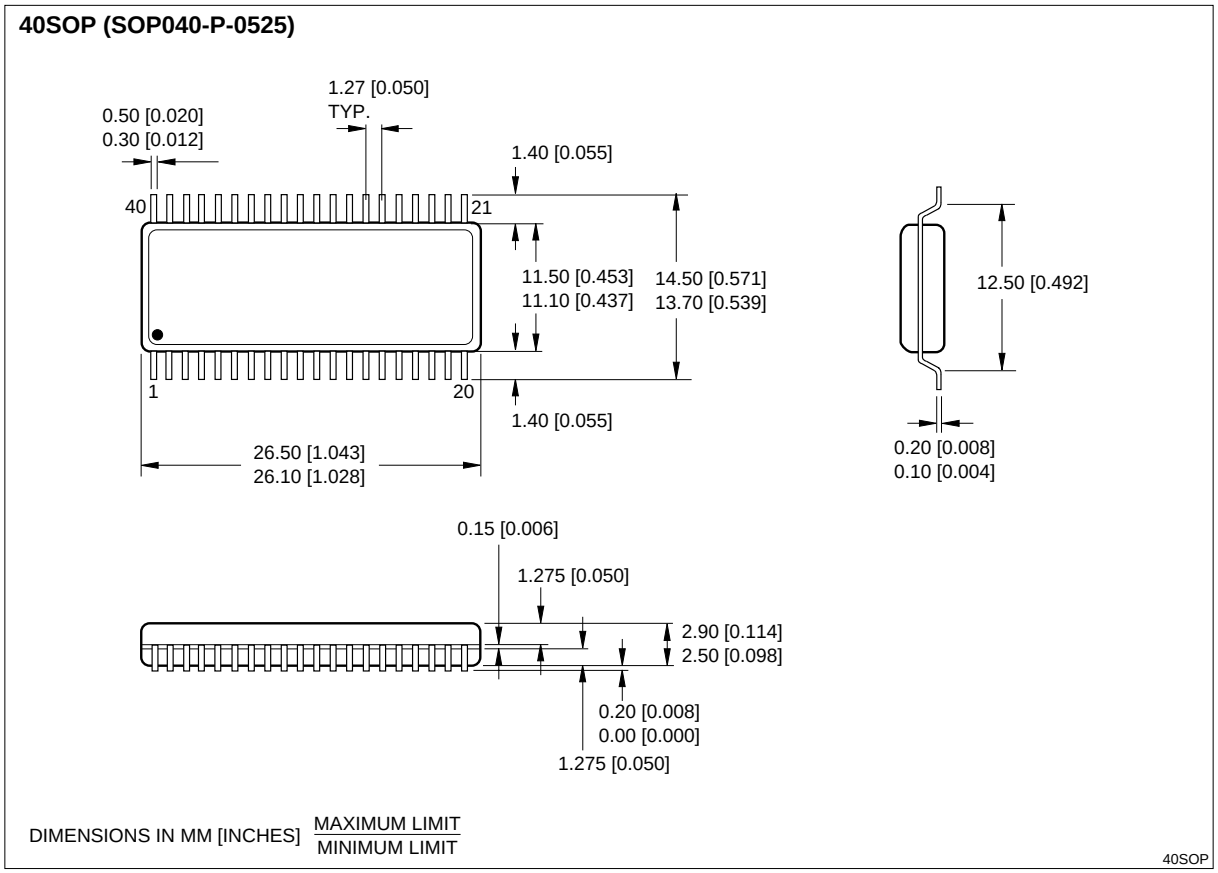


Figure 8. Auto Refresh Cycle

PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP

ORDERING INFORMATION