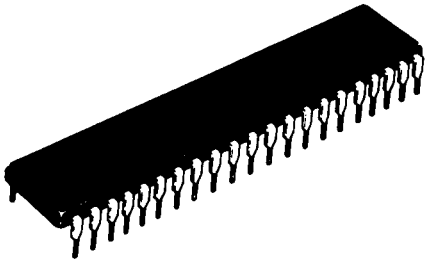
# HMCS44C(HD44801)
# HMCS44CL(HD44808)

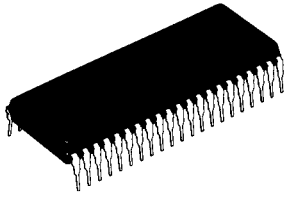
The HMCS44C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Event Counter on single chip. The HMCS44C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS44C provides the flexibility of microcomputers for battery powered and battery back-up applications.

HMCS44C,HMCS44CL



(DP-42)

HMCS44C

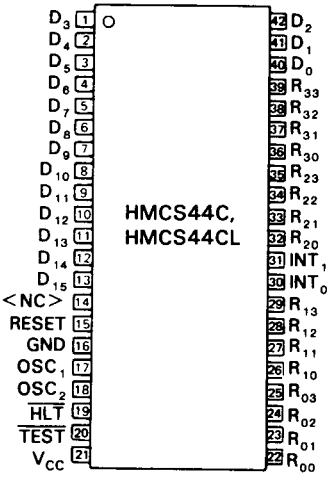


(DP-42S)

## ■ FEATURES

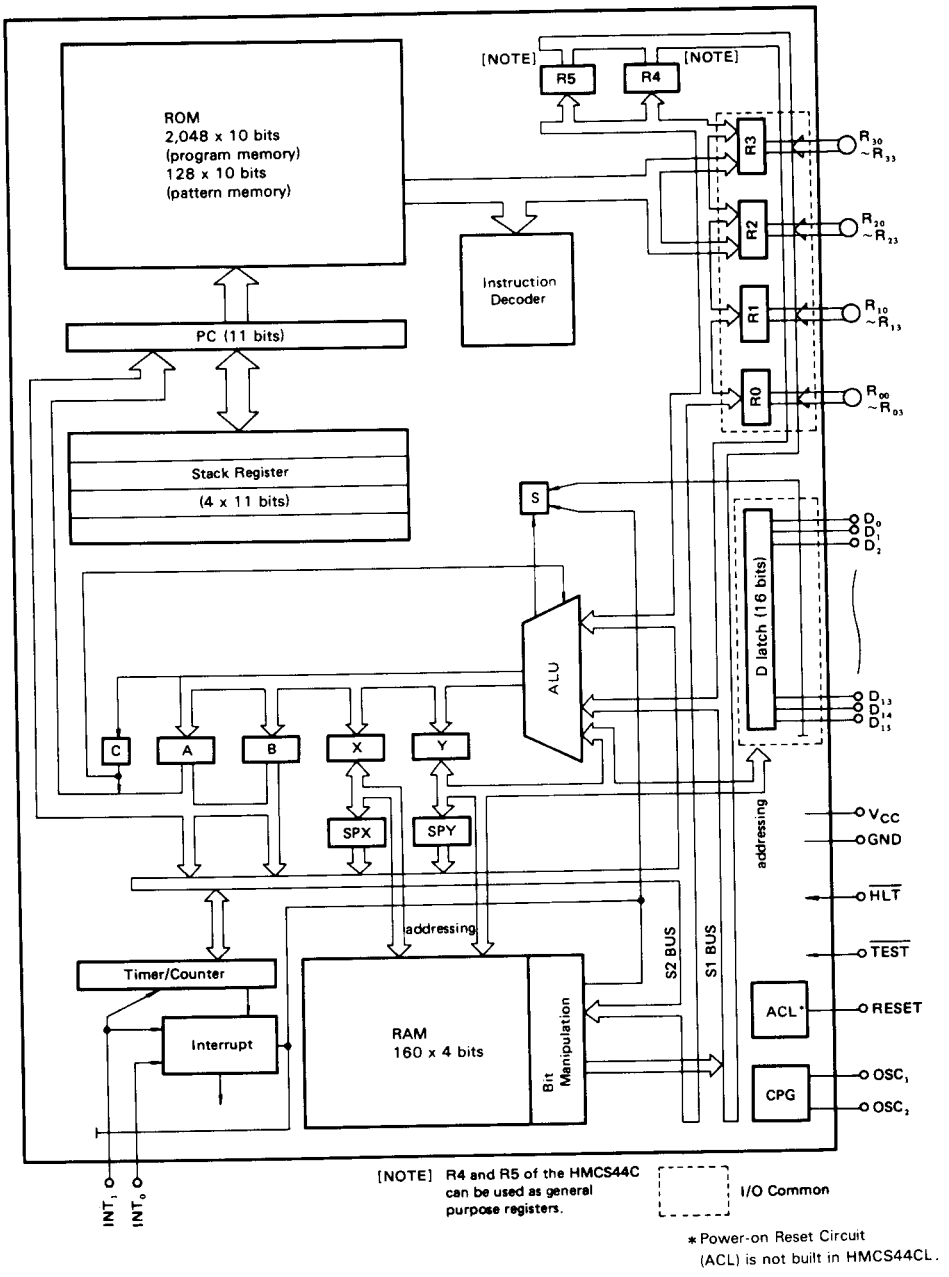
- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
  128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM (4 bits/Digit)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- Instruction Cycle Time: HMCS44C; 10 $\mu$s
  HMCS44CL; 20 $\mu$s
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  — Table Look Up Capability —
- Powerful Interrupt Function
  3 Interrupt Sources
  ├ 2 External Interrupt Lines
  └ Timer/Event Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator
- Built-in Power-on Reset Circuit (HMCS44C only)
- Low Operating Power Dissipation; 2mW typ.
- Stand-by Mode (Halt Mode); 50 $\mu$W max.
- CMOS Technology
- Single Power Supply: HMCS44C; 5V±10%
  HMCS44CL; 2.5V to 5.5V

## ■ PIN ARRANGEMENT




(Top View)

## ■ BLOCK DIAGRAM



■ **HMCS44C ELECTRICAL CHARACTERISTICS** ($V_{CC}$=5V±10%)

• **ABSOLUTE MAXIMUM RATINGS**

| Item | Symbol | Value | Unit | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | V | |
| Pin Voltage (1) | $V_{T1}$ | −0.3 to $V_{CC}$+0.3 | V | Except for pins specified by $V_{T2}$ |
| Pin Voltage (2) | $V_{T2}$ | −0.3 to +10.0 | V | Applied to only open drain output pins, open drain I/O common pins. |
| Maximum Total Output Current (1) | $-\Sigma I_{o1}$ | 45 | mA | [NOTE 3] |
| Maximum Total Output Current (2) | $\Sigma I_{o2}$ | 45 | mA | [NOTE 3] |
| Operating Temperature | $T_{opr}$ | −20 to +75 | °C | |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C | |

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

## • ELECTRICAL CHARACTERISTICS-1 ($V_{CC}$=5V±10%, Ta=−20°C to +75°C)

| Item | Symbol | Test Conditions | Value min | Value typ | Value max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input "Low" Voltage | $V_{IL}$ | | – | – | 1.0 | V | |
| Input "High" Voltage (1) | $V_{IH1}$ | | $V_{CC}$−1.0 | – | $V_{CC}$ | V | 2 |
| Input "High" Voltage (2) | $V_{IH2}$ | | $V_{CC}$−1.0 | – | 10 | V | 3 |
| Output "Low" Voltage | $V_{OL}$ | $I_{OL}$=1.6mA | – | – | 0.8 | V | |
| Output "High" Voltage (1) | $V_{OH1}$ | $-I_{OH}$=1.0mA | 2.4 | – | – | V | 4 |
| Output "High" Voltage (2) | $V_{OH2}$ | $-I_{OH}$=0.01mA | $V_{CC}$−0.3 | – | – | V | 5 |
| Interrupt Input Hold Time | $t_{iNT}$ | | 2·$T_{inst}$ | – | – | μs | |
| Interrupt Input Fall Time | $t_{fiNT}$ | | – | – | 50 | μs | |
| Interrupt Input Rise Time | $t_{riNT}$ | | – | – | 50 | μs | |
| Output "High" Current | $I_{OH}$ | $V_{OH}$=10V | – | – | 3 | μA | 6 |
| Input Leakage Current | $I_{IL}$ | $V_{in}$=0 to $V_{CC}$ | – | – | 1.0 | μA | 2 |
| | | $V_{in}$=0 to 10V | – | – | 3 | | 3 |
| Pull up MOS Current | $-I_P$ | $V_{CC}$=5V | 60 | – | 250 | μA | |
| Supply Current (1) | $I_{CC1}$ | $V_{in}$=$V_{CC}$, Ceramic Filter Oscillation | – | – | 2 | mA | 7 |
| Supply Current (2) | $I_{CC2}$ | $V_{in}$=$V_{CC}$, $R_f$ Oscillation, External Clock Operation | – | – | 1.0 | mA | 7 |
| Standby I/O Leakage Current | $I_{LS}$ | $\overline{HLT}$=1.0V, $V_{in}$=0 to $V_{CC}$ | – | – | 1 | μA | 2, 8 |
| | | $\overline{HLT}$=1.0V, $V_{in}$=0 to 10V | – | – | 3 | μA | 3, 8 |
| Standby Supply Current | $I_{CCS}$ | $V_{in}$=$V_{CC}$, $\overline{HLT}$=0.2V | – | – | 10 | μA | 9 |
| External Clock Operation | | | | | | | |
| External Clock Frequency | $f_{cp}$ | | 200 | 400 | 440 | kHz | |
| External Clock Duty | Duty | | 45 | 50 | 55 | % | |
| External Clock Rise Time | $t_{rcp}$ | | 0 | – | 0.2 | μs | |
| External Clock Fall Time | $t_{fcp}$ | | 0 | – | 0.2 | μs | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst}$=4/$f_{cp}$ | 9.1 | 10 | 20 | μs | |
| Internal Clock Operation ($R_f$ Oscillation) | | | | | | | |
| Clock Oscillation Frequency | $f_{OSC}$ | $R_f$=91kΩ±2% | 300 | – | 500 | kHz | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst}$=4/$f_{OSC}$ | 8.0 | – | 13.3 | μs | |
| Internal Clock Operation (Ceramic Filter Oscillation) | | | | | | | |
| Clock Oscillation Frequency | $f_{OSC}$ | Ceramic Filter Circuit | 392 | – | 408 | kHz | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst}$=4/$f_{OSC}$ | 9.8 | – | 10.2 | μs | |

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, $OSC_1$, $INT_0$, $INT_1$, and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the With Pull up MOS or CMOS type of I/O or Output pins.
[NOTE 6] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 7] I/O current is excluded.
[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at $V_{CC}$=5V±10% in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current ($I_{DH}$), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

- **ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75°C)
  Reset and Halt

| Item | Symbol | Test Conditions | Value min | Value max | Unit |
|---|---|---|---|---|---|
| Halt Duration Voltage | $V_{DH}$ | $\overline{HLT}$=0.2V | 2.3 | – | V |
| Halt Current | $I_{DH}$ | $V_{in}=V_{CC}$, $\overline{HLT}$=0.2V, $V_{DH}$=2.3V | – | 10 | μA |
| Halt Delay Time | $t_{HD}$ | | 100 | – | μs |
| Operation Recovery Time | $t_{RC}$ | | 100 | – | μs |
| $\overline{HLT}$ Fall Time | $t_{fHLT}$ | | – | 1000 | μs |
| $\overline{HLT}$ Rise Time | $t_{rHLT}$ | | – | 1000 | μs |
| $\overline{HLT}$ "Low" Hold Time | $t_{HLT}$ | | 400 | – | μs |
| $\overline{HLT}$ "High" Hold Time | $t_{OPR}$ | $R_f$ Oscillation, External Clock Operation | 0.1 | – | ms |
| | | Ceramic Filter Oscillation | 4 | – | |
| Power Supply Rise Time | $t_{rCC}$ | Built-in Reset, $\overline{HLT}=V_{CC}$ | 0.1 | 10 | ms |
| Power Supply OFF Time | $t_{OFF}$ | Built-in Reset, $\overline{HLT}=V_{CC}$ | 1 | – | ms |
| RESET Pulse Width (1) | $t_{RST1}$ | External Reset, $V_{CC}$=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ ($R_f$ Oscillation, External Clock Operation) | 1 | – | ms |
| | | External Reset $V_{CC}$=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ (Ceramic Filter Oscillation) | 4 | – | |
| RESET Pulse Width (2) | $t_{RST2}$ | External Reset $V_{CC}$=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ | $2 \cdot T_{inst}$ | – | μs |
| RESET Rise Time | $t_{rRST}$ | External Reset $V_{CC}$=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ | – | 20 | ms |
| RESET Fall Time | $t_{fRST}$ | External Reset $V_{CC}$=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ | – | 20 | ms |

[NOTE] All voltages are with respect to GND.

■ **HMCS44CL ELECTRICAL CHARACTERISTICS** ($V_{CC}$=2.5V to 5.5V)

- **ABSOLUTE MAXIMUM RATINGS**

| Item | Symbol | Value | Unit | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | V | |
| Pin Voltage (1) | $V_{T1}$ | −0.3 to $V_{CC}$+0.3 | V | Except for pins specified by $V_{T2}$ |
| Pin Voltage (2) | $V_{T2}$ | −0.3 to +10.0 | V | Applied to only open-drain output pins and open-drain I/O common pins. |
| Maximum Total Output Current (1) | $-\Sigma I_{o1}$ | 45 | mA | [NOTE 3] |
| Maximum Total Output Current (2) | $\Sigma I_{o2}$ | 45 | mA | [NOTE 3] |
| Operating Temperature | $T_{opr}$ | −20 to +75 | °C | |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C | |

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to GND.
[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

• **ELECTRICAL CHARACTERISTICS-1** ($V_{CC}$=2.5 to 5.5V, Ta=−20 to +75°C)

| Item | Symbol | Test Conditions | | Value min | Value typ | Value max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Input "Low" Voltage | $V_{IL}$ | | | – | – | 0.15·$V_{CC}$ | V | |
| Input "High" Voltage (1) | $V_{IH1}$ | | | 0.85·$V_{CC}$ | – | $V_{CC}$ | V | 2 |
| Input "High" Voltage (2) | $V_{IH2}$ | | | 0.85·$V_{CC}$ | – | 10 | V | 3 |
| Output "Low" Voltage | $V_{OL}$ | $I_{OL}$=0.4mA | | – | – | 0.4 | V | |
| Output "High" Voltage | $V_{OH}$ | $-I_{OH}$=0.08mA | | $V_{CC}$−0.4 | – | – | V | 4 |
| Interrupt Input Hold Time | $t_{iNT}$ | | | 2·$T_{inst}$ | – | – | μs | |
| Interrupt Input Fall Time | $t_{fiNT}$ | | | – | – | 50 | μs | |
| Interrupt Input Rise Time | $t_{riNT}$ | | | – | – | 50 | μs | |
| Output "High" Current | $I_{OH}$ | $V_{OH}$=10V | | – | – | 3 | μA | 5 |
| Input Leakage Current | $I_{IL}$ | $V_{in}$=0 to $V_{CC}$ | | – | – | 1.0 | μA | 2 |
| | | $V_{in}$=0 to 10V | | – | – | 3 | | 3 |
| Pull-up MOS Current | $-I_P$ | $V_{CC}$=3V | | 10 | – | 80 | μA | |
| Supply Current | $I_{CC}$ | $V_{in}$=$V_{CC}$, $V_{CC}$=3V ($f_{OSC}$/$f_{cp}$=200kHz) $R_f$ Oscillation, External Clock Operation | | – | – | 140 | μA | 6 |
| Standby I/O Leakage Current | $I_{LS}$ | $\overline{HLT}$=0.5V | $V_{in}$=0 to $V_{CC}$ | – | – | 1 | μA | 2, 7 |
| | | | $V_{in}$=0 to 10V | – | – | 3 | μA | 3, 7 |
| Standby Supply Current | $I_{CCS}$ | $V_{in}$=$V_{CC}$, $\overline{HLT}$=0.1V | $V_{CC}$=2.5 to 3.5V | – | – | 6 | μA | 8 |
| | | | $V_{CC}$=2.5 to 5.5V | – | – | 10 | μA | |
| External Clock Operation | | | | | | | | |
| External Clock Frequency | $f_{cp}$ | | | 130 | 200 | 240 | kHz | |
| External Clock Duty | Duty | | | 45 | 50 | 55 | % | |
| External Clock Rise Time | $t_{rcp}$ | | | 0 | – | 0.2 | μs | |
| External Clock Fall Time | $t_{fcp}$ | | | 0 | – | 0.2 | μs | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst}$=4/$f_{cp}$ | | 16.8 | 20 | 30.8 | μs | |
| Internal Clock Operation ($R_f$ Oscillation) | | | | | | | | |
| Clock Oscillation Frequency | $f_{OSC}$ | $R_f$=180kΩ±2%, $V_{CC}$=2.5 to 3.5V | | 130 | – | 250 | kHz | |
| | | $R_f$=180kΩ±2%, $V_{CC}$=2.5 to 5.5V | | 130 | – | 350 | | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst}$=4/$f_{OSC}$, $V_{CC}$=2.5 to 3.5V | | 16 | – | 30.8 | μs | |
| | | $T_{inst}$=4/$f_{OSC}$, $V_{CC}$=2.5 to 5.5V | | 11.4 | – | 30.8 | | |

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, $OSC_1$, $INT_0$, INT, and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 6] I/O current is excluded.
[NOTE 7] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 8] I/O current is excluded.
The Standby Supply Current is the supply current at $V_{CC}$=2.5 to 5.5V in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current ($I_{DH}$), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

- **ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75°C)
  Reset and Halt

| Item | Symbol | Test Conditions | Value | | Unit |
|---|---|---|---|---|---|
| | | | min | max | |
| Halt Duration Voltage | $V_{DH}$ | $\overline{HLT}$=0.2V | 2.0 | – | V |
| Halt Current | $I_{DH}$ | $V_{in}=V_{CC}$, $\overline{HLT}$=0.1V, $V_{DH}$=2.0V | – | 4 | μA |
| Halt Delay Time | $t_{HD}$ | | 200 | – | μs |
| Operation Recovery Time | $t_{RC}$ | | 200 | – | μs |
| $\overline{HLT}$ Fall Time | $t_{fHLT}$ | | – | 1000 | μs |
| $\overline{HLT}$ Rise Time | $t_{rHLT}$ | | – | 1000 | μs |
| $\overline{HLT}$ "Low" Hold Time | $t_{HLT}$ | | 800 | – | μs |
| $\overline{HLT}$ "High" Hold Time | $t_{OPR}$ | $R_f$ Oscillation, External Clock Operation $V_{CC}$=2.5 to 5.5V | 0.2 | – | ms |
| RESET Pulse Width (1) | $t_{RST1}$ | External Reset, $V_{CC}$=2.5 to 5.5V, $\overline{HLT}=V_{CC}$ ($R_f$ Oscillation, External Clock Operation) | 2 | – | ms |
| RESET Pulse Width (2) | $t_{RST2}$ | External Reset, $V_{CC}$=2.5 to 5.5V, $\overline{HLT}=V_{CC}$ | $2 \cdot T_{inst}$ | – | μs |
| RESET Fall Time | $t_{fRST}$ | $\overline{HLT}=V_{CC}$ | – | 20 | ms |
| RESET Rise Time | $t_{rRST}$ | $\overline{HLT}=V_{CC}$ | – | 20 | ms |

[NOTE] All voltages are with respect to GND.

## ■ SIGNAL DESCRIPTION

The input and output signals for the HMCS44C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

- **$V_{CC}$ and GND**
  Power is supplied to the HMCS44C using these two pins. $V_{CC}$ is power and GND is the ground connection.

- **RESET**
  This pin resets the HMCS44C independently of the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS44C. The HMCS44C can be reset by pulling RESET high.
  Refer to RESET FUNCTION for additional information.

- **$OSC_1$ and $OSC_2$**
  These pins provide control input for the built-in oscillator circuit. Resistor and capacitor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized.
  Refer to OSCILLATOR for recommendations about these pins.

- **$\overline{HLT}$**
  This pin is used to enter the HMCS44C into the Halt State.
  Refer to HALT FUNCTION for details of the Halt Mode.

- **$\overline{TEST}$**
  This pin is not for user application and must be connected to $V_{CC}$.

- **$INT_0$ and $INT_1$**
  These pins generate interrupt request to the HMCS44C.
  Refer to INTERRUPTS for additional information.

- **$R_{00}$ to $R_{03}$, $R_{10}$ to $R_{13}$, $R_{20}$ to $R_{23}$, $R_{30}$ to $R_{33}$**
  These 16 lines are arranged into four 4-bit Data Input/Output Common Channels. The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction.
  Refer to INPUT/OUTPUT for additional information.

- **$D_0$ to $D_{15}$**
  These lines are sixteen 1-bit Discrete Input/Output Common Pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register. The $D_0$ to $D_3$ pins are also addressed directly by the operand of input/output instruction.
  Refer to INPUT/OUTPUT for additional information.

## ■ ROM

- **ROM Address Space**
  ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS44C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.
  The ROM address is composed of the program area (page 0 to page 31) and the pattern area (pages 61, 62) (64 words/page).
  The ROM capacity is 2,176 words (1 word = 10 bits) in all.
  Only the program area can contain both the instructions and the patterns (constants).
  The ROM address space is shown in Figure 1.

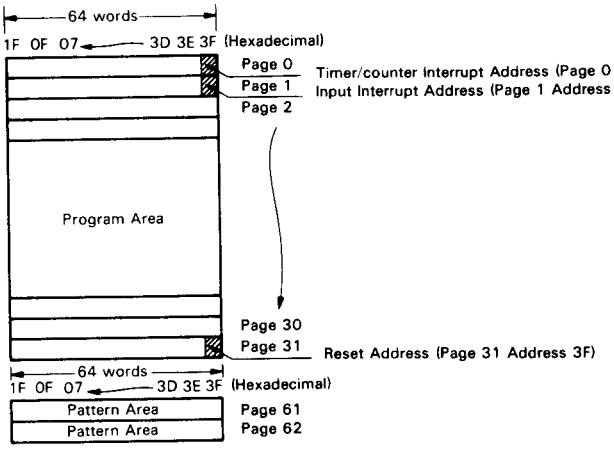



Figure 1 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. It consists of the page part and the address part as shown in Figure 2.

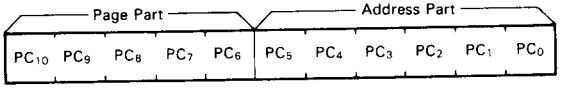



Figure 2 Configuration of Program Counter

Once a certain value is loaded into a page part, it is unchanged until other value is loaded by the program. Any number among 0 to 31 can be set in the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexadecimal system is shown in Table 1. This sequence forms a loop and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the page part is changed.

Table 1 Program Counter Address Part Sequence

| Decimal | Hexadecimal | Decimal | Hexadecimal | Decimal | Hexadecimal |
|---|---|---|---|---|---|
| 63 | 3F | 5 | 05 | 9 | 09 |
| 62 | 3E | 11 | 0B | 19 | 13 |
| 61 | 3D | 23 | 17 | 38 | 26 |
| 59 | 3B | 46 | 2E | 12 | 0C |
| 55 | 37 | 28 | 1C | 25 | 19 |
| 47 | 2F | 56 | 38 | 50 | 32 |
| 30 | 1E | 49 | 31 | 37 | 25 |
| 60 | 3C | 35 | 23 | 10 | 0A |
| 57 | 39 | 6 | 06 | 21 | 15 |
| 51 | 33 | 13 | 0D | 42 | 2A |
| 39 | 27 | 27 | 1B | 20 | 14 |
| 14 | 0E | 54 | 36 | 40 | 28 |
| 29 | 1D | 45 | 2D | 16 | 10 |
| 58 | 3A | 26 | 1A | 32 | 20 |
| 53 | 35 | 52 | 34 | 0 | 00 |
| 43 | 2B | 41 | 29 | 1 | 01 |
| 22 | 16 | 18 | 12 | 3 | 03 |
| 44 | 2C | 36 | 24 | 7 | 07 |
| 24 | 18 | 8 | 08 | 15 | 0F |
| 48 | 30 | 17 | 11 | 31 | 1F |
| 33 | 21 | 34 | 22 | | |
| 2 | 02 | 4 | 04 | | |

- **Designation of ROM Address and ROM Code**

The page part of the ROM address is represented by decimal and the address part is divided into 2 parts (2 bits and 4 bits) and represented by hexadecimal.

One word (10 bits) is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit $O_{10}$) and represented by hexadecimal. The examples are shown in Figure 3.

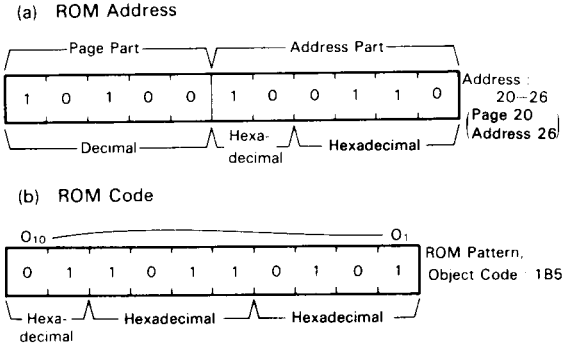



Figure 3 Designation of ROM Address and ROM Code

## ■ PATTERN GENERATION

The pattern (constants) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

- **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part is ORed with the upper 2 bits of B register, the Carry F/F and the operand p ($p_0$, $p_1$). The upper bit ($p_2$) of the operand is for referring to the pattern area.

The contents of the program counter is only modified apparently and is not changed. Then the address is counted up after the execution of the pattern instruction and the next instruction is executed.

The pattern instruction is executed in 2 cycles.

Even when interrupt is enable, interrupt is disabled in the second cycle of the pattern instruction. However, the interrupt request is latched into the interrupt request F/F.

- **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii)The pattern is loaded into the Data I/O registers R2 and R3.

The command bits ($O_9$, $O_{10}$) in the pattern determine which way is taken.

Mode (i) is performed when $O_9$ is "1" and mode (ii) is performed when $O_{10}$ is "1".

Mode (i) and mode (ii) are simultaneously performed when both $O_9$ and $O_{10}$ are "1".

The correspondence of each bit of the pattern is shown in Figure 5.

Examples of how to use pattern instruction is shown in Table 2.

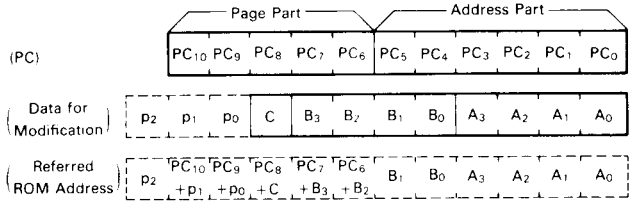



Figure 4 ROM Addressing for Pattern Generation

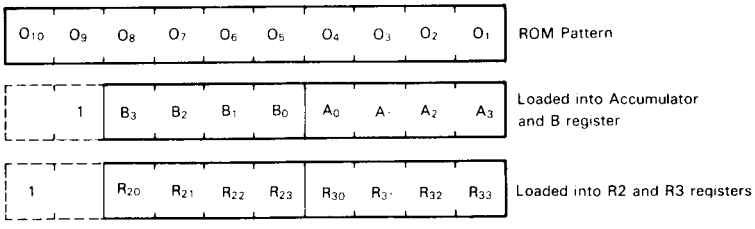



Figure 5 Correspondence of Each Bit of Pattern



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Table 2 Example of how to use Pattern Instruction

| Before Execution | | | | | Referred ROM Address | Pattern | After Execution | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PC Value | p | C | B | A | | | B | A | R2 | R3 |
| 0-3F | 1 | 0 | A | 0 | 10-20 | 12D | 2 | B | – | – |
| 0-3F | 7 | 1 | 4 | 0 | 61-00 | 22D | – | – | 4 | B |
| 30-00 | 4 | 0/1 | 0 | 9 | 62-09 | 32D | 2 | B | 4 | B |
| 30-00 | 4 | 0/1 | F | 9 | 63-39 | | | | | |

"–" means that the value is unchanged after the execution.
"0/1" means that either "0" or "1" will do.

## ■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways.

They are explained in the following paragraphs.

### • BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, $O_6$ to $O_1$) are transferred to the lower 6 bits of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 6.

### • LPU

By LPU instruction, a jump between pages is performed.

The lower 5 bits of the ROM Object Code (operand u) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. Therefore, the cycle just after the issuing of this instruction is on the same page and the page jump is performed at the next cycle.

This instruction is a conditional instruction and performed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped. The operation is shown in Figure 7.

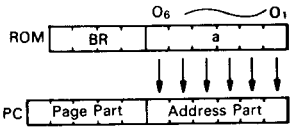



Figure 6 BR Operation

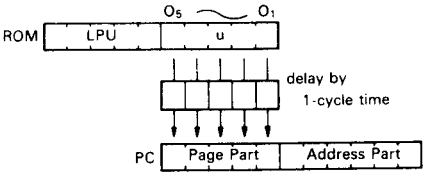



Figure 7 LPU Operation

### • BRL

By BRL instruction, the program branches to an address in any page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two steps as follows.

BRL a – b → LPU a
<Jump to address b on page a> BR b

BRL instruction is a conditional instruction because of its characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1".

### • TBR (Table Branch)

By TBR instruction, the program branches referring to the table.

The program counter is modified with the accumulator, the B register, the Carry F/F, the operand p. The method for modification is shown in Figure 8.

The accumulator and the lower 2 bits of B register are assigned into the address part of the program counter. The upper 2 bits of B register, Carry F/F, and the operand $p_1$, $p_0$ are ORed with the page part of the program counter.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

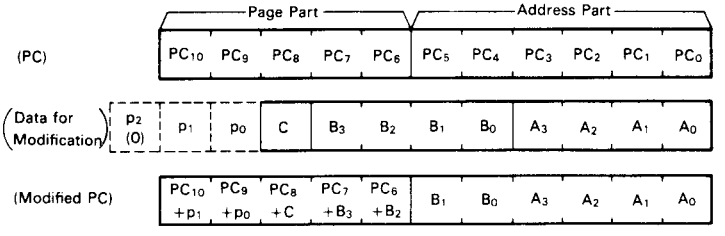



Figure 8 Modification of Program Counter by TBR Instruction

## ■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

### • CAL

By CAL instruction, subroutine jump to an address in the Subroutine Page is performed.

The Subroutine Page is page 0.

The address next to CAL instruction address is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 9.

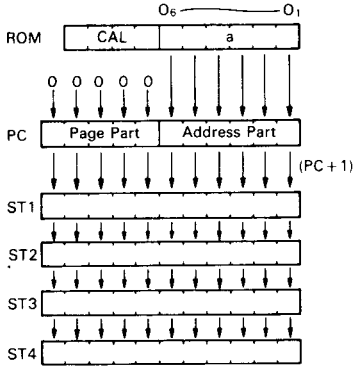



Figure 9 Subroutine Jump Stacking Order

The page part of the program counter is 0. The lower 6 bits (operand a, $O_6$ to $O_1$) of the ROM Object Code is transferred to the address part of the program counter.

The HMCS44C has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1"

### • CALL

By CALL instruction, subroutine jump to an address in any page is performed.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two steps as follows.

CALL a – b → LPU a
<Subroutine jump to address b on page a> CAL b

CALL instruction is conditional because of its characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

## ■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 160 digits (640 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits, 16 digits (MR0 to MR15), are called "Memory Register (MR)". The memory register can be exchanged with the accumulator by XAMR instruction.

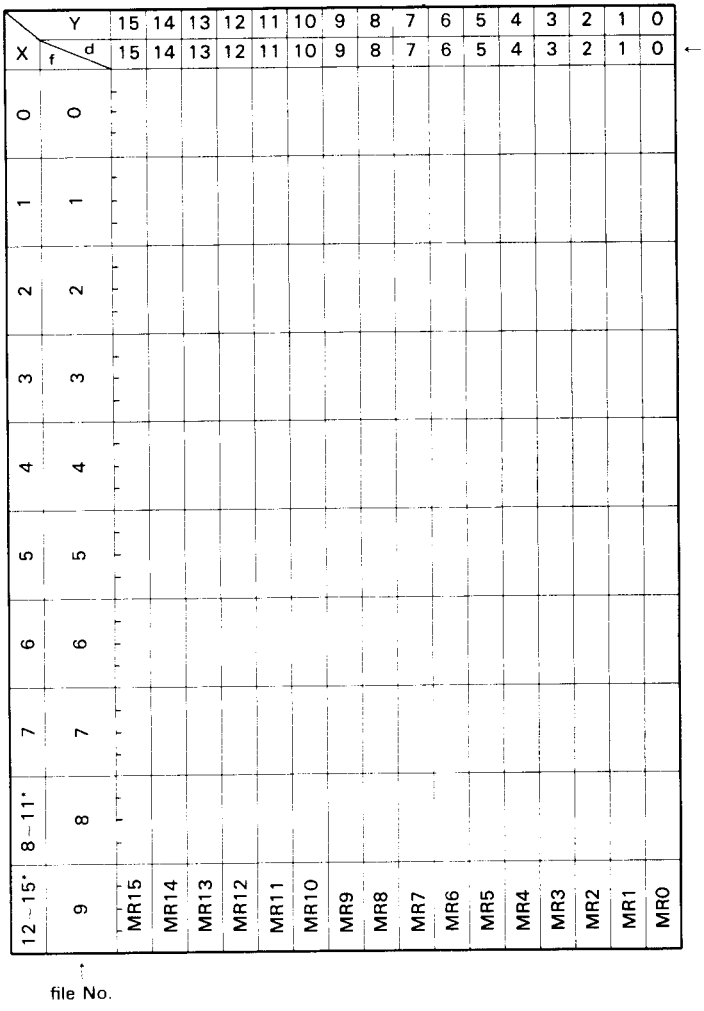
The RAM address space is shown in Figure 10.

If an instruction consists of a simultaneous read/write operation of RAM (exchange between the contents of RAM and those of the register), the writing data doesn't affect the reading data because read operation precedes write operation.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status F/F "1" and makes it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 11.




* The file 8 is selected when X register has any value among 8 to 11, and the file 9 is selected when 12 to 15.

Figure 10 RAM Address Space

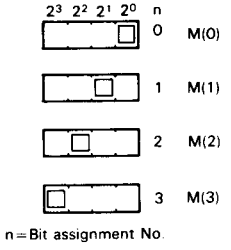



Figure 11 RAM Bit and Operand n

## ■ REGISTER

The HMCS44C has six 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

### • Status F/F (S)

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1"

- **Accumulator (A; A Register) and Carry F/F (C)**

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F respectively. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

- **B Register (B)**

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

- **X Register (X)**

The result of ALU operation (4 bits) is loaded into this register. The X register is exchangeable with the SPX register, and addresses the RAM file and is composed of 4-bit register.

- **SPX Register (SPX)**

The SPX register is exchangeable with the X register.

The SPX register is used to stack the contents of the X register and expand the addressing system of RAM in combination with the X register. It is composed of 4-bit register.

- **Y Register (Y)**

The result of ALU operation (4 bits) is loaded into this register. The Y register is exchangeable with the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digits and 1-bit Discrete I/Os.

- **SPY Register (SPY)**

The SPY register is exchangeable with the Y register. The SPY register is used to stack the contents of the Y register and expand the addressing system of RAM and 1-bit Discrete I/O in combination with the Y register.

## ■ INPUT/OUTPUT

- **4-bit Data Input/Output Channel (R)**

The HMCS44C has four 4-bit Data I/O Common Channels (R0, R1, R2, R3).

The 4-bit registers (Data I/O Registers) are attached to R1, R2 and R3 channels.

Each channel is directly addressed by the operand p of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R3 via the bus lines. ROM bit patterns are loaded into the Data I/O Registers R2 and R3 by the pattern instruction.

The input instruction inputs the 4-bit data into the accumulator and the B register through the channels R0 to R3. Note that, since the Data I/O Register output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register output and the pin input.

Therefore, the Data I/O Register should be set to 15 (all bits of the Data I/O Register is "1") not to affect the pin input before execution of input instruction.

The block diagram is shown in Figure 12 and the I/O timing is in Figure 13.

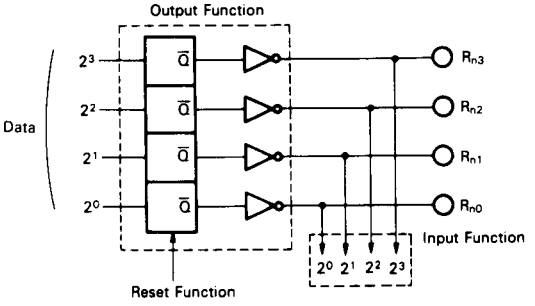



Figure 12 4-bit Data I/O Block Diagram

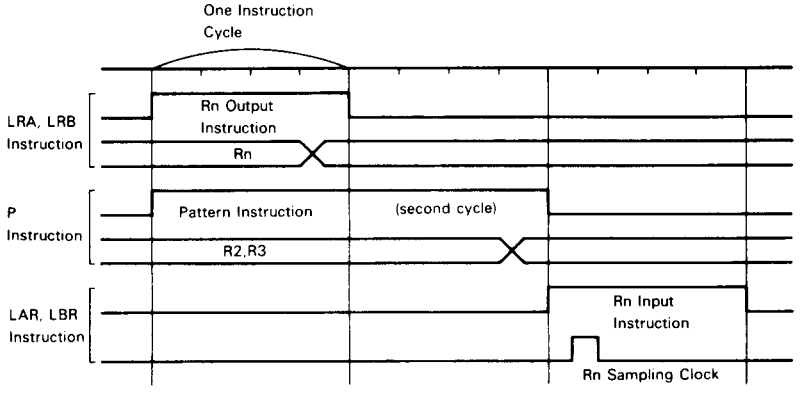



Figure 13 4-bit Data I/O Timing

- **1-bit Discrete Input/Output Common Pin (D)**

The HMCS44C has sixteen 1-bit Discrete I/O Common Pins.

The 1-bit Discrete I/O Common pin consists of a 1-bit latch and an I/O common pin.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and level ("0" or "1") of the addressed pin can be tested by an input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is

wired logic of the latch output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before execution of input instruction.

The $D_0$ to $D_3$ pins are also addressed directly by the operand n of input/output instruction and can be set or reset.

The block diagram is shown in Figure 14 and the I/O timing is in Figure 15.

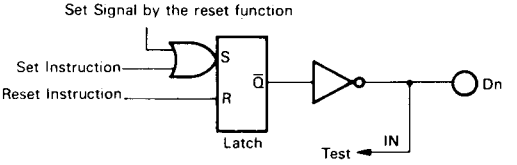



Figure 14 1-bit Discrete I/O Block Diagram

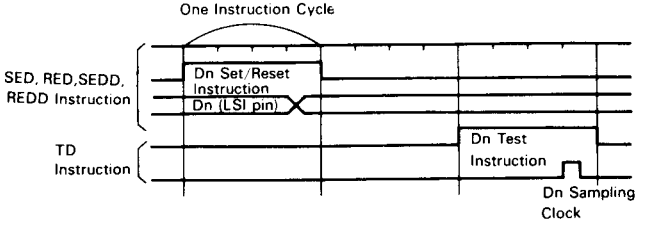
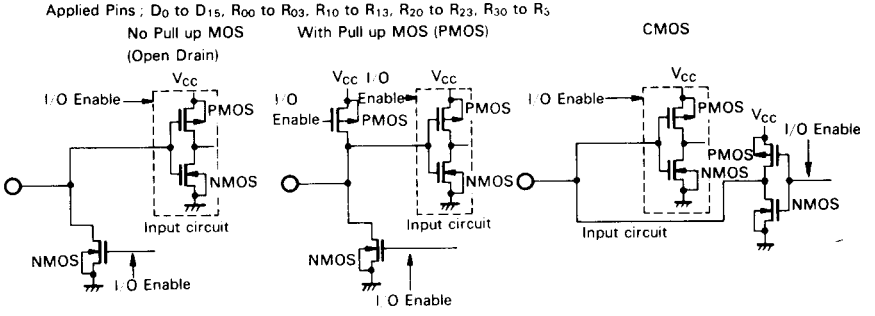



Figure 15 1-bit Discrete I/O Timing

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain and With Pull up MOS using a mask option as shown in Figure 16.




*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit, Pull up MOS and NMOS output and sets CMOS output to high impedance (PMOS, NMOS; OFF).

Figure 16 I/O Configuration

- **TIMER/COUNTER**

The timer/counter consists of 4-bit counter and 6-bit prescaler as shown in Figure 17.

The counter operates in the Timer Mode or Counter Mode according to the counting object. In the timer mode it counts overflow output pulse from the prescaler, and in the Counter Mode it counts $INT_1$ input pulse (counts leading edge), and increments to 15. Mode selection is determined according to the state of the CF. When the counter reaches zero (returns from 15), overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow \cdots$).

The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 3.

The prescaler is a 6-bit frequency divider. It generates 100/64 kHz pulses by dividing the system clock by 64. The prescaler is cleared when the data is loaded into the 4-bit counter by LTA, LTI instructions. The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output pulse is generated from the prescaler. During operation of the LSI, the prescaler operates and cannot be stopped.

The CF is the flip-flop (F/F) which controls the counter input. When the CF F/F is "1", input pulse of $INT_1$ is input to the counter (Counter Mode). When the CF is "0", prescaler overflow output pulse is input to the counter (Timer Mode).

The TF is the flip-flop (F/F) which masks the interrupt request from the timer/counter. It is set, reset and tested by instructions. If the overflow output pulse of the counter is generated when the TF F/F is "0", an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is "1", no interrupt request occurs. So it can be used as timer/counter interrupt mask.

The pulse width of $INT_1$ in the Counter Mode should be two or more cycles both at "High" and "Low" levels as shown in Figure 18.

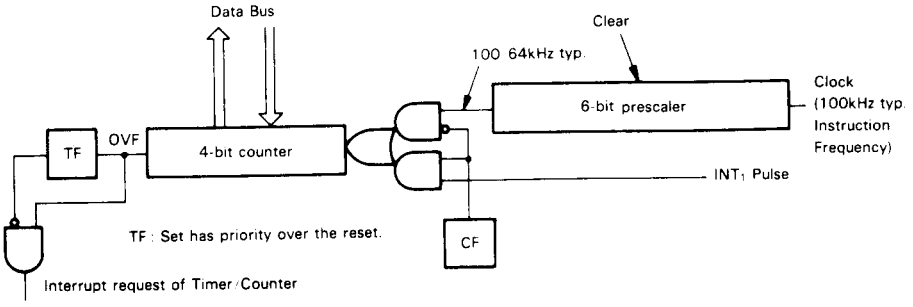



Figure 17 Timer Counter Block Diagram

Table 3 Timer Range

| Specified Value | Cycles | Time (ms) | Specified Value | Cycles | Time (ms) |
|---|---|---|---|---|---|
| 0 | 1,024 | 10.24 | 8 | 512 | 5.12 |
| 1 | 960 | 9.60 | 9 | 448 | 4.48 |
| 2 | 896 | 8.96 | 10 | 384 | 3.84 |
| 3 | 832 | 8.32 | 11 | 320 | 3.20 |
| 4 | 768 | 7.68 | 12 | 256 | 2.56 |
| 5 | 704 | 7.04 | 13 | 192 | 1.92 |
| 6 | 640 | 6.40 | 14 | 128 | 1.28 |
| 7 | 576 | 5.76 | 15 | 64 | 0.64 |

[NOTE] Time is based on instruction frequency 100kHz. (one instruction cycle = 10$\mu$s)

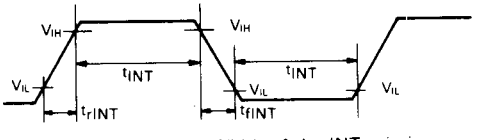



Figure 18 The Pulse Width of the $INT_1$ pin in the Counter Mode

## ■ INTERRUPT

The HMCS44C can be interrupted in two different ways: through the external interrupt input pins ($INT_0$, $INT_1$) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the contents of the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively. At that time, the Interrupt Enable F/F (I/E) is set and the address jumps to a fixed destination (Interrupt Address), and then the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI (Return Interrupt) instruction which sets the I/E F/F simultaneously with the RTN instruction.

The Interrupt Address:

Input Interrupt Address . . . . .
Page 1 Address 3F

Timer/Counter Interrupt Address . . . . .
Page 0 Address 3F

The input interrupt has priority over the timer/counter interrupt.

The $INT_0$ and $INT_1$ pins have interrupt request functions.

Each pin consists of a circuit which generates leading pulse and the interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the $INT_0$ or $INT_1$ pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, it is an interrupt mask for $INT_0$ or $INT_1$. (If a leading pulse is generated, no interrupt request occurs.)

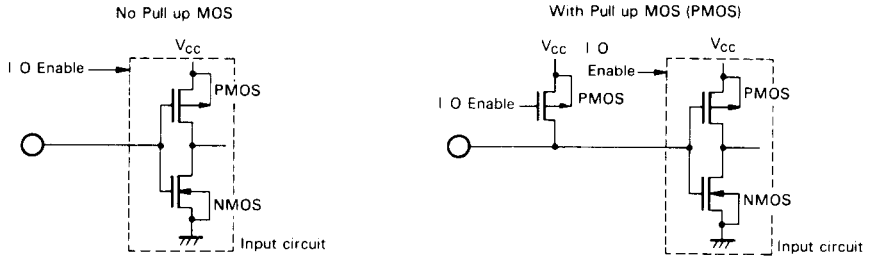
An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS44C gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the $INT_0$ pin and the $INT_1$ pin can be tested by interrupt instruction. Therefore, the $INT_0$ and the $INT_1$ can be used as additional input pins with latches.

The $INT_0$ pin and $INT_1$ pin can be provided with Pull up MOS using a mask option as shown in Figure 19.

An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are the same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt servicing is achieved.

The interrupt circuit block diagram is shown in Figure 20.




*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit and Pull up MOS.

Figure 19 Configuration of $INT_0$ and $INT_1$

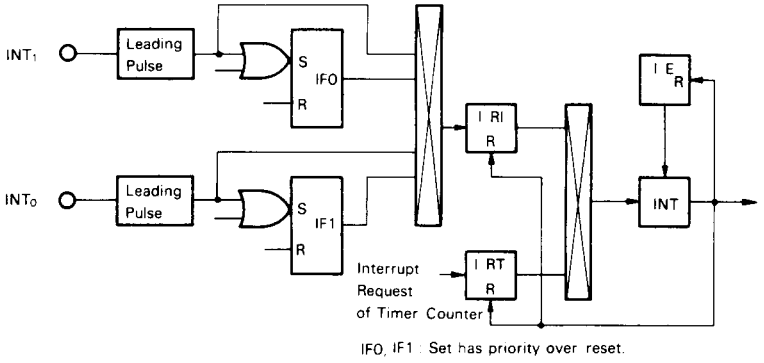



Figure 20 Interrupt Circuit Block Diagram

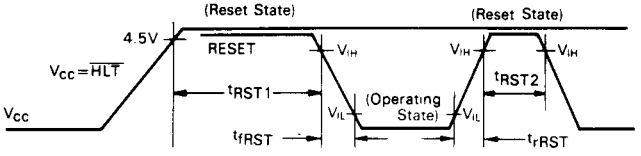
## ■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS44C gets into operation by setting it to "0" ("Low" level). Refer to Figure 21. Moreover, the HMCS44C has the automatic reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply. Refer to Figure 22. When the Built-in Reset Circuit is used, RESET should be connected to $V_{SS}$.

Internal state of the HMCS44C is specified as follows by the reset function.

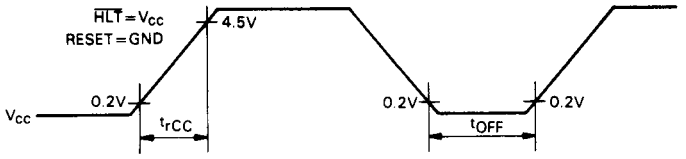
- Program Counter (PC) is set to address 3F on page 31 (31-3F).
- I/RI, I/RT, I/E and CF are reset to "0".
- IF0, IF1 and TF are set to "1".
- I/O latch and registers ($D_0$ to $D_{15}$, R0 to R6) are set to "1".

Note that other blocks (Status, Register, Timer/Counter, RAM, etc.) are not cleared.




- $t_{RST1}$ includes the time required from the power ON until the operation gets into the constant state.
- $t_{RST2}$ is applied when the operation is in the constant state.

Figure 21 RESET Timing




$t_{OFF}$ specifies the period when the power supply is OFF in the case that a short break of the power supply occurs and the power supply ON/OFF is repeated.

Figure 22 Power Supply Timing for Built-in Reset Circuit

## ■ HALT FUNCTION

When the $\overline{HLT}$ pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, etc.) are held. Because all internal logic operations stop in this state, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at ROM ordering.

"Enable"
- Output ..... The Status before the Halt State is held.
- Pull up MOS... ON
- Input..... No relation to "Halt"

Since Pull up MOS is ON, Pull up MOS current flows when output is "0" ("Low" level) in the Halt State (NMOS;ON). When an input signal changes, transmission current flows into an input circuit. Also, current flows into Pull up MOS. These currents are added to the Stand-by Supply Current (or Halt Current).

"Disable"
- Output ..... High Impedance (NMOS, PMOS: OFF)
- Pull up MOS... OFF
- Input..... Input Circuit: OFF

Both input and output are at high impedance state. Since an input circuit is OFF, only the Stand-by Supply Current (or Halt Current) flows even if an input signal changes.

When the $\overline{HLT}$ pin is set to "1" ("High" level), the HMCS-44C gets into operation from the status just before the Halt State. The halt timing is shown in Figure 23.

**CAUTION**

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

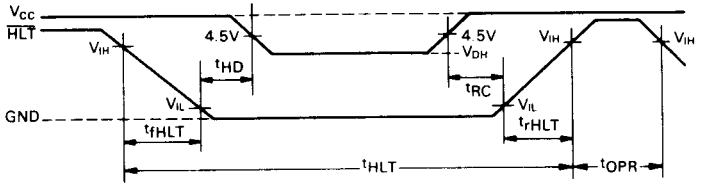



Figure 23 Halt Timing

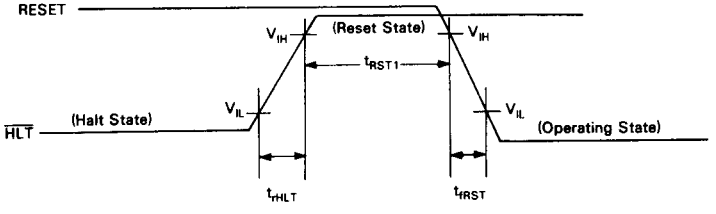



Figure 24 RESET Timing when Releasing Halt (Ceramic Filter Oscillation)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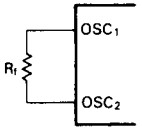
## ■ OSCILLATOR

The HMCS44C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor $R_f$ or ceramic filter circuit (Internal Clock Operation).

The $OSC_1$ clock frequency is internally divided by four to produce the internal system clocks.

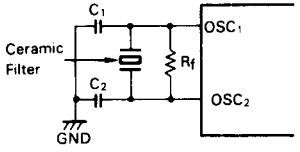
The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 25. There is no need of specifying it by using the mask option.

(a) Internal Clock Operation Using Resistor $R_f$

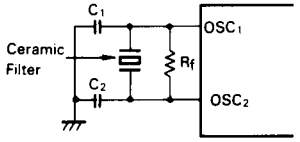



**Wiring of $OSC_1$ and $OSC_2$ pins should be as short as possible because the oscillation frequency is modified by capacitance of these pins.**

(b) Internal Clock Operation Using Ceramic Filter Circuit (Built-in CPG ; Ceramic Filter Oscillator)
(This is not applied to HMCS44CL.)



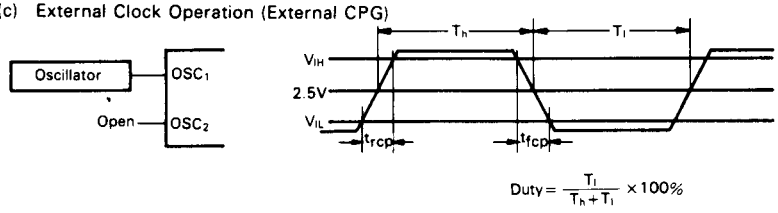

Ceramic Filter : CSB400P (MURATA)
$R_f$ : 1MΩ ± 10%
$C_1$ : 2200pF ± 10% (ceramic capacitor)
$C_2$ : 470pF ± 10% (ceramic capacitor)




Ceramic Filter : FCR-400K (TDK)
$R_f$ : 1MΩ ± 10%
$C_1$ : 1000pF ± 10% (ceramic capacitor)
$C_2$ : 1000pF ± 10% (ceramic capacitor)

**Reset at the time of Halt releasing.**
**This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.**

(c) External Clock Operation (External CPG)




$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 25 Clock Operation Mode

## ■ INSTRUCTION LIST

The instructions of the HMCS44C are listed according to their functions, as shown in Table 4.

Table 4 Instruction List

| Group | Mnemonic | Function | Status |
|---|---|---|---|
| Register · Register Instruction | LAB | B → A | |
| | LBA | A → B | |
| | LAY | Y → A | |
| | LASPX | SPX → A | |
| | LASPY | SPY → A | |
| | XAMR m | A ↔ MR (m) | |
| RAM Address Register Instruction | LXA | A → X | |
| | LYA | A → Y | |
| | LXI i | i → X | |
| | LYI i | i → Y | |
| | IY | Y+1 → Y | NZ |
| | DY | Y−1 → Y | NB |
| | AYY | Y+A → Y | C |
| | SYY | Y−A → Y | NB |
| | XSPX | X ↔ SPX | |
| | XSPY | Y ↔ SPY | |
| | XSPXY | X ↔ SPX, Y ↔ SPY | |
| RAM · Register Instruction | LAM (XY) | M → A (XY ↔ SPXY) | |
| | LBM (XY) | M → B (XY ↔ SPXY) | |
| | XMA (XY) | M ↔ A (XY ↔ SPXY) | |
| | XMB (XY) | M ↔ B (XY ↔ SPXY) | |
| | LMAIY (X) | A → M, Y+1 → Y (X ↔ SPX) | NZ |
| | LMADY (X) | A → M, Y−1 → Y (X ↔ SPX) | NB |
| Immediate Transfer Instruction | LMIIY i | i → M, Y+1 → Y | NZ |
| | LAI i | i → A | |
| | LBI i | i → B | |
| Arithmetic Instruction | AI i | A+i → A | C |
| | IB | B+1 → B | NZ |
| | DB | B−1 → B | NB |
| | AMC | M+A+C (F/F) → A | C |
| | SMC | M−A−$\overline{C}$ (F/F) → A | NB |
| | AM | M+A → A | C |
| | DAA | Decimal Adjustment (Addition) | |
| | DAS | Decimal Adjustment (Subtraction) | |
| | NEGA | $\overline{A}$+1 → A | |
| | COMB | $\overline{B}$ → B | |
| | SEC | "1" → C (F/F) | |
| | REC | "0" → C (F/F) | |
| | TC | Test C (F/F) | C (F/F) |
| | ROTL | Rotation Left | |
| | ROTR | Rotation Right | |
| | OR | A ∪ B → A | |

(to be continued)

| Group | Mnemonic | Function | Status |
|---|---|---|---|
| Compare Instruction | MNEI i | M ≠ i | NZ |
| | YNEI i | Y ≠ i | NZ |
| | ANEM | A ≠ M | NZ |
| | BNEM | B ≠ M | NZ |
| | ALEI i | A ≦ i | NB |
| | ALEM | A ≦ M | NB |
| | BLEM | B ≦ M | NB |
| RAM Bit Manipulation Instruction | SEM n | "1" → M (n) | |
| | REM n | "0" → M (n) | |
| | TM n | Test M (n) | M (n) |
| ROM Address Instruction | BR a | Branch on Status 1 | 1 |
| | CAL a | Subroutine Jump on Status 1 | 1 |
| | LPU u | Load Program Counter Upper on Status 1 | |
| | TBR p | Table Branch | |
| | RTN | Return from Subroutine | |
| Interrupt Instruction | SEIE | "1" → I/E | |
| | SEIF0 | "1" → IF0 | |
| | SEIF1 | "1" → IF1 | |
| | SETF | "1" → TF | |
| | SECF | "1" → CF | |
| | REIE | "0" → I/E | |
| | REIF0 | "0" → IF0 | |
| | REIF1 | "0" → IF1 | |
| | RETF | "0" → TF | |
| | RECF | "0" → CF | |
| | TI0 | Test $INT_0$ | $INT_0$ |
| | TI1 | Test $INT_1$ | $INT_1$ |
| | TIF0 | Test IF0 | IF0 |
| | TIF1 | Test IF1 | IF1 |
| | TTF | Test TF | TF |
| | LTI i | i → Timer/Counter | |
| | LTA | A → Timer/Counter | |
| | LAT | Timer/Counter → A | |
| | RTNI | Return Interrupt | |
| Input/Output Instruction | SED | "1" → D (Y) | |
| | RED | "0" → D (Y) | |
| | TD | Test D (Y) | D (Y) |
| | SEDD n | "1" → D (n) | |
| | REDD n | "0" → D (n) | |
| | LAR p | R(p) → A | |
| | LBR p | R(p) → B | |
| | LRA p | A → R(p) | |
| | LRB p | B → R(p) | |
| | P p | Pattern Generation | |
| | NOP | No Operation | |

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

| | | |
|---|---|---|
| Mnemonic only | | Instruction execution only |
| Mnemonic with X | | After instruction execution, X ↔ SPX |
| Mnemonic with Y | | After instruction execution, Y ↔ SPY |
| Mnemonic with XY | | After instruction execution, X ↔ SPX, Y ↔ SPY |
| [Example] | LAM | M → A |
| | LAMX | M → A, X ↔ SPX |
| | LAMY | M → A, Y ↔ SPY |
| | LAMXY | M → A, X ↔ SPX, Y ↔ SPY |

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ ..... ALU Not Zero
   - C ..... ALU Overflow in Addition, that is, Carry
   - NB ..... ALU Overflow in Subtraction, that is, No Borrow
   - Except above ..... Contents of the status column affects the Status F/F directly.
3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F.
   Instructions which affect the Carry F/F are eight as follows.

| | |
|---|---|
| AMC | SEC |
| SMC | REC |
| DAA | ROTL |
| DAS | ROTR |

4. All instructions except the pattern instruction (P) are executed in 1 cycle. The pattern instruction (P) is executed in 2 cycles.

**HMCS44C Mask Option List**

| |
|---|
| ☐ 5V Operation : HMCS44C |
| ☐ 3V Operation : HMCS44CL |

☆ Mark "✓" in "☐" for the selected spec.

| | |
|---|---|
| Date | |
| Customer | |
| Dept. | |
| Name | |
| ROM CODE ID | |
| LSI Type Name (entered by Hitachi) | |

(1) I/O Option

| Pin Name | I/O | I/O Option A | I/O Option B | I/O Option C | Remarks | Pin Name | I/O | I/O Option A | I/O Option B | I/O Option C | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_0$ | I/O | | | | | $R_{00}$ | I/O | | | | |
| $D_1$ | I/O | | | | | $R_{01}$ | I/O | | | | |
| $D_2$ | I/O | | | | | $R_{02}$ | I/O | | | | |
| $D_3$ | I/O | | | | | $R_{03}$ | I/O | | | | |
| $D_4$ | I/O | | | | | $R_{10}$ | I/O | | | | |
| $D_5$ | I/O | | | | | $R_{11}$ | I/O | | | | |
| $D_6$ | I/O | | | | | $R_{12}$ | I/O | | | | |
| $D_7$ | I/O | | | | | $R_{13}$ | I/O | | | | |
| $D_8$ | I/O | | | | | $R_{20}$ | I/O | | | | |
| $D_9$ | I/O | | | | | $R_{21}$ | I/O | | | | |
| $D_{10}$ | I/O | | | | | $R_{22}$ | I/O | | | | |
| $D_{11}$ | I/O | | | | | $R_{23}$ | I/O | | | | |
| $D_{12}$ | I/O | | | | | $R_{30}$ | I/O | | | | |
| $D_{13}$ | I/O | | | | | $R_{31}$ | I/O | | | | |
| $D_{14}$ | I/O | | | | | $R_{32}$ | I/O | | | | |
| $D_{15}$ | I/O | | | | | $R_{33}$ | I/O | | | | |
| $INT_0$ | I | | | | | | | | | | |
| $INT_1$ | I | | | | | | | | | | |

☆ Specify the I/O composition with a mark of "○" in the applicable composition column.
A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) I/O State at "Halt" mode

| I/O State |
|---|
| ☐ Enable |
| ☐ Disable |

☆ Mark "✓" in "☐" for the selected I/O state.

(3) Package

| Package |
|---|
| ☐ DP-42 |
| ☐ DP-42S |

☆ Mark "✓" in "☐" for the selected package.

**Check List of Application**

[A] Oscillator (CPG option)

| CPG | 5V Operation | 3V Operation |
|---|---|---|
| Resistor | ☐ $R_f = 91k\Omega \pm 2\%$ | ☐ $R_f = 180k\Omega \pm 2\%$ |
| Ceramic Filter | ☐ MURATA: CSB400P | |
| | ☐ TDK: FCR400K | |
| | ☐ Kyocera: KBR-400B | |
| External Clock | ☐ $f_{cp} = 200k$ to $440kHz$ | ☐ $f_{cp} = 130k$ to $240kHz$ |

☆ Mark "✓" in "☐" for the selected oscillator.

[B] Halt Function (Only when Ceramic Filter is selected in [A].)

| | Using Ceramic Filter |
|---|---|
| Halt Mode | ☐ Not used |
| | ☐ Used (Recovery with Reset) |

☆ Mark "✓" in "☐" for the selected spec.