



# HCF4027B

## DUAL J-K MASTER SLAVE FLIP-FLOP

- SET RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM-SPEED OPERATION - 16MHz (Typ. clock toggle rate at 10V)
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA}$  (MAX) AT  $V_{DD} = 18\text{V}$   $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

HCF4027B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input



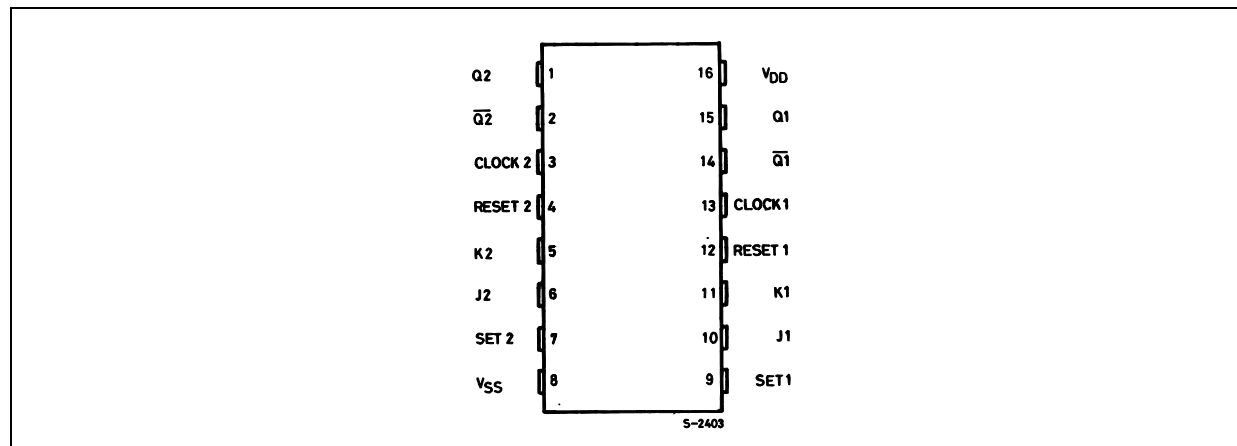
### ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4027BEY	
SOP	HCF4027BM1	HCF4027M013TR

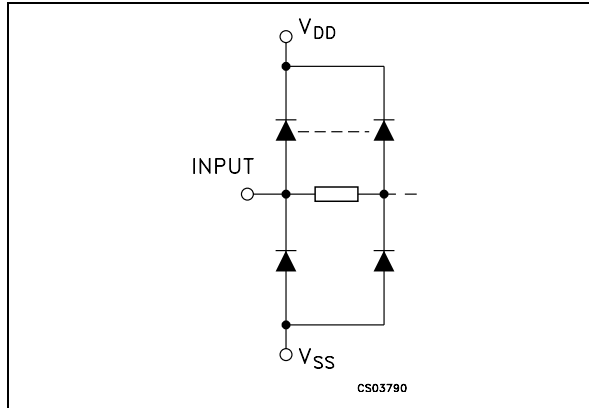
signals. Buffered Q and  $\bar{Q}$  signals are provided as outputs. This input-output arrangement provides for compatible operation with the HCF4013B dual D type flip-flop.

This device is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs, along with internal self-steering, control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and Reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

### PIN CONNECTION



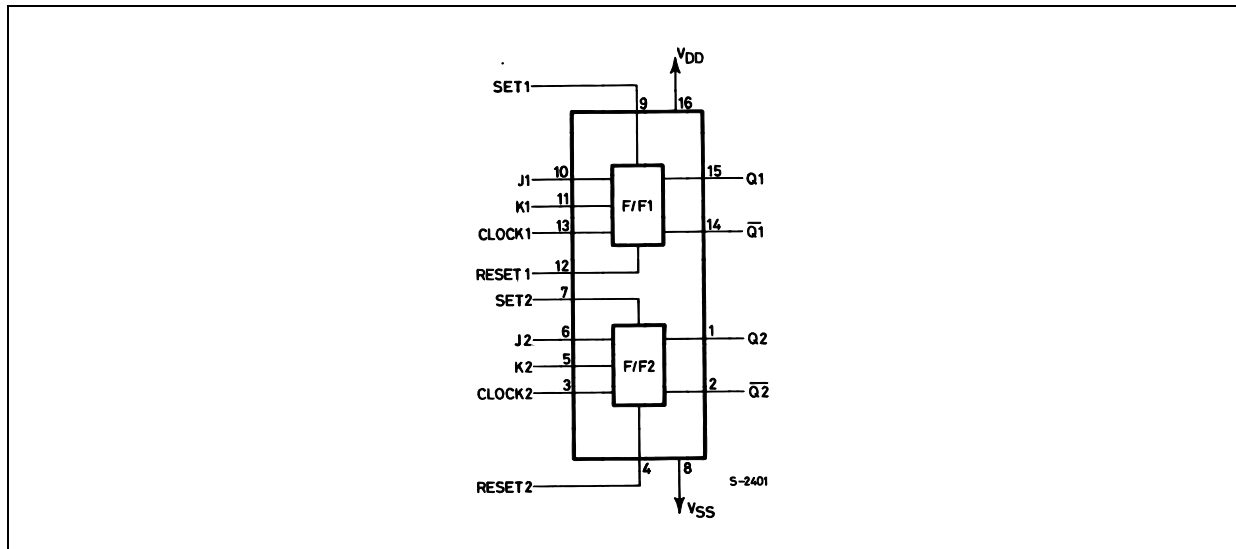
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
6, 5	J2, K2	Inputs
10,11	J1, K1	inputs
13, 3	CLOCK1, CLOCK2	Clock Inputs
12, 4	RESET1, RESET2	Reset Inputs
9, 7	SET1, SET2	Set Inputs
1, 2	Q2, Q2	Outputs
15, 14	Q1, Q1	Outputs
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

FUNCTIONAL DIAGRAM

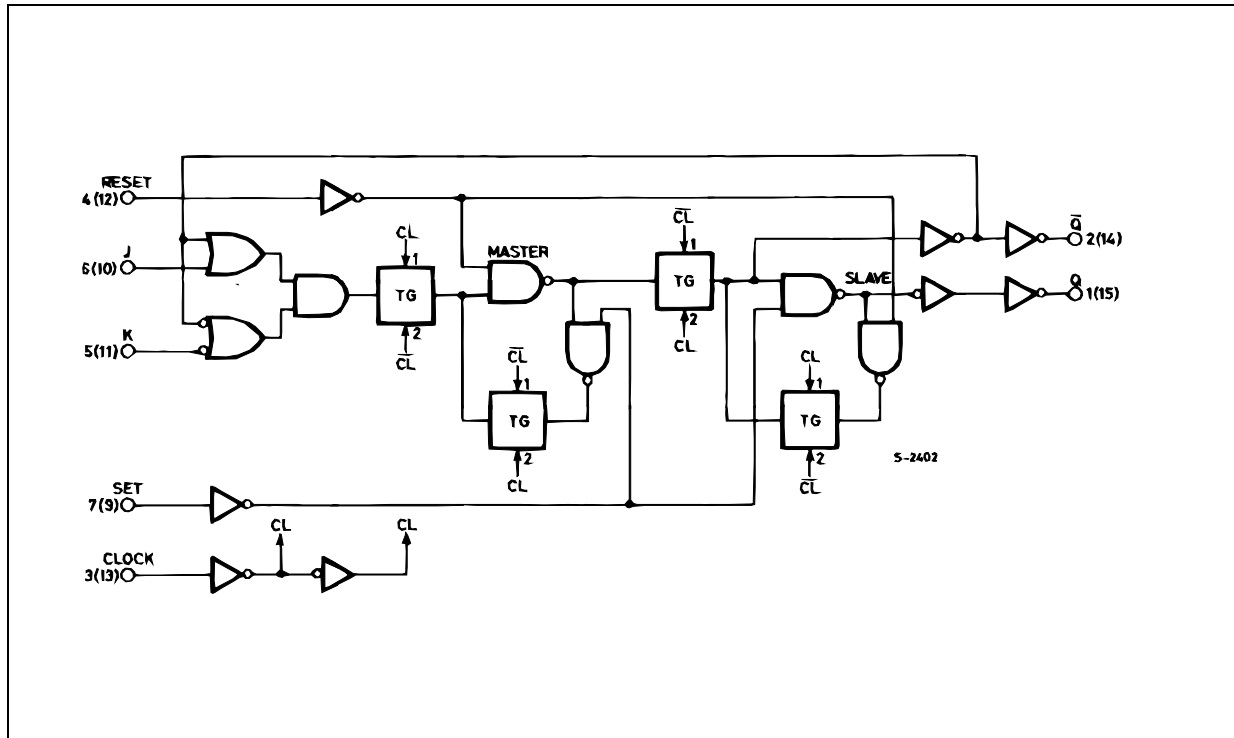


TRUTH TABLE

PRESENT STATE				Output	CLOCK*	NEXT STATE		
Inputs			Q			Q	Q-bar	
J	K	S	R	Q		Q	Q-bar	
H	X	L	L	L	⌋	H	L	
X	L	L	L	H	⌋	H	L	
L	X	L	L	L	⌋	L	H	
X	H	L	L	H	⌋	L	H	
X	X	L	L	X	⌋			NO CHANGE
X	X	H	L	X	X	H	L	
X	X	L	H	X	X	L	H	
X	X	H	H	X	X	H	H	

X : Don't Care  
 \* : Level Change

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}\text{C}$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.02	1		30		30	$\mu$ A
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{K}\Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (Clock to Q or $\bar{Q}$ Outputs)	5			150	300	ns
		10			65	130	
		15			45	90	
$t_{PLH}$	Propagation Delay Time (Set to Q or Reset to $\bar{Q}$ )	5			150	300	ns
		10			65	130	
		15			45	90	
$t_{PHL}$	Propagation Delay Time (Set to $\bar{Q}$ or Reset to Q)	5			200	400	ns
		10			85	170	
		15			60	120	
$t_{TLH}$ $t_{THL}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$t_W$	Pulse Width (Clock)	5		140	70		ns
		10		60	30		
		15		40	20		
$t_W$	Pulse Width (Set or Reset)	5		180	90		ns
		10		80	40		
		15		50	25		
$t_r$ , $t_f$	Clock input Rise or Fall Time	5				15	$\mu\text{s}$
		10				4	
		15				1	
$t_{setup}$	Setup Time (DATA)	5		200	100		ns
		10		75	35		
		15		50	25		
$f_{MAX}$	Maximum Clock Input Frequency <sup>(1)</sup> (toggle mode)	5		3.5	7		MHz
		10		8	16		
		15		12	24		

(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.(1) Input  $t_r$ ,  $t_f = 5\text{ ns}$

TEST CIRCUIT

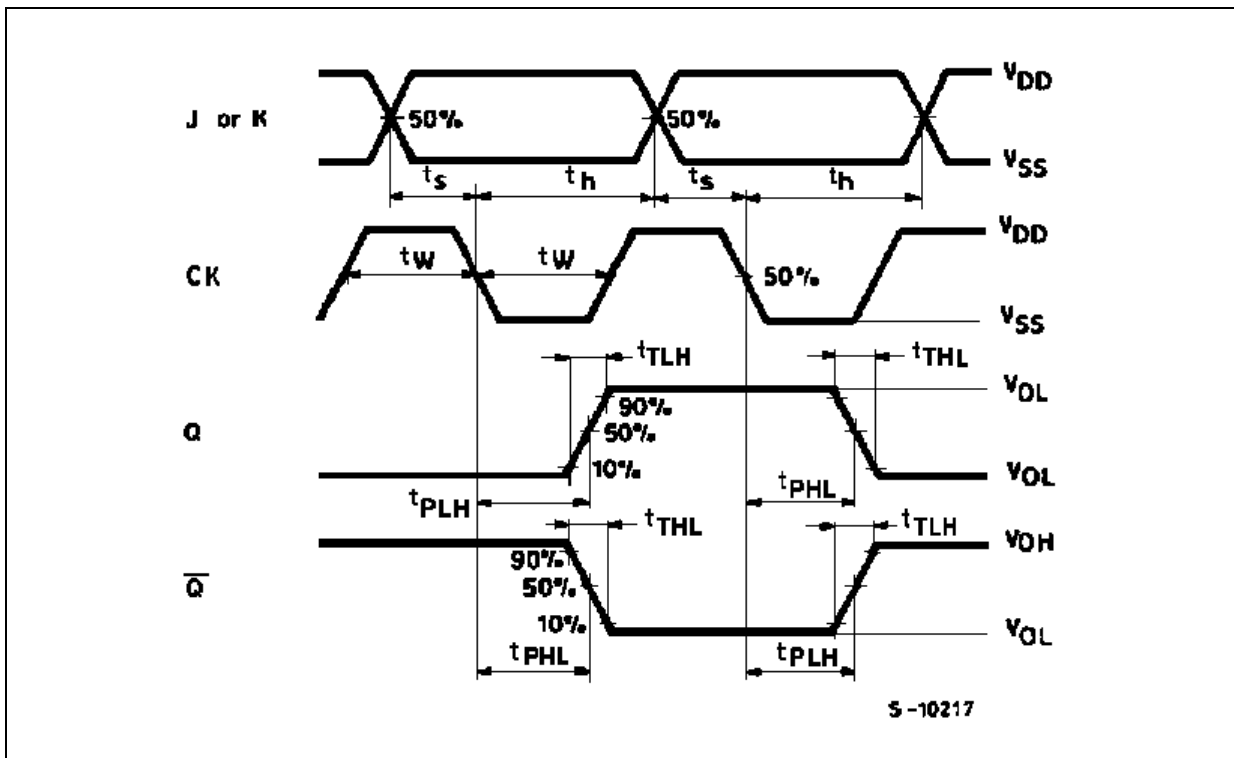


$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)

$R_L = 200\text{K}\Omega$

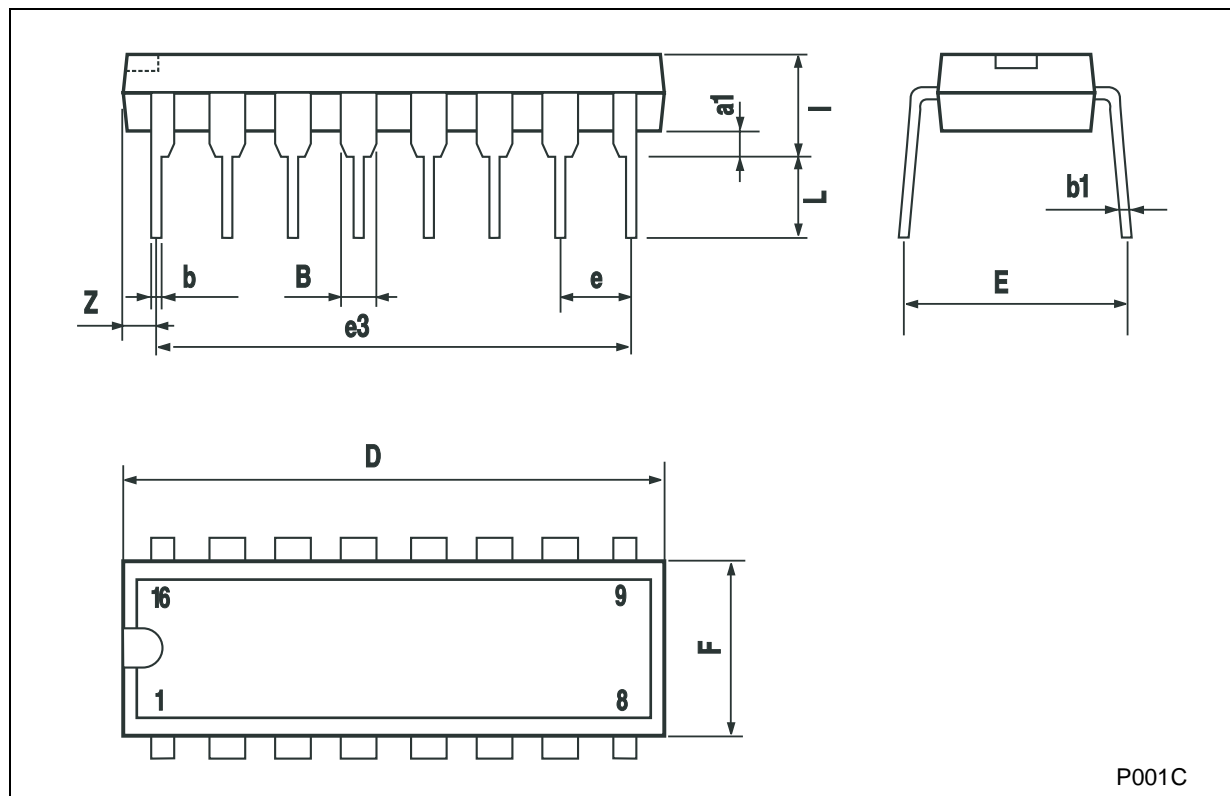
$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**WAVEFORM : PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (CK), SETUP AND HOLD TIME (J or K to CK) ( $f=1\text{MHz}$ ; 50% duty cycle)**



### Plastic DIP-16 (0.25) MECHANICAL DATA

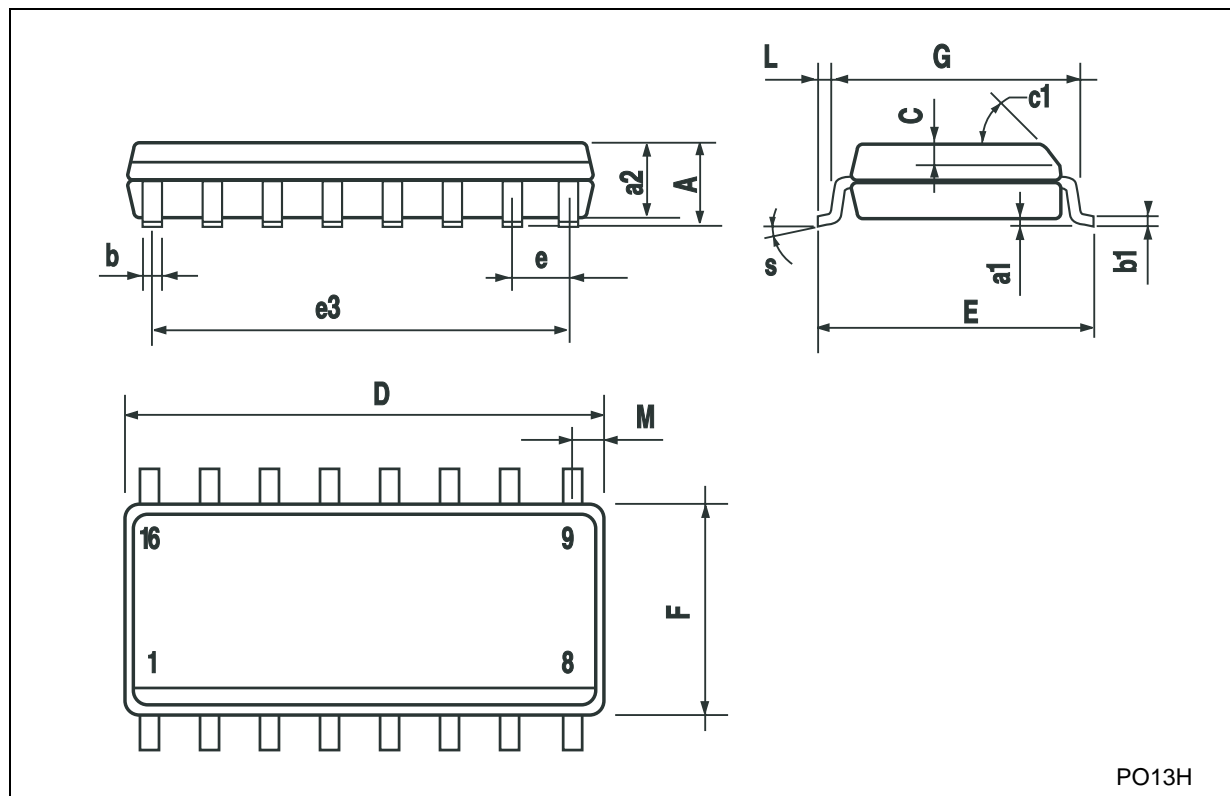
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

## SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>

