PROCESS CP323

Central™
Semiconductor Corp.

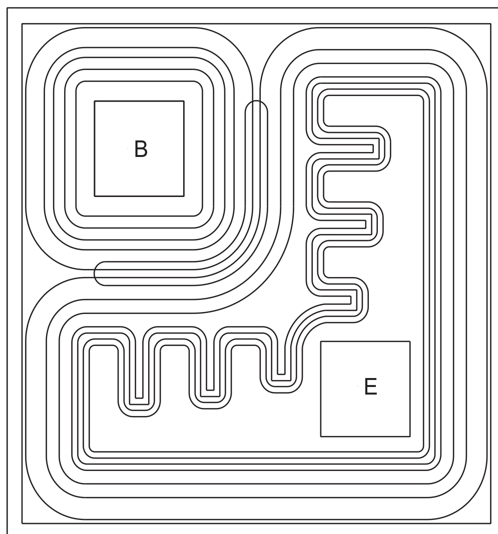
Small Signal Transistor

NPN - Darlington Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26.8 x 26.8 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	4.2 x 4.2 MILS
Emitter Bonding Pad Area	4.3 x 4.3 MILS
Top Side Metalization	Al -
Back Side Metalization	Au - 18,000Å

GEOMETRY



GROSS DIE PER 4 INCH WAFER
15,900

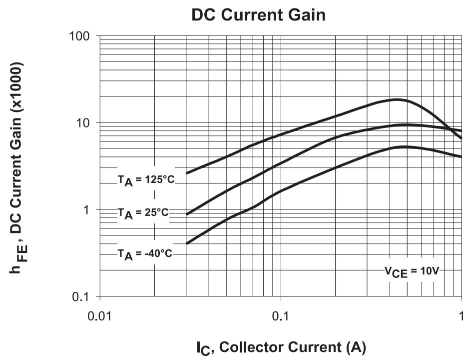
PRINCIPAL DEVICE TYPES
BSS52
BST52

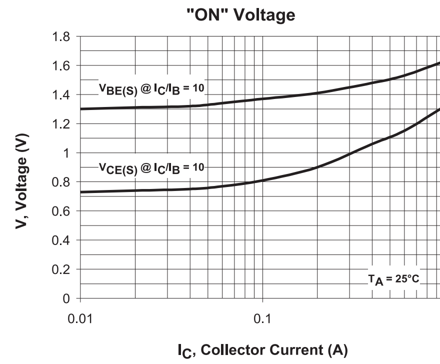
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

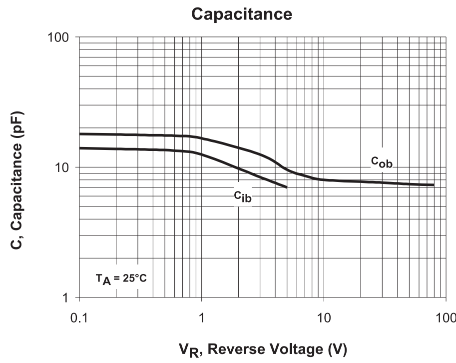
R1 (1-August 2002)

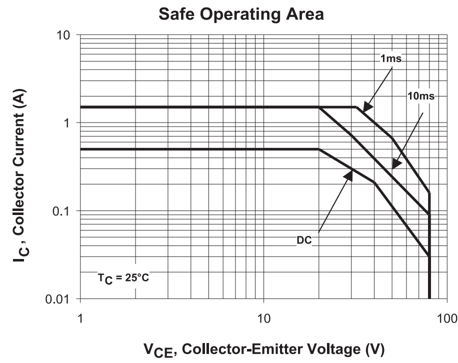
PROCESS CP323

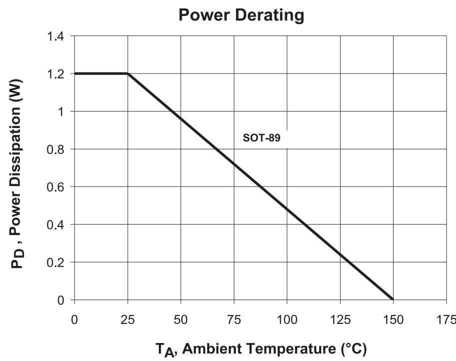
Typical Electrical Characteristics

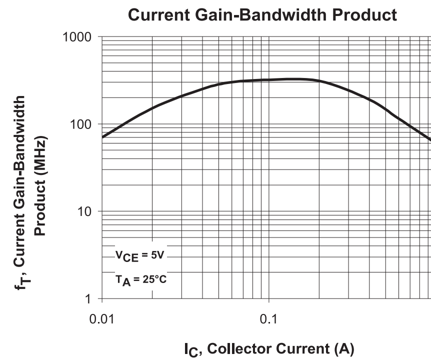












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