Am29821A – Am29826A

High-Performance Bus Interface Registers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - Noninverting CP-Y t_{PD} = 6 ns typical
  - Inverting CP-Y t_{PD} = 6 ns typical
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down. Outputs have Schottky clamp to ground
- I_{OL}: 48 mA Commercial, 32 mA Military
- Metastable "Hardened" Registers
- Higher speed, lower power versions of the Am29821 – 826.

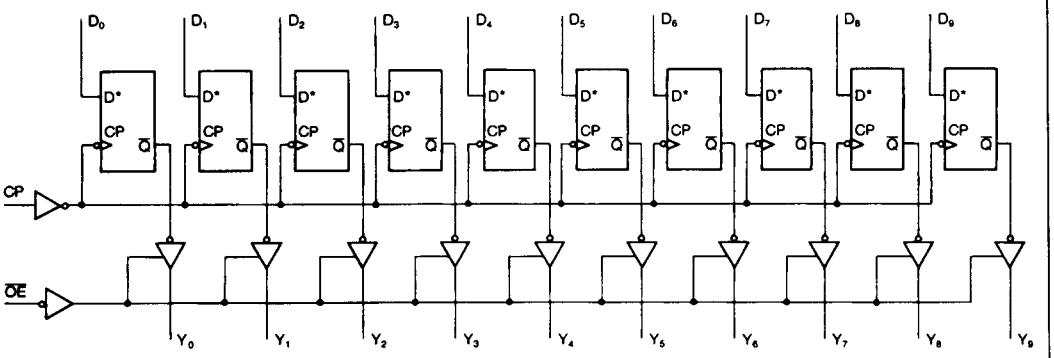
GENERAL DESCRIPTION

The Am29821A – 826A Series Bus Interface Registers are designed to eliminate the extra packages required to buffer existing registers, and provide extra data width for wider address/data paths or buses carrying parity. The Am29821A and Am29822A are buffered, 10-bit wide versions of the popular '374/'534 functions. The Am29823A and Am29824A are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The Am29825A and Am29826A are 8-bit buffered registers with all the 9-bit controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800A high-performance interface family are designed for high-capacitance load drive capability.

BLOCK DIAGRAM

Am29821A/Am29822A*



BD005500

D* = D for the Am29821A, $\overline{D}$ for the Am29822A

PRODUCT SELECTOR GUIDE

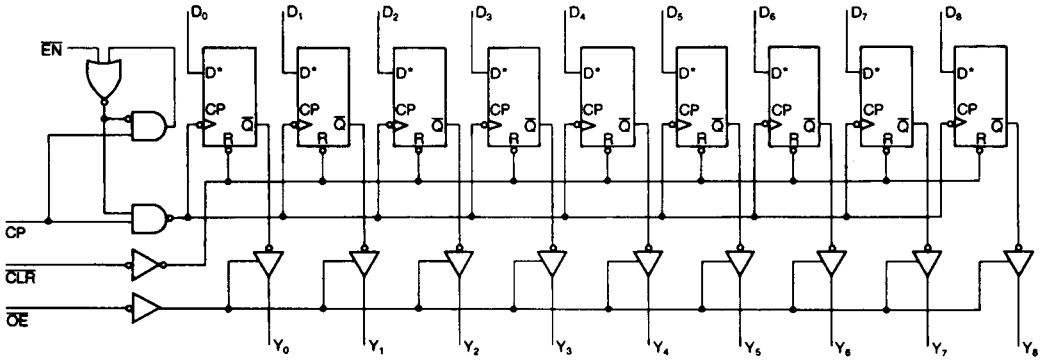
	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29821A	Am29823A	Am29825A
Inverting	Am29822A	Am29824A	Am29826A

*See following page for additional Block Diagrams.

Order #07138A

BLOCK DIAGRAMS (Cont.)

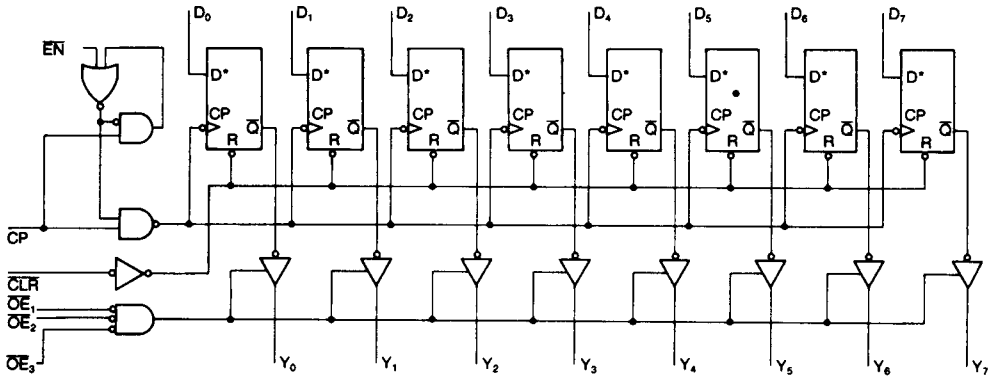
Am29823A/Am29824A



BD005510

D* = D for the Am29823A, $\overline{D}$ for the Am29824A

Am29825A/Am29826A



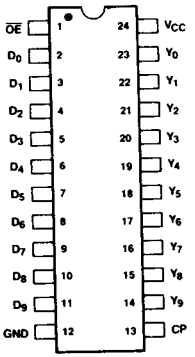
BD005520

D* = D for the Am29825A, $\overline{D}$ for the Am29826A

CONNECTION DIAGRAMS
Top View

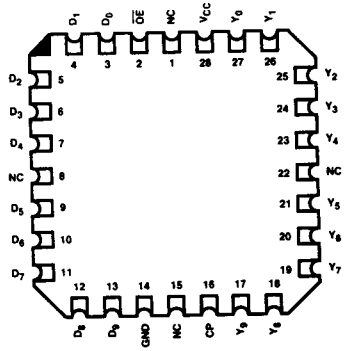
Am29821A/Am29822A

DIPs



CD001360

LCC*

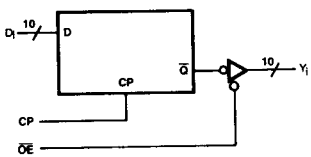


CD001370

*Same pinouts apply for PLCC

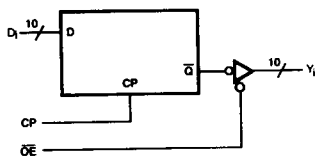
LOGIC SYMBOLS

Am29821A



LS000453

Am29822A



LS000452

FUNCTION TABLE

Inputs			Am29821A		Am29822A		
			Internal	Outputs	Internal	Outputs	
$\overline{OE}$	D_I	CP	$\overline{Q}_I$	Y_I	$\overline{Q}_I$	Y_I	Function
H	L	↑	H	Z	L	Z	Hi-Z
H	H	↑	L	Z	H	Z	
H	X	X	NC	Z	NC	Z	Hold
L	X	X	NC	NC	NC	NC	
L	L	↑	H	L	L	H	Load
L	H	↑	L	H	H	L	

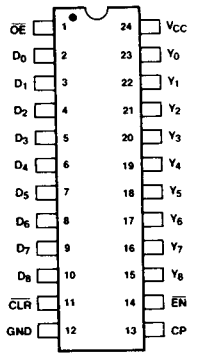
H = HIGH
L = LOW
X = HIGH or LOW

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

CONNECTION DIAGRAMS
Top View

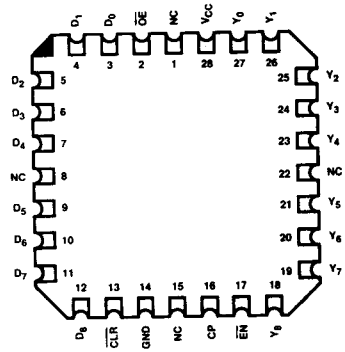
Am29823A/Am29824A

DIPs



CD001220

LCC*

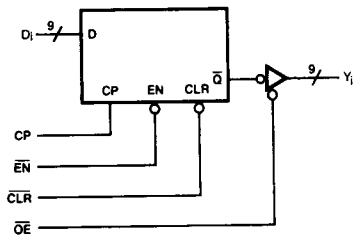


CD001230

*Same pinouts apply for PLCC

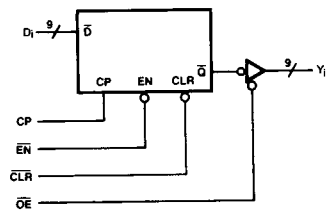
LOGIC SYMBOLS

Am29823A



LS000432

Am29824A



LS000431

FUNCTION TABLE

Inputs					Am29823A		Am29824A		
					Internal	Outputs	Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i	$\overline{Q}_i$	Y_i	Function
H	H	L	L	↑	H	Z	L	Z	Hi-Z
H	H	L	H	↑	L	Z	H	Z	
H	L	X	X	X	H	Z	H	Z	Clear
L	L	X	X	X	H	L	H	L	
H	H	H	X	X	NC	Z	NC	Z	Hold
L	H	H	X	X	NC	NC	NC	NC	
H	H	L	L	↑	H	Z	L	Z	Load
H	H	L	H	↑	L	Z	H	Z	
L	H	L	L	↑	H	L	L	H	
L	H	L	H	↑	L	H	H	L	

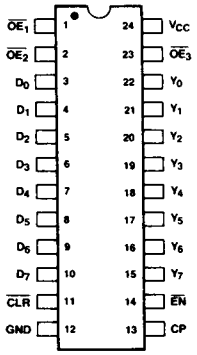
H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

CONNECTION DIAGRAMS
Top View

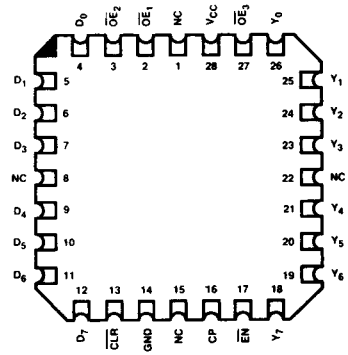
Am29825A/Am29826A

DIPs



CD001200

LCC*

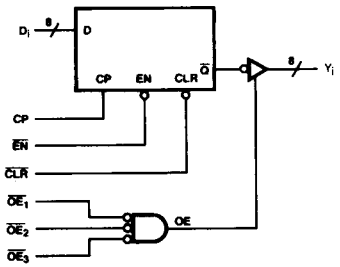


CD001210

*Same pinouts apply for PLCC

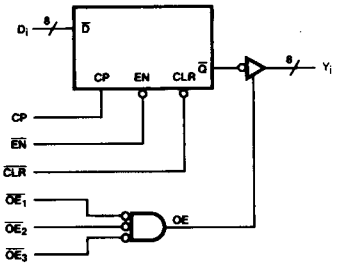
LOGIC SYMBOLS

Am29825A



LS000422

Am29826A



LS000421

FUNCTION TABLE

					Am29825A		Am29826A		
	Inputs				Internal	Outputs	Internal	Outputs	
OE*	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i	$\overline{Q}_i$	Y_i	Function
L L	H H	L L	L H	↑ ↑	H L	Z Z	L H	Z Z	Hi-Z
L H	L L	X X	X X	X X	H H	Z L	H H	Z L	Clear
L H	H H	H H	X X	X X	NC NC	Z NC	NC NC	Z NC	Hold
L L H H	H H H H	L L L L	L H L H	↑ ↑ ↑ ↑	H L H L	Z Z L H	L H L H	Z Z H L	Load

H = HIGH
L = LOW
X = Don't Care

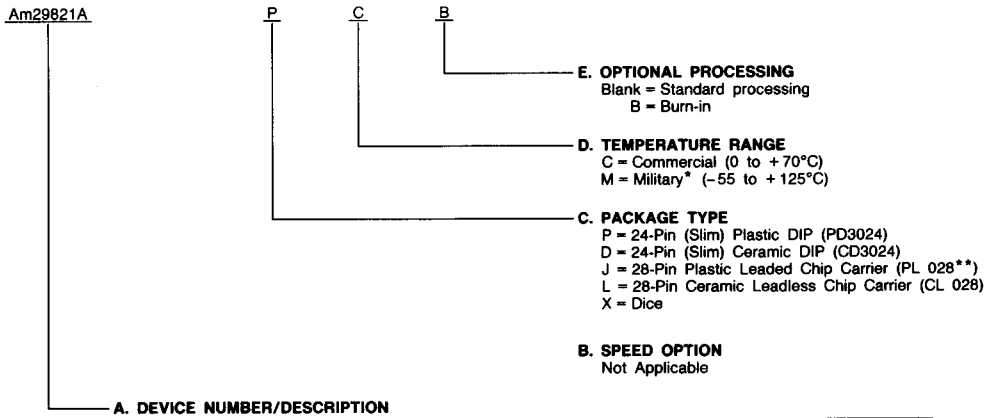
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

*OE is an Active HIGH internal signal produced as follows:

$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

ORDERING INFORMATION
AMD STANDARD PRODUCTS

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
Am29821A – 826A	PC, PCB, DC, DCB, DM, DMB, JC**, JCB**, LC, LCB, LM, LMB, XC, XM

* Military or Limited Military temperature range products are "NPL" (Non-Compliant Product List), or Non-MIL-STD-883C Compliant products only.

** Preliminary. Subject to Change.

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

D_i Data Input (Input)
D_i are the flip-flop data inputs.

Y_i Data Outputs (Output)
Y_i are the three-state data outputs.

CP Clock Pulse (Input, LOW-to-HIGH Transition)
Clock Pulse is the clock input for the registers. Data is entered into the registers on LOW-to-HIGH transitions.

Am29821A/Am29822A Only

$\overline{OE}$ Output Enable (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is transferred to the Y_i outputs.

Am29823A/Am29824A Only

$\overline{EN}$ Clock Enable (Input, Active LOW)
When the $\overline{EN}$ input is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of data or clock input transitions.

$\overline{CLR}$ Clear (Input, Active LOW)
When the $\overline{CLR}$ input is LOW and $\overline{OE}$ is LOW, the Y_i outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.

$\overline{OE}$ Output Enable (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are put in the high-impedance state. When $\overline{OE}$ is LOW, the register data is passed to the Y_i outputs.

Am29825A/Am29826A Only

$\overline{EN}$ Clock Enable (Input, Active LOW)
When the $\overline{EN}$ input is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of data or clock input transitions.

$\overline{CLR}$ Clear (Input, Active LOW)
When the $\overline{CLR}$ input is LOW and all $\overline{OE}_i$ inputs are LOW, the Y_i outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.

$\overline{OE}$ Output Enables (Input, Active LOW)
When $\overline{OE}_1$, $\overline{OE}_2$, and $\overline{OE}_3$ are all LOW, register data is passed to the Y_i outputs. If any or all $\overline{OE}_i$ are HIGH, the Y_i outputs are put in a high-impedance state.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to 5.5 V
DC Input Voltage ..... −0.5 V to +5.5 V
DC Output Current, into Outputs ..... 100 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15$ mA	2.4		Volts
			$I_{OH} = -24$ mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	MIL, I_{OL} = 32 mA		0.5	Volts
			COM'L, I_{OL} = 48 mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., $I_{IN} = -18$ mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−500	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V			100	μA
I_{OZL}	Output Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4 V		−50	μA
I_{OZH}			V_O = 2.7 V		50	
I_{SC}	Output Short Circuit Current (Note 1)	V_{CC} = Max., V_{OUT} = 0 V		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	μA
I_{CC}	Supply Current (Note 2)	V_{CC} = Max. Outputs Open $\overline{EN}$ = LOW	Over Temperature Range		110	mA
			+70°C			
			+125°C			

Notes: 1. Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.
2. Clock input, CP, is HIGH after clocking in data to produce outputs = LOW.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	3.5	7.5	3.5	9.0	ns
t_{PLH}			3.5	10.5	3.5	11.5	ns
t_S	Data to $\overline{CP}$ Setup Time		4		4		ns
t_H	Data to $\overline{CP}$ Hold Time		2		2		ns
t_S	Enable ($\overline{EN}$ ⌝⌞) to CP Setup Time		4		4		ns
t_S	Enable ($\overline{EN}$ ⌟⌜) to CP Setup Time		4		4		ns
t_H	Enable ($\overline{EN}$) Hold Time		0		0		ns
t_{PHL}	Propagation Delay, Clear to Y_i			15		15	
t_S	Clear ($\overline{CLR}$ ⌟⌜) to CP Setup Time		7		7		ns
t_{PWH}	Clock Pulse Width HIGH		7		7		ns
t_{PWL}	Clock Pulse Width LOW		7		7		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width		7		7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌝⌞ to Y_i			10		10	ns
t_{ZL}				10		10	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌟⌜ to Y_i			8		10	ns
t_{LZ}				8		10	ns

*See Test Circuit and Waveforms.