AKD4394
Evaluation board Rev.C for AK4394

General Description

The AKD4394 is an evaluation board for AK4394, which is 192kHz sampling 24Bit ΔΣ DAC. The AKD4394 includes a LPF which can add differential analog outputs from the AK4394 and also has a digital interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it is easy to evaluate the AK4394.

■ **Ordering Guide**

AKD4394 Rev.C --- Evaluation board Rev.C for AK4394: differential output

Function

■ On-board differential output buffer circuit

■ On-board clock generator

■ BNC connector for an external clock input

■ Compatible with 3types of interface

1. Direct interface with evaluation boards for AKM's A/D converter (AKD539X, AKD535X)
2. Interface with a signal generator (AKD43XX)
3. On-board CS8414 as DIR which accepts optical input.

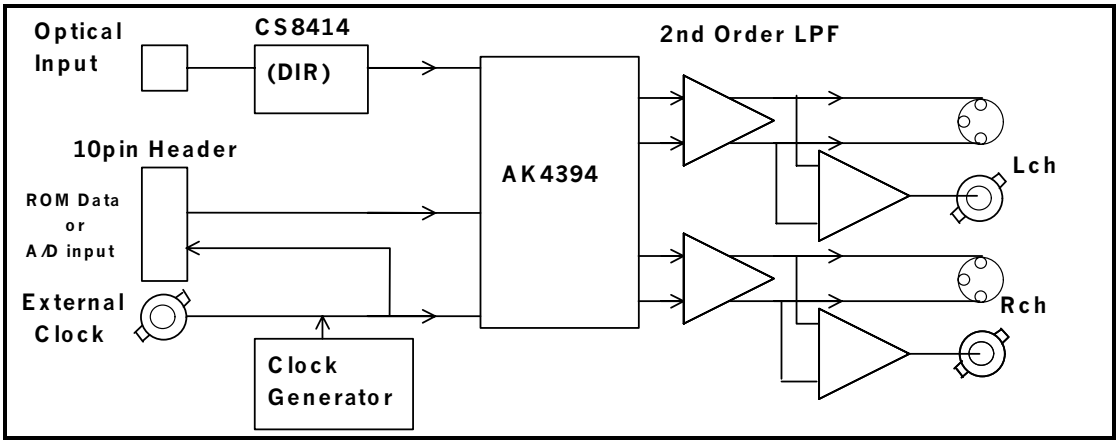


Fig.1 Block diagram

* Circuit diagram and PCB layout are attached at the end of this manual.
(AKD4394 Rev.C is same as AKD4393 Rev.C.)

■ External Analog Circuit (Rev.C)

The differential output circuit and LPF is implemented on board. The differential outputs of AK4394 is buffered by non-inverted circuit and output via Cannon connector(differential output). LPF adds differential outputs. NJM5534D is used for op-amp on this board that has low noise and high voltage torelance characteristics. Analog signal is output via Cannon and BNC connectors on the board. The output level is about 2.94Vrms(typ@VREF=5.0V) by Cannon and 2Vrms(typ@VREF=5.0V) by BNC.

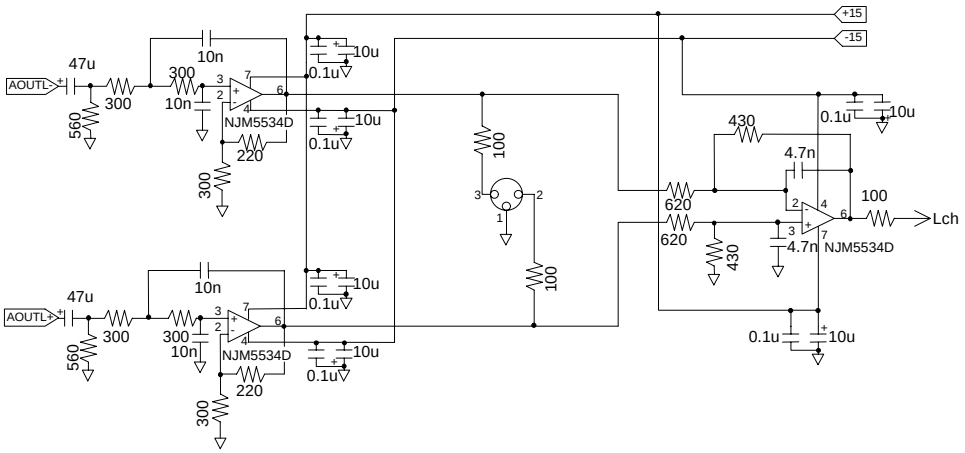


Fig.2 External Analog Filter

■ Operation sequence

1. Set up the jumpers for power supply.

[JP15(REG)] selects power supply for AVDD pin of AK4394.

short: 5V is supplied from regulator. (default)
Nothing should be connected to A5V jack.

open: 5V is supplied from A5V.

2. Set up the power supply lines.

+15V=15V, -15V=-15V: Power supply for op-amp. AVDD of AK4394 is supplied from "+15V" through regulator (JP15: short).

A5V=5V: This jack is used when AVDD of AK4394 is supplied from this. In this case, JP15 should be open.

DVDD=5V: Power supply for logic circuit on this board.

VP=3V~5.25V: Digital (set JP10 to VP),

AGND=DGND=0V .

Each supply line should be distributed from the power unit.

3. Set up the evaluation modes by jumper pins and DIP switches.(See next item.)
4. Power on.(The AK4394 should be reset once by bringing PD "L" upon power-up.)

*SW1 resets the AK4394 during operation.

The AK4394 is reset at SW1="L" and exits resetting at SW1="H".

■ The evaluation modes and corresponding jumper pins setting

1. Evaluation Modes

•Applicable Evaluation Mode

(1) DIR(Optical Link)
(2) Ideal sine wave generated by ROM data
(3) Using AD converted data
(4)All interface signals including master clock are fed externally.

(1) DIR(Optical Link) (default)

PORT2 is used for the evaluation using such as CD test disk. The DIR generates MCLK, BICK and LRCK SDATAfrom the received data through optical connector(PORT2: TORX176).

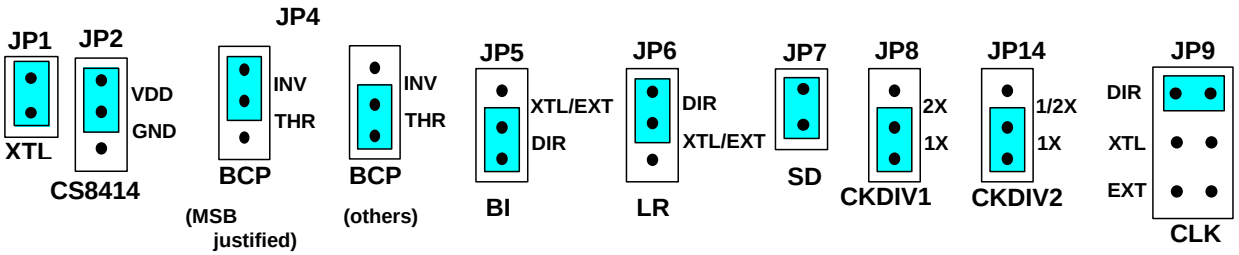


Fig.3 Jumper set-up (DIR)

(2) Ideal sine wave generated by ROM data

Digital signal generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4394 to AKD43XX then LRCK, BICK and SDATA are sent from AKD43XX to AKD4394.

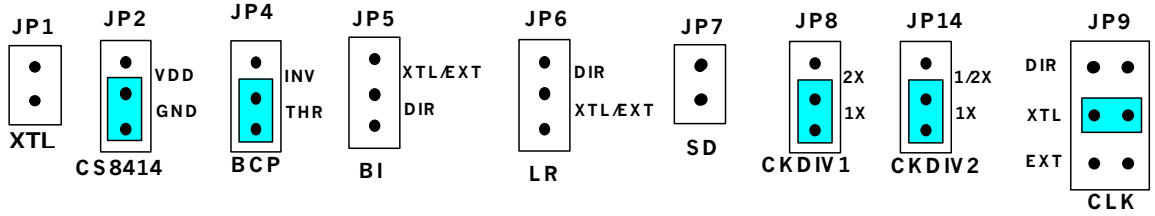


Fig.4 Jumper set-up (ROM data)

(3) Using AD converted data

AD converted data from AKM's AD evaluation boards(AKD539X, AKD535X) is used through PORT1.

* In case of using external clock through a BNC connector, select EXT of JP9 and short JP1.

* In case of using the double speed sampling mode, select 1/2X of JP8 and set S2-2(DFS) on.

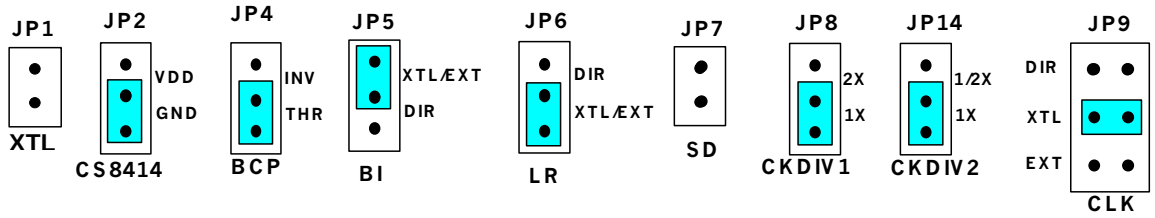


Fig.5 Jumper set-up (A/D)

(4) All interface signals including master clock are fed externally.

Under the following set-up, MCLK, LRCK and SCLK signals needed for the D/A to operate could be fed through PORT1.

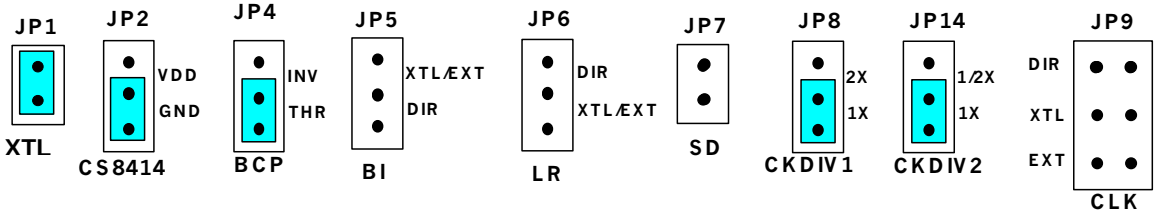


Fig.6 Jumper set-up (ext.)

2. MCLK set-up

When the LRCK is fed from the 74HC4040 on the board, The ratio of MCLK to LRCK can be selected by JP8 and JP14.

JP14	JP8	X'tal	MCLK	fs	MCLK/LRCK
1X	1X	12.288MHz	12.288MHz	48kHz	256
1X	2X	24.576MHz	24.576MHz	48kHz	512
1/2X	1X	24.576MHz	12.288MHz	96kHz	128
1/2X	2X	49.152MHz	12.288MHz	96kHz	128

Table.1 set-up example

3. BICK set-up

When BICK is supplied from U1(74HC4040), either 32fs or 64fs could be selected. Fig.8 shows 64fs mode. 64fs mode is recommended.

*Only mode 0(LSB justified 16bit mode) can correspond to 32fs.

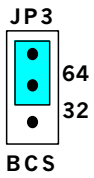


Fig.7 Jumper Set-up (BCS)

4. DIP switch set-up

Confirm the set-up of the DIP switch before the operation. “ON” means “H” and “OFF” means “L”.

4-1. Set-up of SW3, SW4(Mode set-up of AK4394: see the data sheet of AK4394)

DIF2	DIF1	DIF0	Mode	BICK	
OFF	OFF	OFF	0: LSB justified, 16bit	≥32fs	
OFF	OFF	ON	1: LSB justified, 20bit	≥40fs	
OFF	ON	OFF	2: LSB justified, 24bit	≥48fs	
OFF	ON	ON	3: I^2S	≥48fs	(default)
ON	OFF	OFF	4: MSB justified, 24bit	≥48fs	

Table 2 Audio Serial Interface Format Select Pins (SW3-5,6,7)

4-2. Set-up of SW6 (Mode set-up of CS8414. About details, see the data-sheet of CS8414)

Adjust the audio data format of CS8414 (DIR) to AK4394. CS8414 does not match the LSB justified 20bit/24bit mode of AK4394.

M3 (SW6-2)	M2 (SW6-3)	M1 (SW6-4)	M0 (SW6-5)	Data format	JP4	
OFF	OFF	OFF	OFF	MSB justified, 24bit	INV	
OFF	OFF	ON	OFF	I^2S	THR	(default)
OFF	ON	OFF	ON	LSB justified, 16bit	THR	

Table 3 Set-up of SW6

SW6-1(SEL) :Usually ON.

SW6-6(CS12): Select the channel for indicating the channel status.

ON: Rch (default), OFF: Lch

5. Parallel/Serial Control

SW5: set up P/S pin of AK4394.

H: parallel mode. PORT3 is used JP11, 12 and 13 should be open.

L: serial mode. PORT3 is used. JP11, 12 and 13 should be open.

6. Other set-up

SW1: Reset of AK4394. Select "H" during operation.

SW2: Soft-mute of AK4394. The soft-mute is executed during SW2 pushed.

LE1 : This LED shows pre-emphasis status. It turns on when the data is pre-emphasized.

LE2 : This LED shows the output of VERF pin in CS8414. It turns on when the error is occured in CS8414.

■ AK4394 Measurement Example

Conditions:

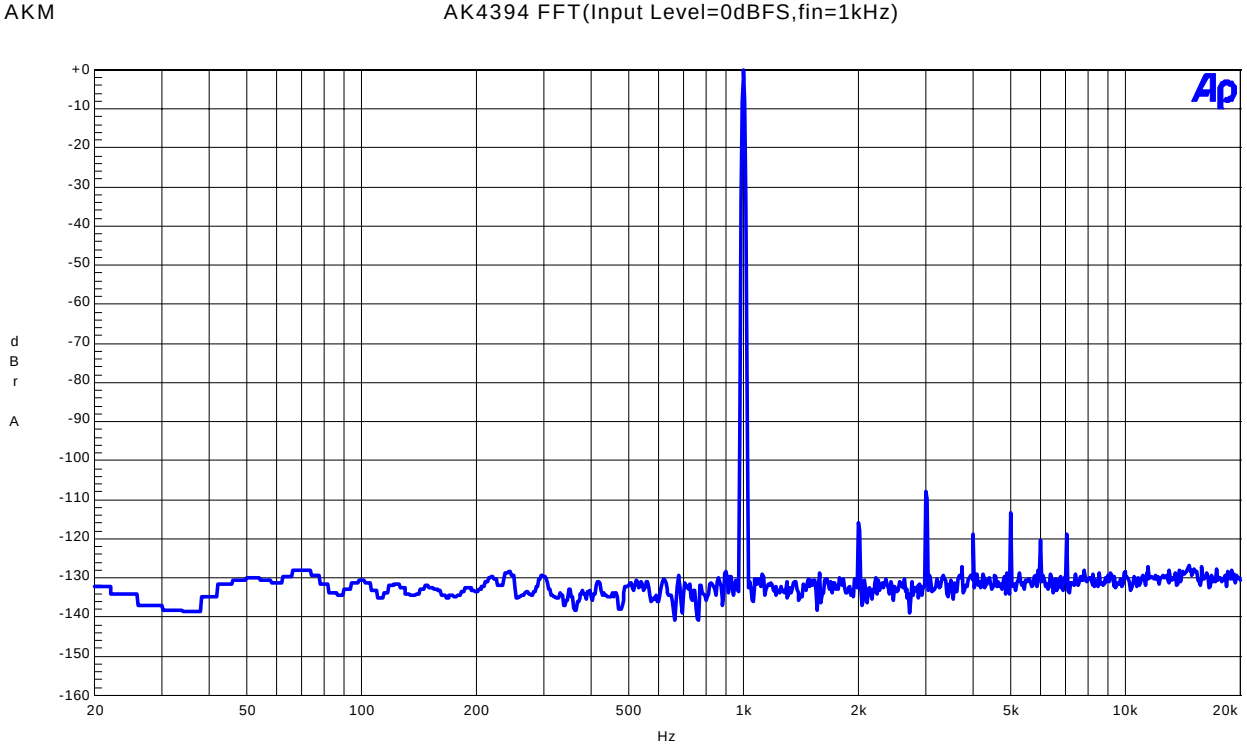
AVDD =DVDD= 5.0V
Interface = DIR (44.1kHz, 96kHz)
MCLK = 256fs(fs=44.1kHz, 96kHz)
BICK = 64fs
fs = 44.1kHz, 96kHz,
Input data = 24bit
Measurement unit: Audio Precision System Two Cascade (fs=44.1kHz, 96kHz)

(AKD4394 Rev.C: differential output)

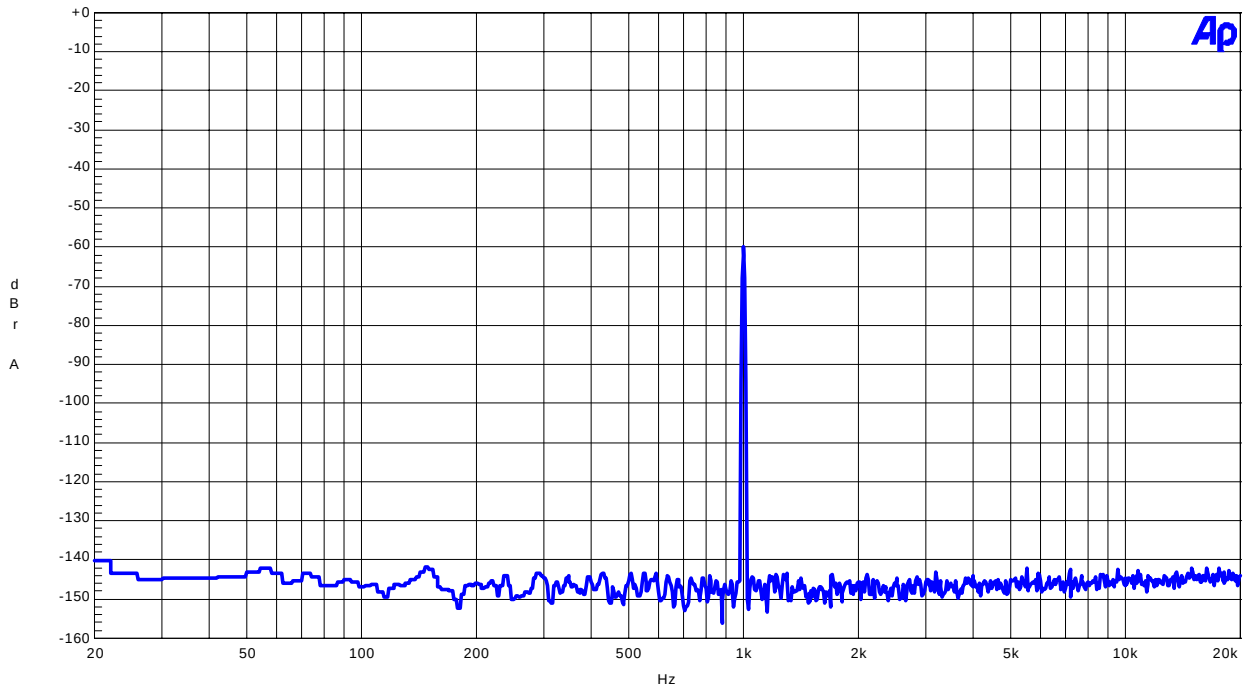
fs		Result	
44.1kHz	THD+N	100.3	20kLPF
	DR	120.1	22kLPF + A-weighted
	S/N	120.2	22kLPF + A-weighted
96kHz	THD+N	99.6	40kLPF
	DR	119.2	80kLPF + A-weighted
	S/N	119.8	80kLPF + A-weighted

Plot:
FFT Point: 16384
Window: Equiripple
Averages: 4

(fs=44.1kHz)



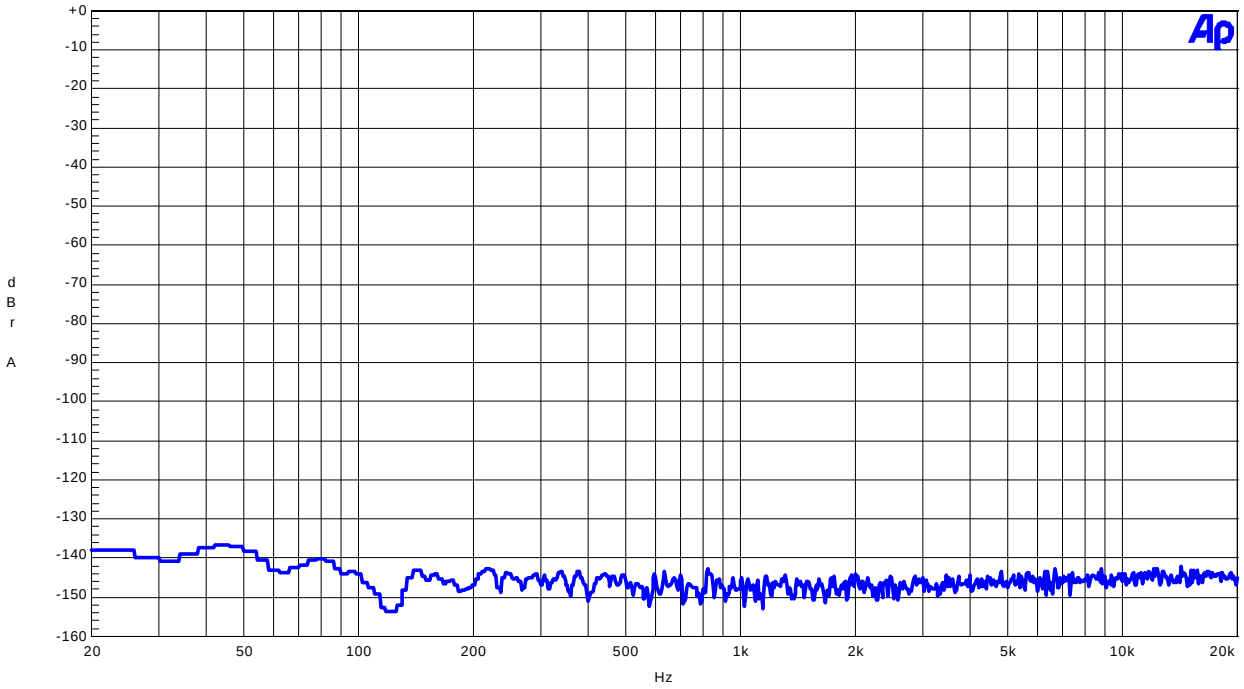
FFT (Input Level=0dBFS, fin=1kHz)



FFT (Input Level=-60dBFS, fin=1kHz)

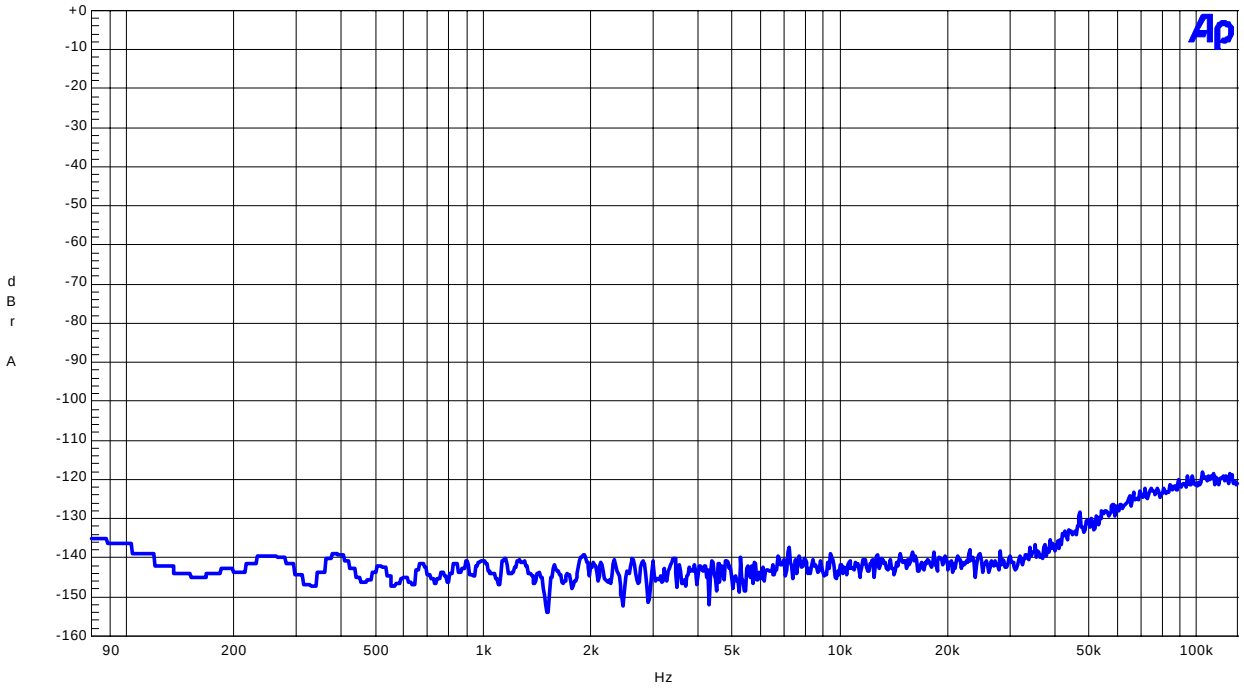
(fs=44.1kHz)

AKM AK4394 FFT(Input="0"data)



FFT (noise floor)

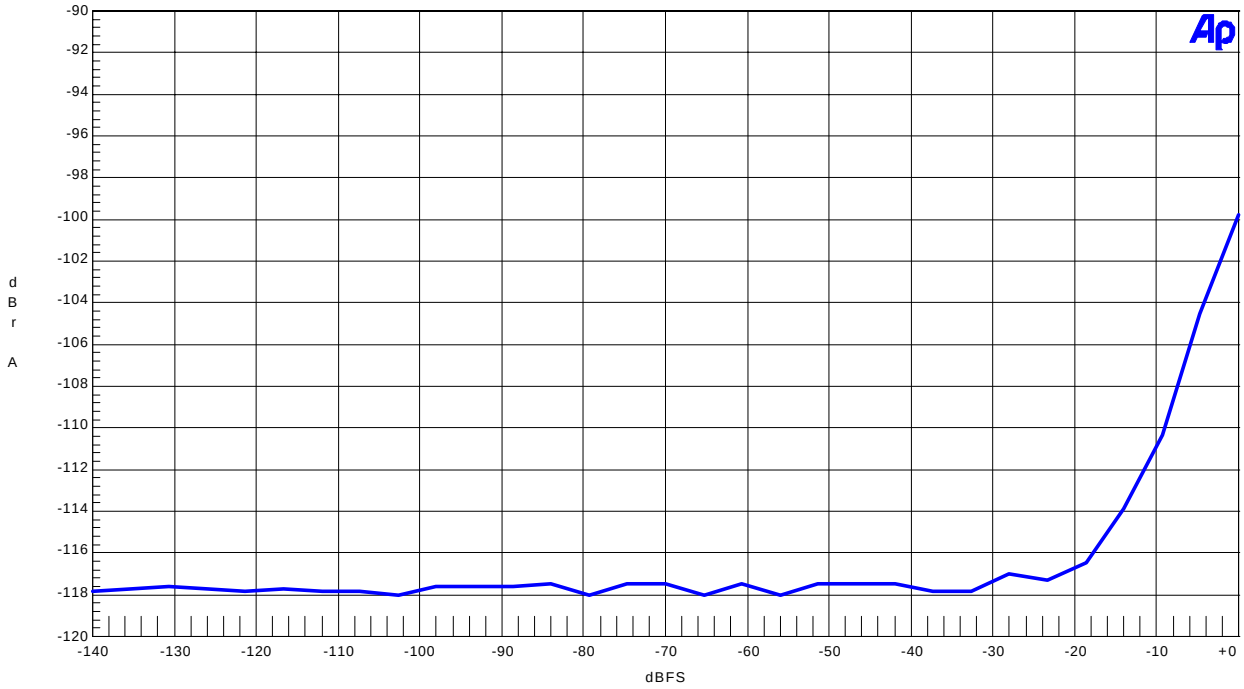
AKM AK4394 FFT(Input = "0"data, out-of band)



FFT (noise floor, out-of band)

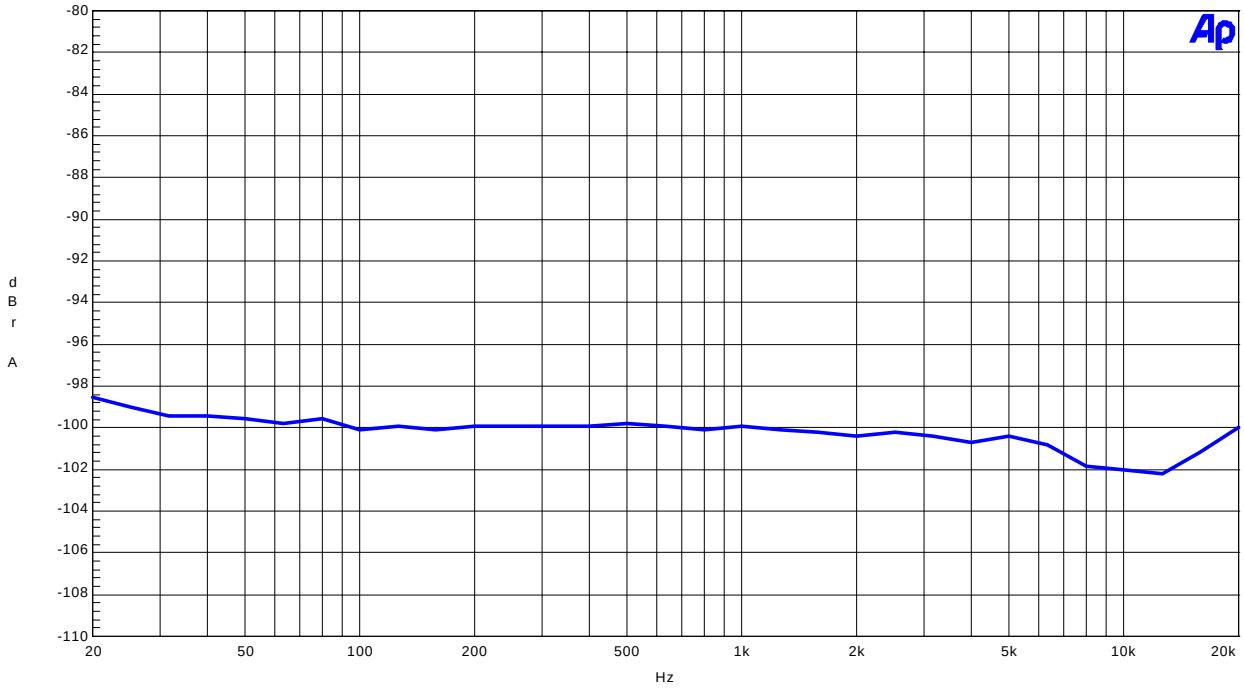
(fs=44.1kHz)

AKM AK4394 THD + N vs Amplitude(fin=1kHz)



THD + N vs Amplitude (fin=1kHz)

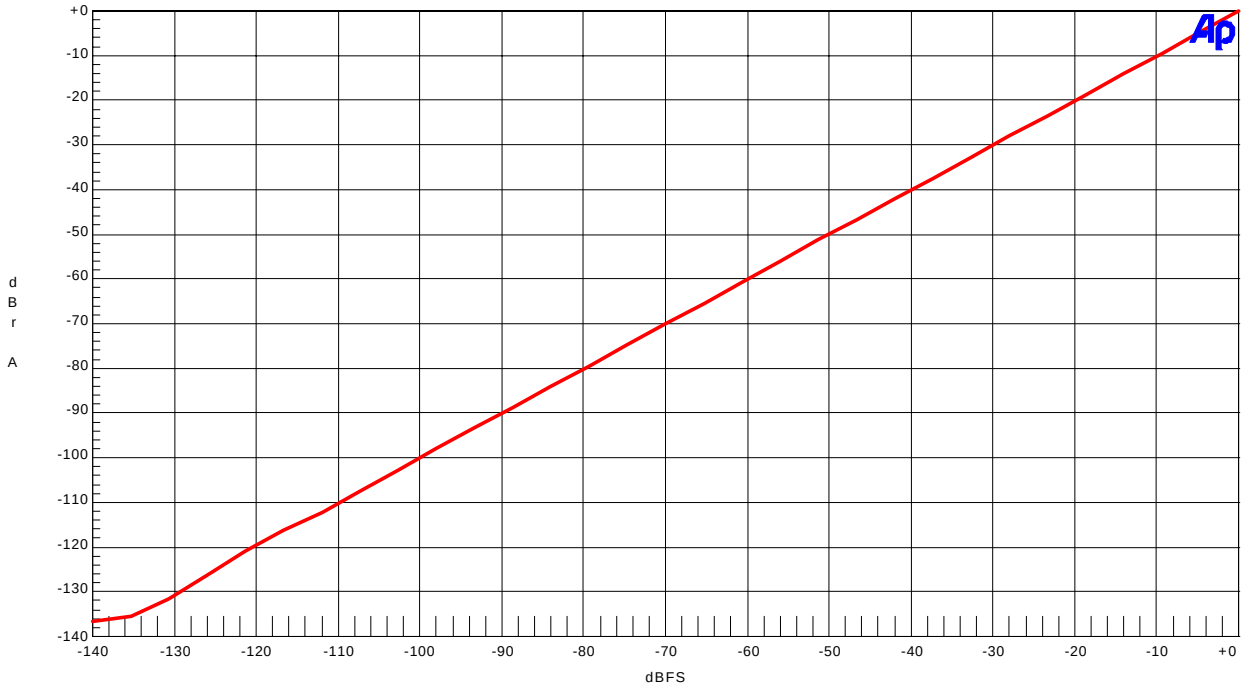
AKM AK4394 THD + N vs Input Frequency(Input Level=0dBFS)



THD +N vs Input Frequency (Input Level=0dBFS)

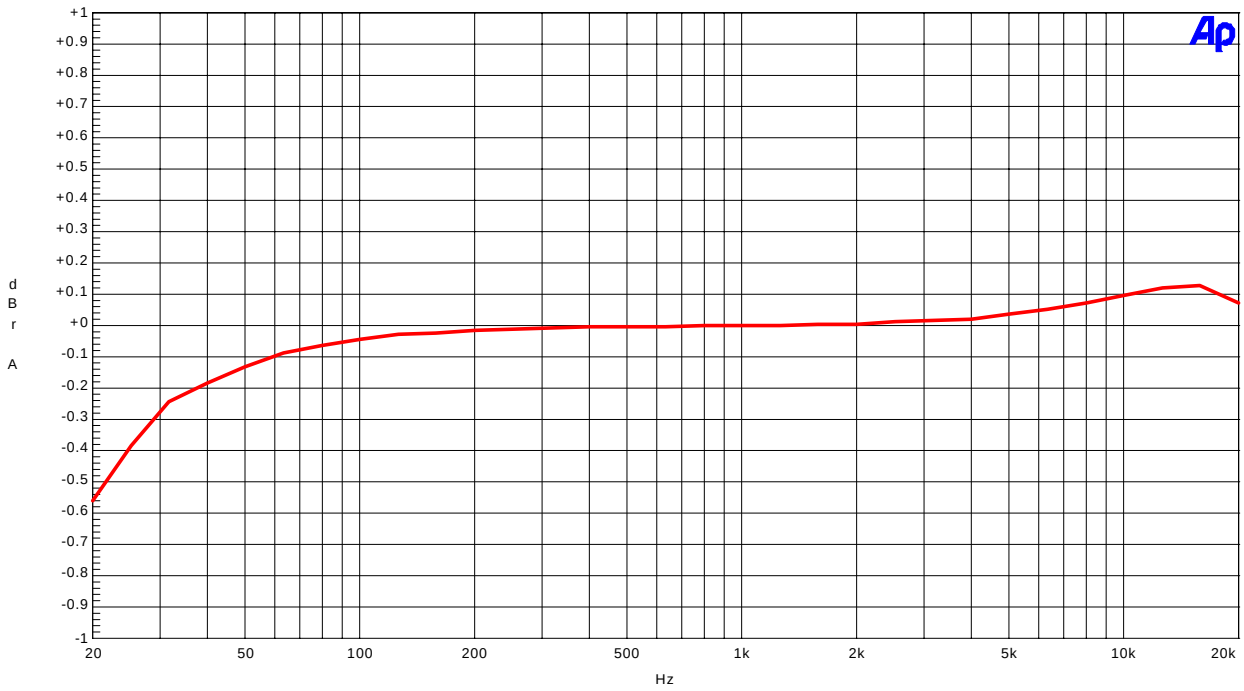
(fs=44.1kHz)

AKM AK4394 Linearity



Linearity (fin=1kHz)

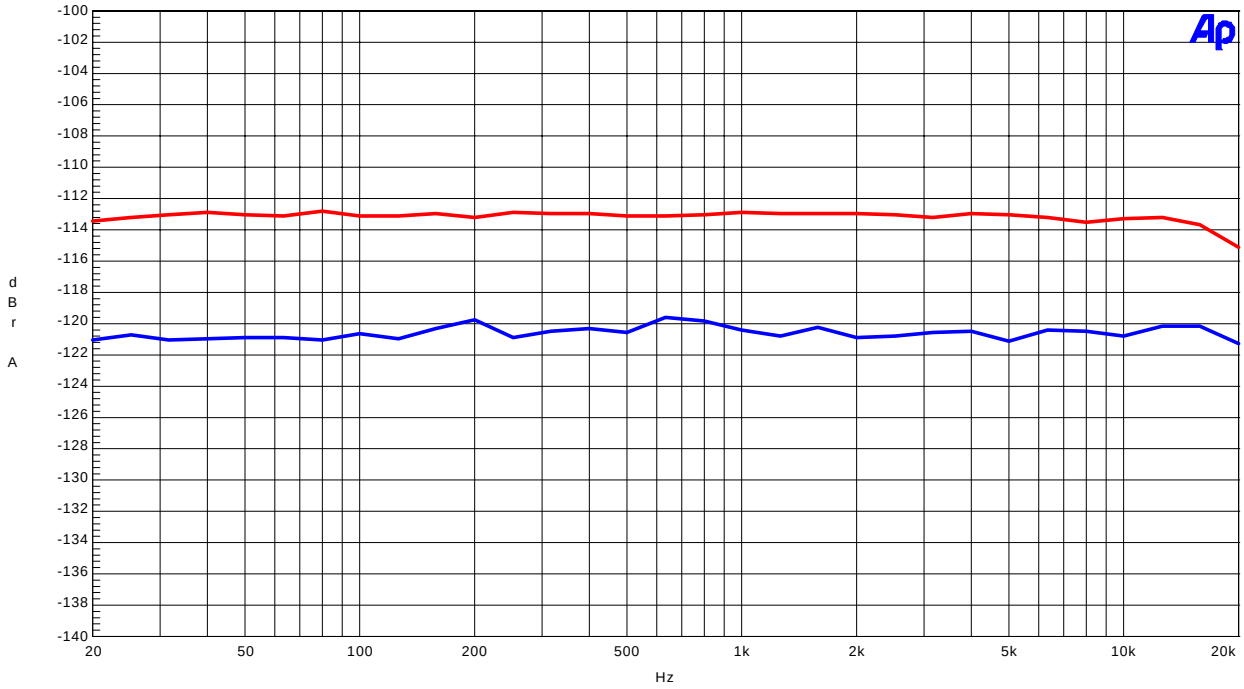
AKM AK4394 Frequency Response



Frequency Response (Input Level=0dBFS)

(fs=44.1kHz)

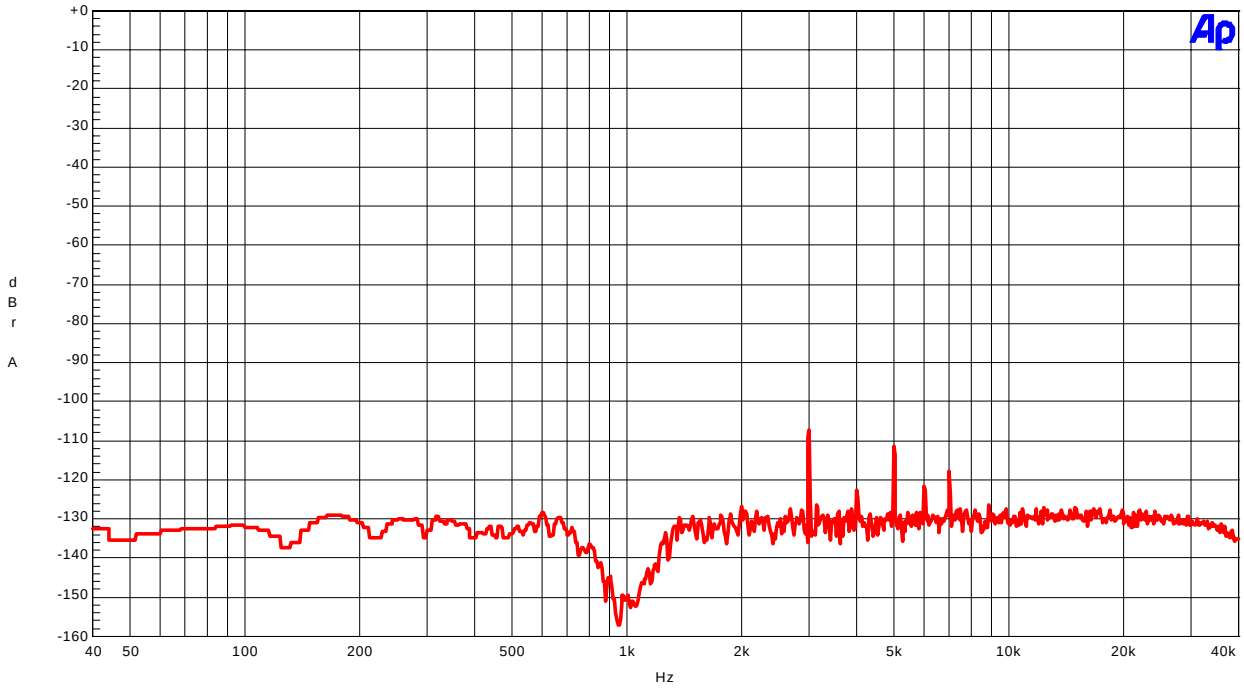
AKM AK4394 Crosstalk



Crosstalk (upper = Rch, Lower = Lch)

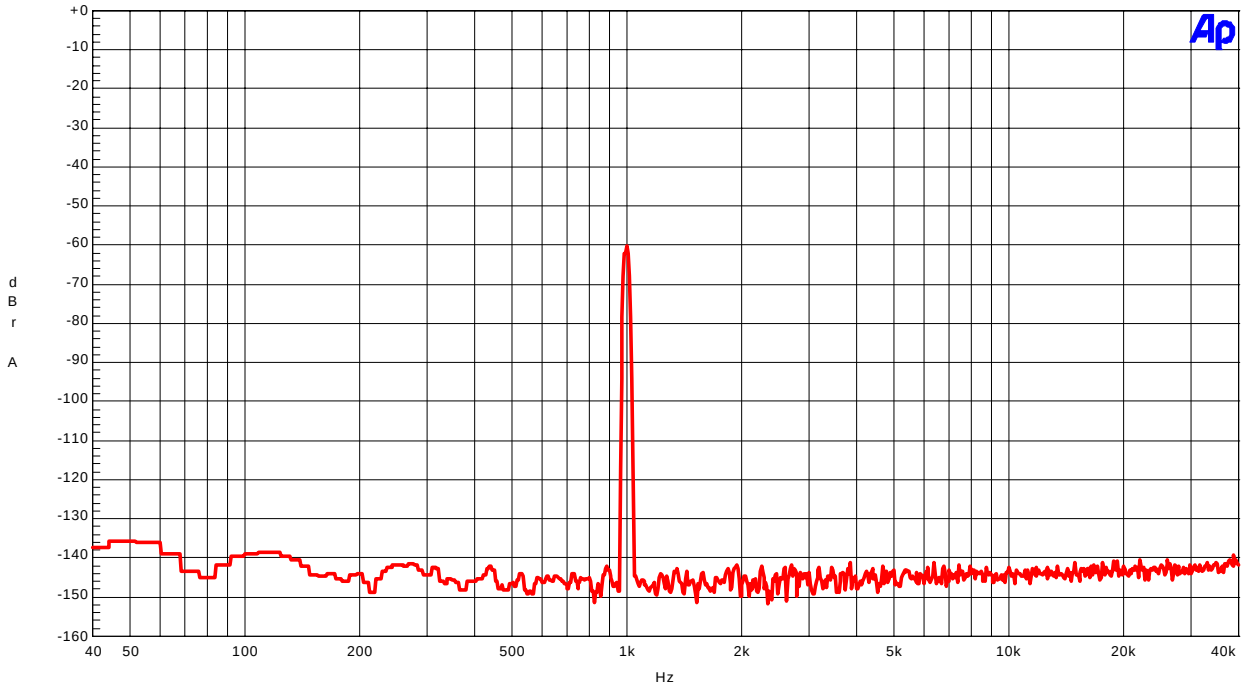
(fs=96kHz)

AKM AK4394 FFT (Input Leve=0dBFS, fin=1kHz, Notch)



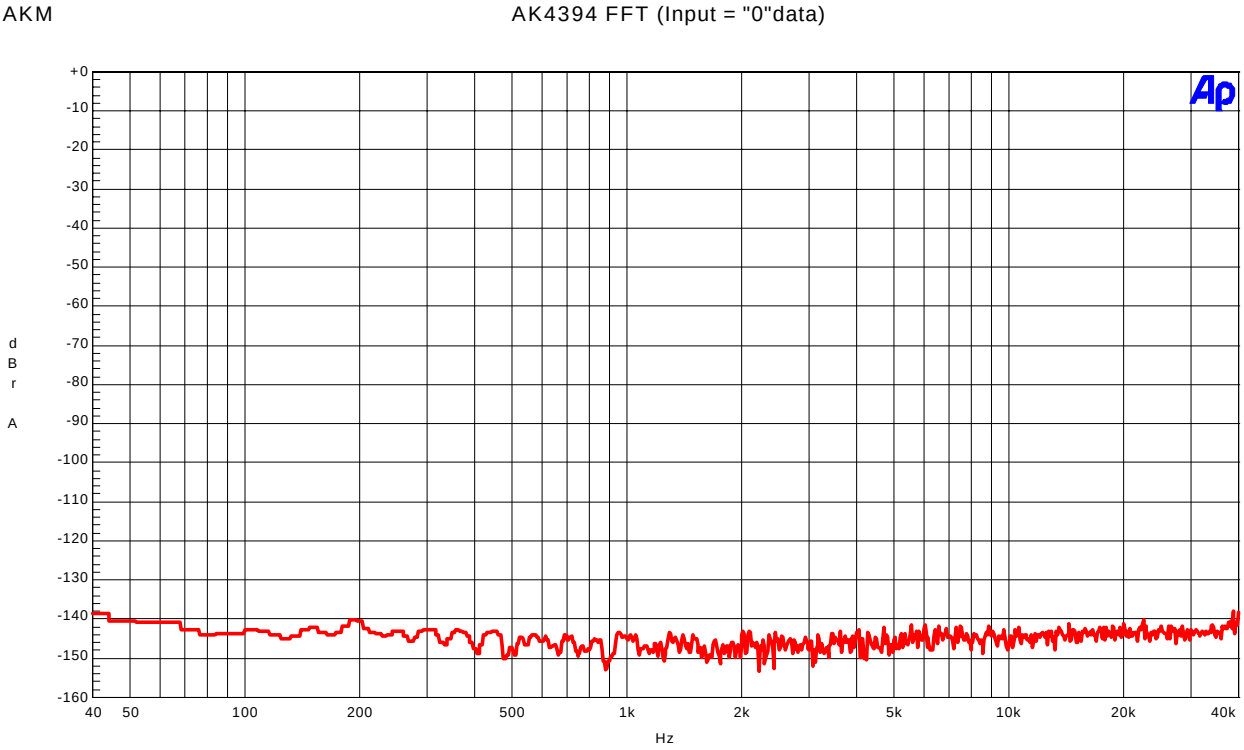
FFT (Input Level=0dBFS, fin=1kHz, notch)

AKM AK4394 FFT (Input Leve=-60dBFS, fin=1kHz)

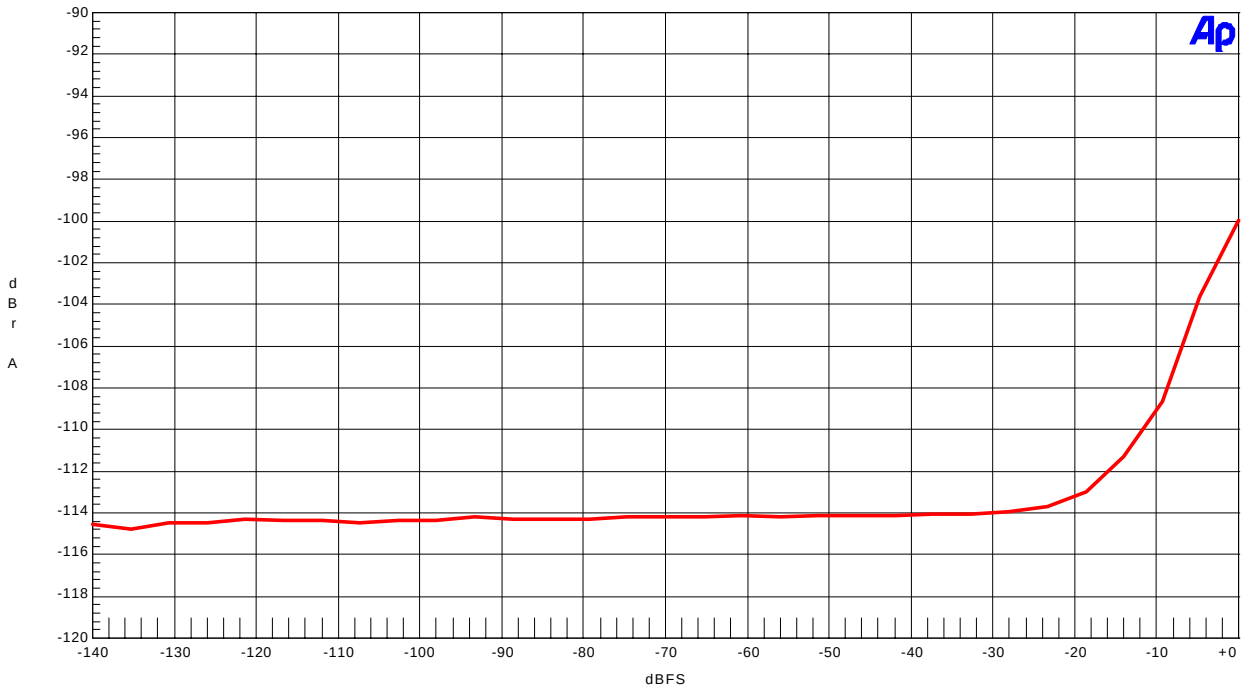


FFT (Input Level=-60dBFS, fin=1kHz)

(fs=96kHz)



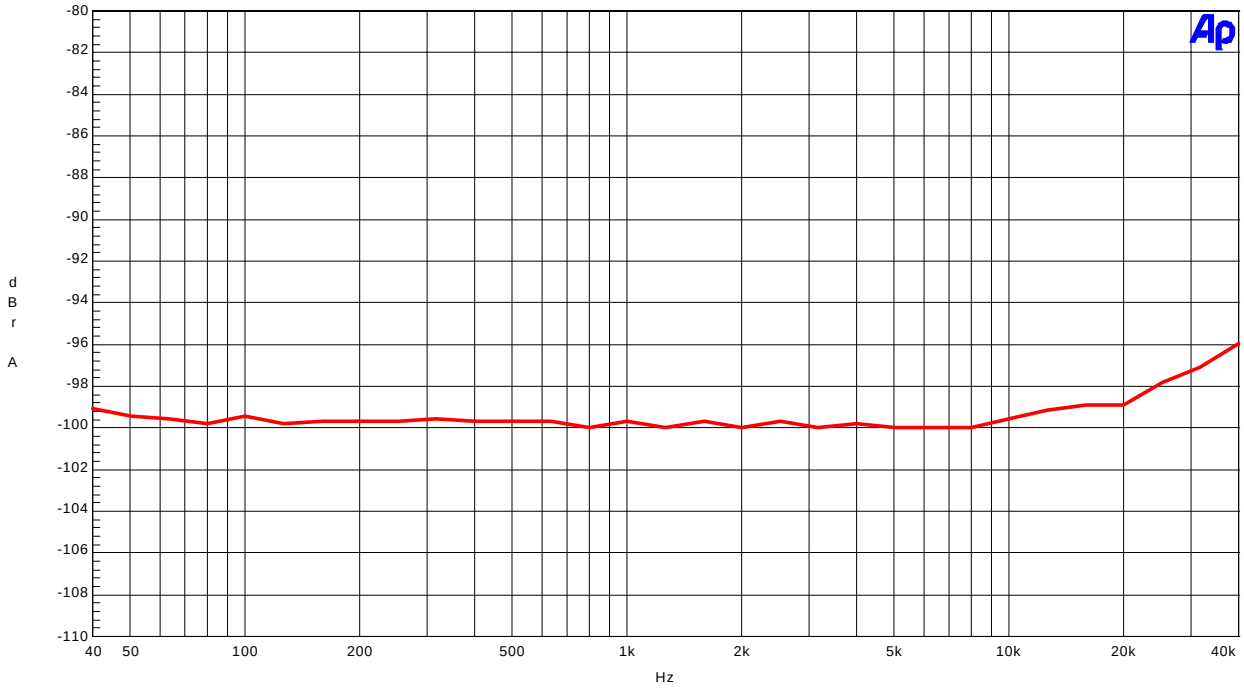
FFT (noise floor)



THD + N vs Amplitude (fin=1kHz)

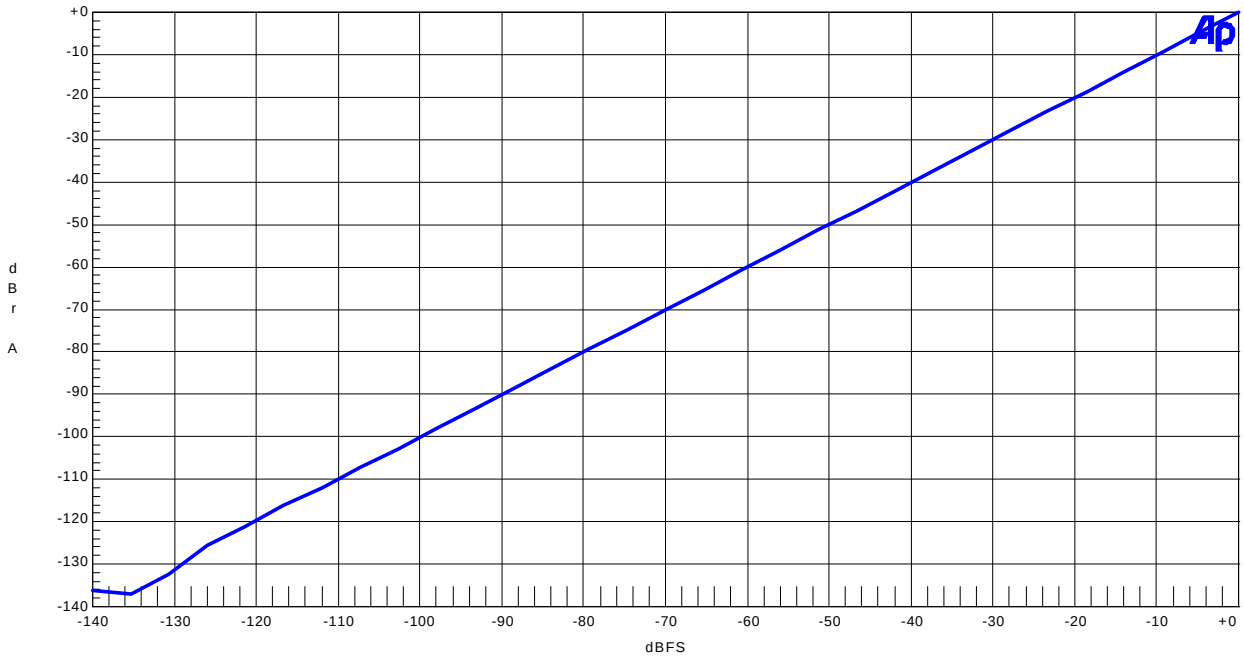
(fs=96kHz)

AKM AK4394 THD + N vs Input Frequency(Input Level=0dBFS)



THD + N vs Input Frequency (Input Level=0dBFS)

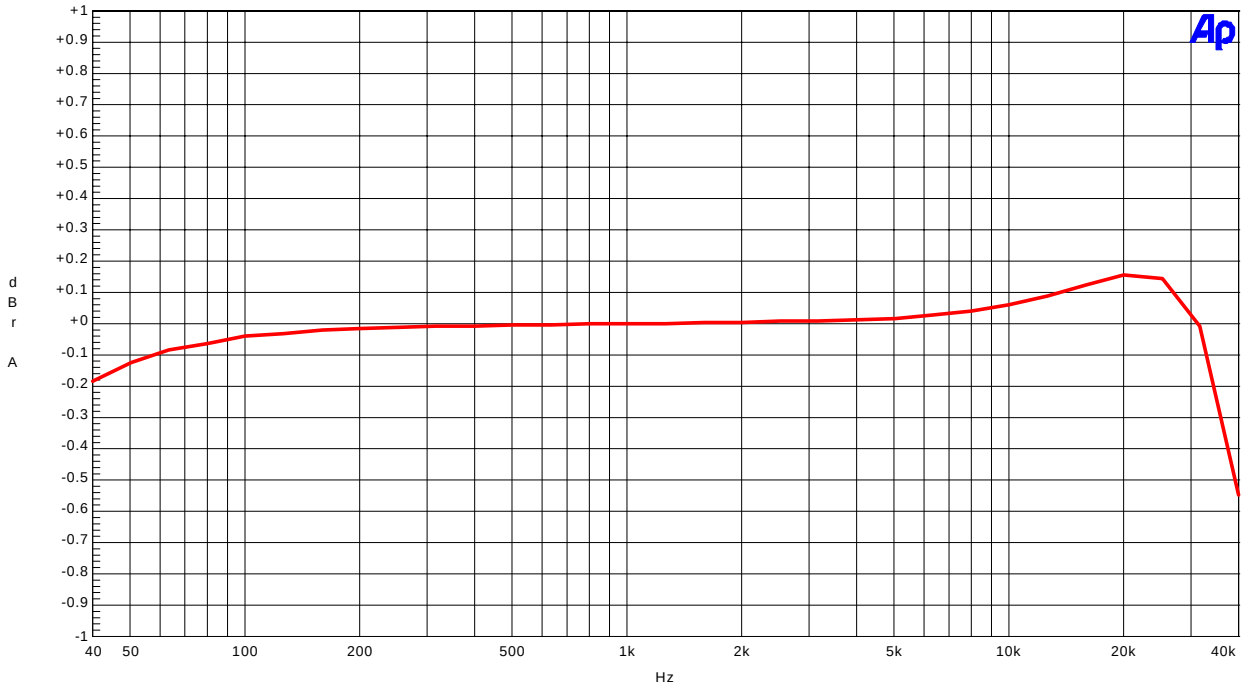
AKM AK4394 Linearity



Linearity (fin=1kHz)

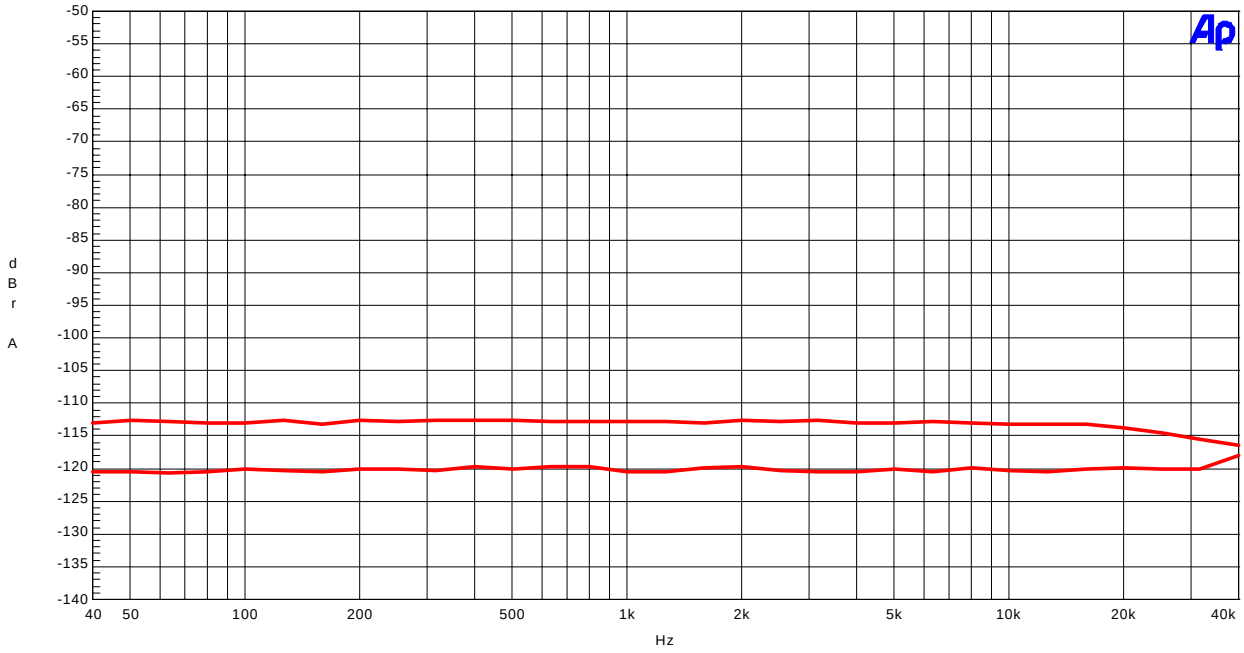
(fs=96kHz)

AKM AK4394 Frequency Response



Frequency Response (Input Level=0dBFS)

AKM AK4394 Crosstalk



Crosstalk (upper = Rch, Lower = Lch)

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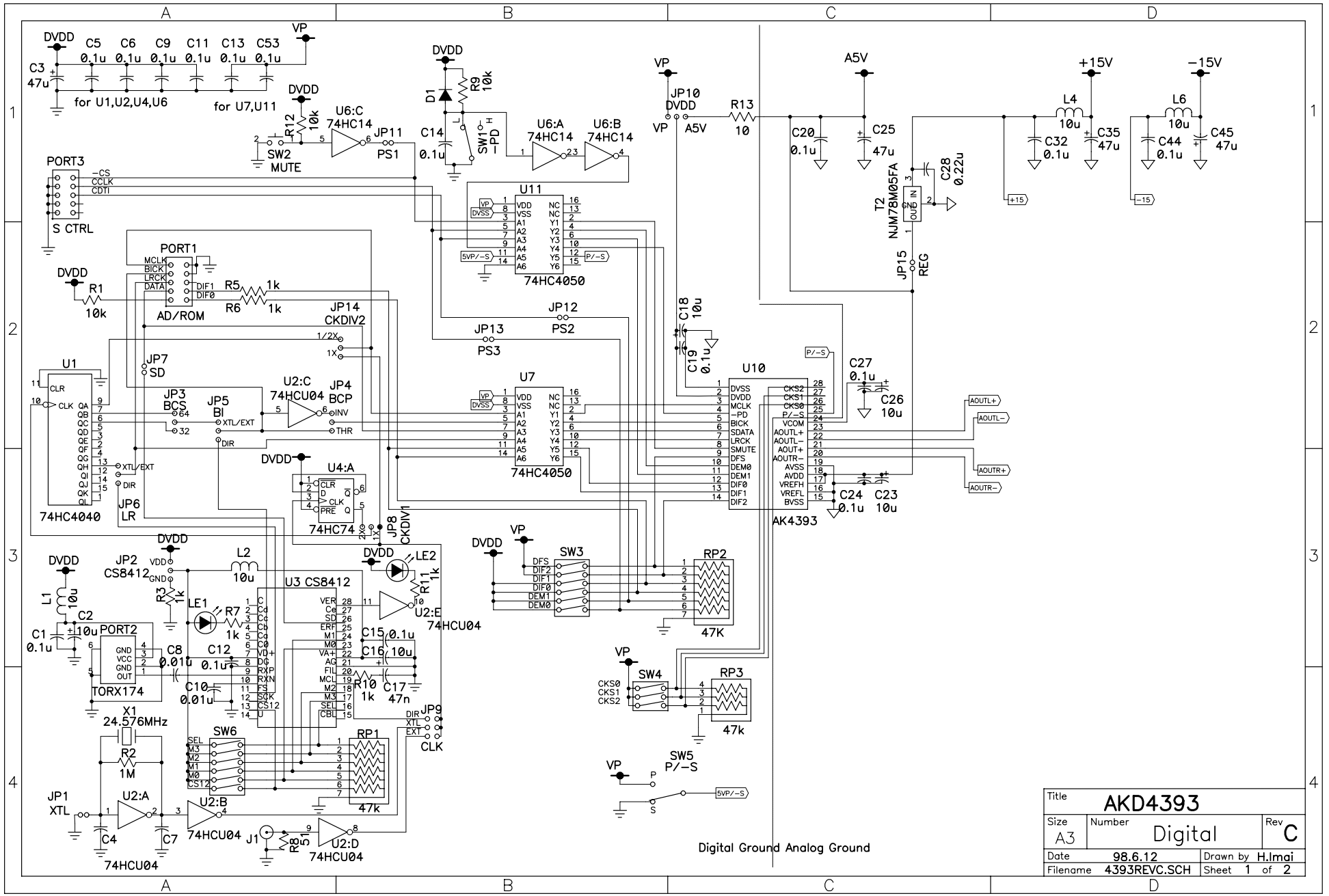
DVDD
VP
C3 47u
C5 0.1u
C6 0.1u
C9 0.1u
C11 0.1u
C13 0.1u
C53 0.1u
for U1,U2,U4,U6
for U7,U11
R12 10k
SW2 MUTE
U6:C 74HC14
JP11 PS1
D1
R9 10k
C14 0.1u
SW1 -PD
U6:A 74HC14
U6:B 74HC14
JP10 DVDD VP A5V
R13 10
C20 0.1u
C25 47u
A5V
+15V
-15V
L4 10u
L6 10u
C32 0.1u
C35 47u
C44 0.1u
C45 47u
T2 NJM78M05FA
C28 0.22u
JP15 REG
PORT3
-CS
CCLK
CDTI
S CTRL
U11
74HC4050
PORT1
MCLK
BICK
LRCK
SDATA
DIF1
DIF0
AD/ROM
R1 10k
R5 1k
R6 1k
JP14 CKDIV2
1/2X
1X
JP12 PS2
JP13 PS3
C18 10u
C19 0.1u
U1
74HC4040
JP7 SD
JP3 BCS
JP5 BI
XTL/EXT
DIR
U2:C 74HCU04
JP4 BCP
INV
THR
U7
74HC4050
U10
AK4393
P/-S
C27 0.1u
C26 10u
C24 0.1u
C23 10u
AOUTL+
AOUTL-
AOUTR+
AOUTR-
JP6 LR
U4:A
74HC74
JP8 CKDIV1
2X
1X
DVDD
VP
SW3
RP2
47K
JP2 CS8412
L2 10u
L1 10u
R3 1k
LE1
R7 1k
LE2
R11 1k
U2:E 74HCU04
U3 CS8412
C2 10u
C1 0.1u
PORT2
TORX174
C8 0.01u
C12 0.1u
C10 0.01u
C15 0.1u
C16 10u
C17 47n
R10 1k
X1 24.576MHz
R2 1M
SW6
RP1
47k
JP9
XTL
EXT
CLK
SW4
RP3
47k
SW5 P/-S
JP1 XTL
U2:A
U2:B
U2:D
74HCU04
C4
C7
R8 51
J1
Digital Ground Analog Ground
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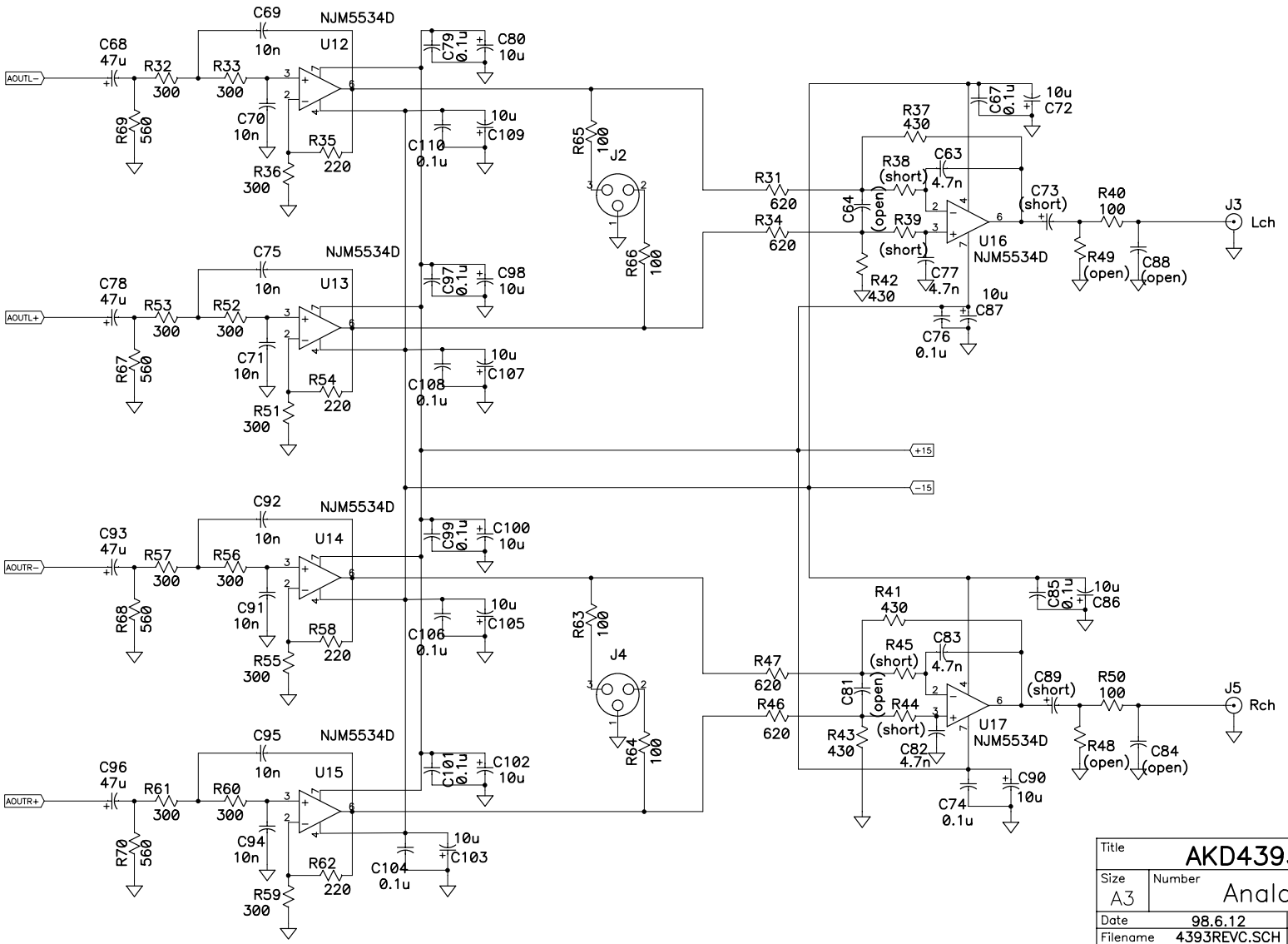
Size A3
Number Digital
Rev C
Date 98.6.12
Drawn by H.Imai
Filename 4393REVC.SCH
Sheet 1 of 2



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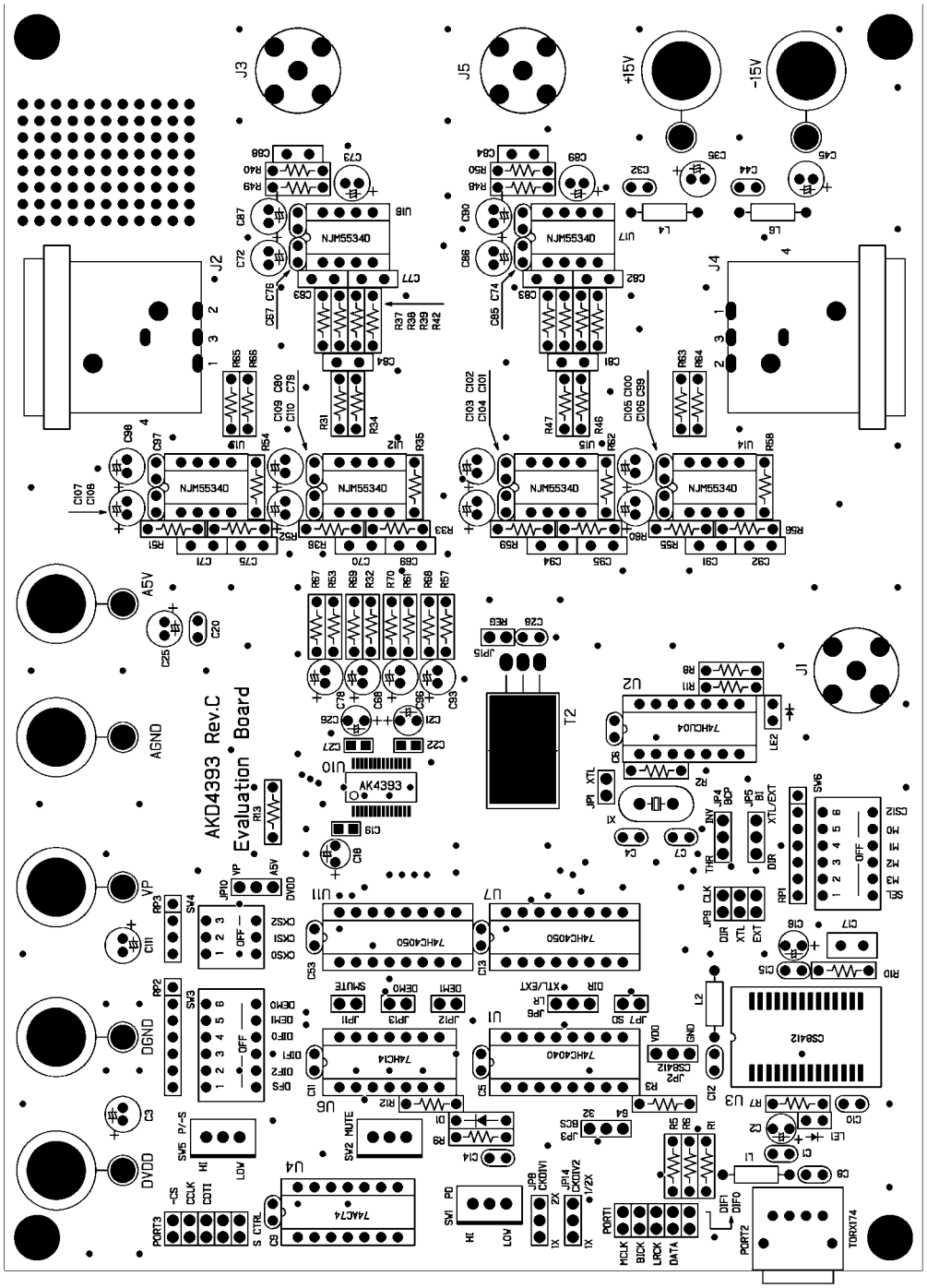
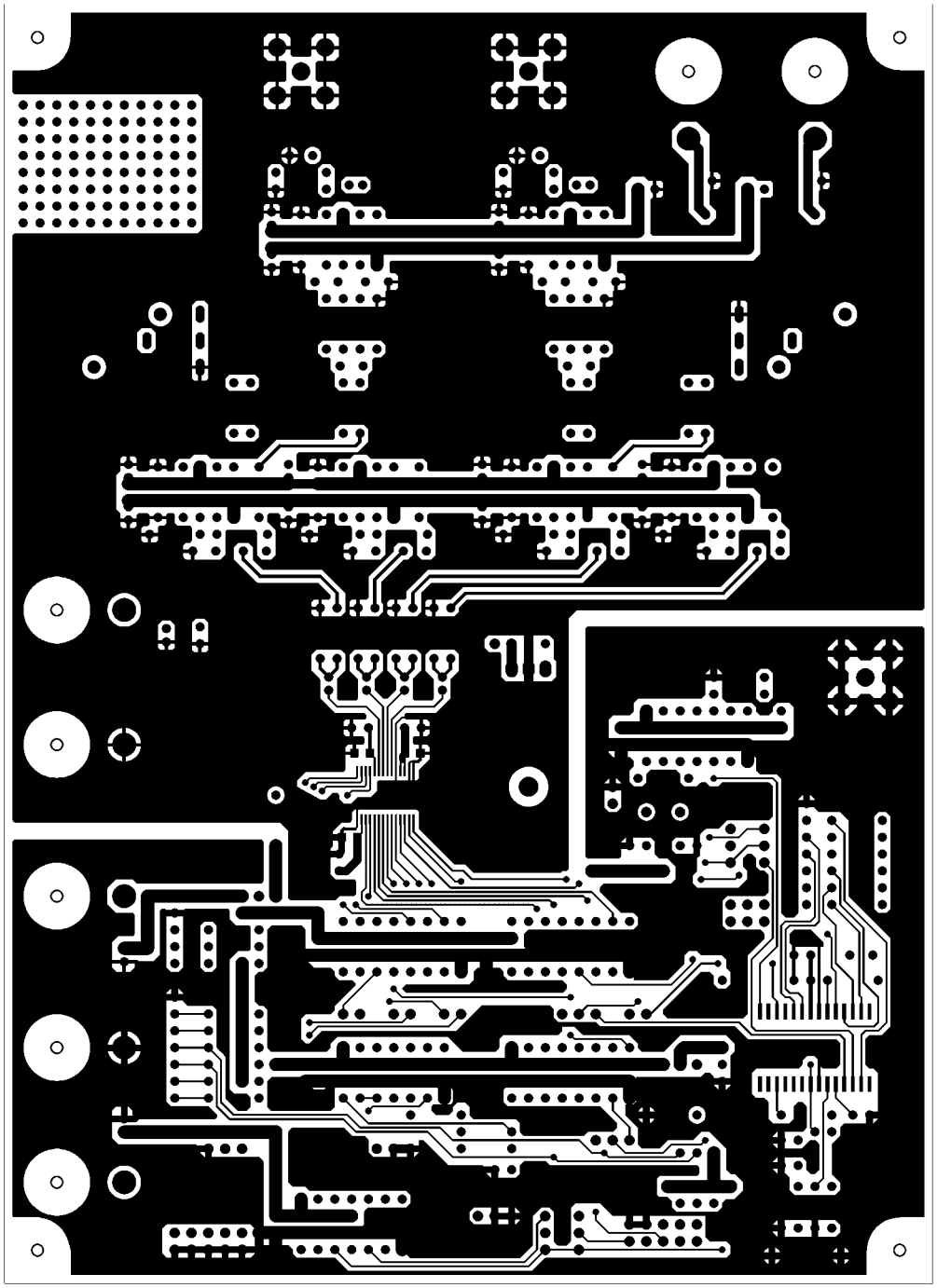


4393C L1 SR SILK



4393C L1

L2 C3936