Audio Codec for Recordable DVD

ADAV803

FEATURES

Stereo analog-to-digital converter (ADC)
- **Supports 48/96 kHz sample rates**
- **102 dB dynamic range**
- **Single-ended input**
- **Automatic level control**

Stereo digital-to-analog converter (DAC)
- **Supports 32/44.1/48/96/192 kHz sample rates**
- **101 dB dynamic range**
- **Single-ended output**

Asynchronous operation of ADC and DAC

Stereo sample rate converter (SRC)
- **Input/output range: 8 kHz to 192 kHz**
- **140 dB dynamic range**

Digital interfaces
- **Record**
- **Playback**
- **Auxiliary record**
- **Auxiliary playback**

S/PDIF (IEC60958) input and output
- **Digital interface receiver (DIR)**
- **Digital interface transmitter (DIT)**

PLL-based audio MCLK generators

Generates required DVDR system MCLKs

Device control via I²C®-compatible serial port

64-lead LQFP package

FUNCTIONAL BLOCK DIAGRAM

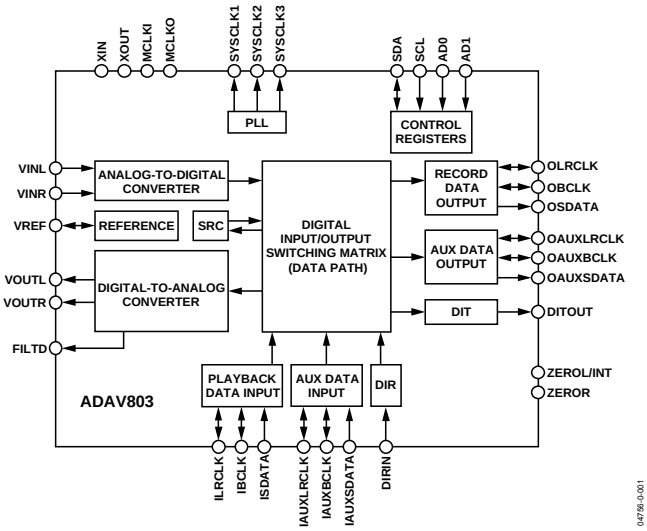

Figure 1.

APPLICATIONS

DVD-recordable

All formats

CD-R/W

PRODUCT OVERVIEW

The ADAV803 is a stereo audio codec intended for applications such as DVD or CD recorders that require high performance and flexible, cost-effective playback and record functionality. The ADAV803 features Analog Devices' proprietary, high performance converter cores to provide record (ADC), playback (DAC), and format conversion (SRC) on a single chip. The ADAV803 record channel features variable input gain to allow for adjustment of recorded input levels and automatic level control, followed by a high performance stereo ADC whose digital output is sent to the record interface. The record channel also features level detectors that can be used in feedback loops to adjust input levels for optimum recording. The playback channel features a high performance stereo DAC with independent digital volume control.

The sample rate converter (SRC) provides high performance sample rate conversion to allow inputs and outputs that require different sample rates to be matched. The SRC input can be selected from playback, auxiliary, DIR, or ADC (record). The SRC output can be applied to the playback DAC, both main and auxiliary record channels, and a DIT. Operation of the ADAV803 is controlled via an I²C-compatible serial interface, which allows the programming of individual control register settings. The ADAV803 operates from a single analog 3.3 V power supply and a digital power supply of 3.3 V with optional digital interface range of 3.0 V to 3.6 V.

The part is housed in a 64-lead LQFP package and is characterized for operation over the commercial temperature range of −40°C to +85°C.

Rev. 0

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TABLE OF CONTENTS

Specifications ... 3
Test Conditions ... 3
ADAV803 Specifications ... 3
Timing Specifications ... 6
Temperature Range ... 7
Absolute Maximum Ratings ... 8
ESD Caution ... 8
Pin Configuration and Function Descriptions ... 9
Typical Performance Characteristics ... 11
Functional Description ... 15
ADC Section ... 15
DAC Section ... 18
Sample Rate Converter (SRC) Functional Overview ... 19
PLL Section ... 22
SPDIF Transmitter and Receiver ... 23
Serial Data Ports ... 27
Interface Control ... 30
I²C Interface ... 30
Block Reads and Writes ... 31
Register Descriptions ... 32
Layout Considerations ... 55
ADC ... 55
DAC ... 55
PLL ... 55
Reset and Power-Down Considerations ... 55
Outline Dimensions ... 56
Ordering Guide ... 56

REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

TEST CONDITIONS

Test conditions, unless otherwise noted.

Table 1.

Test Parameter	Condition
Supply Voltage	
Analog	3.3 V
Digital	3.3 V
Ambient Temperature	25°C
Master Clock (XIN)	12.288 MHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width (All Converters)	24 bits
Load Capacitance on Digital Outputs	100 pF
ADC Input Frequency	1007.8125 Hz at −1 dBFS
DAC Output Frequency	960.9673 Hz at 0 dBFS
Digital Input	Slave Mode, I²S Justified Format
Digital Output	Slave Mode, I²S Justified Format

ADAV803 SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Comments
PGA SECTION					
Input Impedance		4		kΩ	
Minimum Gain		0		dB	
Maximum Gain		24		dB	
Gain Step		0.5		dB	
REFERENCE SECTION					
Absolute Voltage, V_{REF}		1.5		V	
V_{REF} Temperature Coefficient		80		ppm/°C	
ADC SECTION					
Number of Channels		2			
Resolution		24		Bits	
Dynamic Range					−60 dB input
Unweighted		99		dB	f_S = 48 kHz
		98		dB	f_S = 96 kHz
A-Weighted	98	102		dB	f_S = 48 kHz
		101		dB	f_S = 96 kHz
Total Harmonic Distortion plus Noise					Input = −1.0 dBFS
		−88		dB	f_S = 48 kHz
		−87		dB	f_S = 96 kHz
Analog Input					
Input Range (± Full Scale)		1.0		V rms	
DC Accuracy					
Gain Error	−1.5	−0.8		dB	
Interchannel Gain Mismatch		0.05		dB	
Gain Drift		1		mdB/°C	
Offset		−10		mV	
Crosstalk (EIAJ Method)		−110		dB	
Volume Control Step Size (256 Steps)		0.39		% per step	

Parameter	Min	Typ	Max	Unit	Comments
Maximum Volume Attenuation		−48		dB	
Mute Attenuation		∞		dB	ADC outputs all zero codes
Group Delay					
f_S = 48 kHz		910		µs	
f_S = 96 kHz		460		µs	
ADC LOW-PASS DIGITAL DECIMATION FILTER CHARACTERISTICS[1]					
Pass-Band Frequency		22		kHz	Sample rate: 48 kHz
		44		kHz	Sample rate: 96 kHz
Stop-Band Frequency		26		kHz	Sample rate: 48 kHz
		52		kHz	Sample rate: 96 kHz
Stop-Band Attenuation		120		dB	Sample rate: 48 kHz
		120		dB	Sample rate: 96 kHz
Pass-Band Ripple		±0.01		dB	Sample rate: 48 kHz
		±0.01		dB	Sample rate: 96 kHz
ADC HIGH-PASS DIGITAL FILTER CHARACTERISTICS					
Cutoff Frequency		0.9		Hz	f_S = 48 kHz
SRC SECTION					
Resolution		24		Bits	
Sample Rate	8		192	kHz	XIN = 27 MHz
SRC MCLK	138 × f_{S-MAX}		33	MHz	f_{S-MAX} is the greater of the input or output sample rate
Maximum Sample Rate Ratios					
Upsampling			1:8		
Downsampling			7.75:1		
Dynamic Range		140			20 Hz to f_S/2, 1 kHz, −60 dBFS input, f_{IN} = 44.1 kHz, f_{OUT} = 48 kHz
Total Harmonic Distortion plus Noise		120		dB	20 Hz to f_S/2, 1 kHz, 0 dBFS input. f_{IN} = 44.1 kHz, f_{OUT} = 48 kHz
DAC SECTION					
Number of Channels		2			
Resolution		24		Bits	
Dynamic Range					20 Hz to 20 kHz, −60 dB input
Unweighted		99		dB	f_S = 48 kHz
		98		dB	f_S = 96 kHz
A-Weighted	97	101		dB	f_S = 48 kHz
		100		dB	f_S = 96 kHz
Total Harmonic Distorton plus Noise					Referenced to 1V rms
		−91		dB	f_S = 48 kHz
		−90		dB	f_S = 96 kHz
Analog Outputs					
Output Range (± Full Scale)		1.0		V rms	
Output Resistance		60		Ω	
Common-Mode Output Voltage		1.5		V	
DC Accuracy					
Gain Error	−2	−0.8		dB	
Interchannel Gain Mismatch		0.05		dB	
Gain Drift		1		mdB/°C	
DC Offset	−30		+30	mV	
Crosstalk (EIAJ Method)		−110		dB	
Phase Deviation		0.05		Degrees	
Mute Attenuation		−95.625		dB	
Volume Control Step Size (256 Steps)		0.375		dB	

Parameter	Min	Typ	Max	Unit	Comments
Group Delay					
48 kHz		630		µs	
96 kHz		155		µs	
192 kHz		66		µs	
DAC LOW-PASS DIGITAL INTERPOLATION FILTER CHARACTERISTICS					
Pass-Band Frequency		20		kHz	Sample rate: 44.1 kHz
		22		kHz	Sample rate: 48 kHz
		42		kHz	Sample rate: 96 kHz
Stop-Band Frequency		24		kHz	Sample rate: 44.1 kHz
		26		kHz	Sample rate: 48 kHz
		60		kHz	Sample rate: 96 kHz
Stop-Band Attenuation		70		dB	Sample rate: 44.1 kHz
		70		dB	Sample rate: 48 kHz
		70		dB	Sample rate: 96 kHz
Pass-Band Ripple		±0.002		dB	Sample rate: 44.1 kHz
		±0.002		dB	Sample rate: 48 kHz
		±0.005		dB	Sample rate: 96 kHz
PLL SECTION					
Master Clock Input Frequency		27/54		MHz	
Generated System Clocks					
MCLKO		27/54		MHz	
SYSCLK1	256		768	× f_S	256/384/512/768 × 32/44.1/ 48 kHz
SYSCLK2	256		768	× f_S	256/384/512/768 × 32/44.1/ 48 kHz
SYSCLK3	256	512		× f_S	256/512 × 32/44.1/48 kHz
Jitter					
SYSCLK1		65		ps rms	
SYSCLK2		75		ps rms	
SYSCLK3		75		ps rms	
DIR SECTION					
Input Sample Frequency	27.2		200	kHz	
Differential Input Voltage	200			mV	
DIT SECTION					
Output Sample Frequency	27.2		200	kHz	
DIGITAL I/O					
Input Voltage High, V_{IH}	2.0		DVDD	V	
Input Voltage Low, V_{IL}			0.8	V	
Input Leakage, I_{IH} @ V_{IH} = 3.3 V			10	µA	
Input Leakage, I_{IL} @ V_{IL} = 0 V			10	µA	
Output Voltage High, V_{OH} @ I_{OH} = 0.4 mA	2.4			V	
Output Voltage Low, V_{OL} @ I_{OL} = −2 mA			0.4	V	
Input Capacitance			15	pF	
POWER					
Supplies					
Voltage, AVDD	3.0	3.3	3.6	V	
Voltage, DVDD	3.0	3.3	3.6	V	
Voltage, ODVDD	3.0	3.3	3.6	V	
Operating Current					All supplies at 3.3 V
Analog Current			60	mA	
Digital Current			38	mA	
Digital Interface Current			13	mA	
DIRIN/DIROUT Current		5		mA	
PLL Current			18	mA	

Parameter	Min	Typ	Max	Unit	Comments
Power-Down Current					$\overline{\text{RESET}}$ low, no MCLK
Analog Current		18		mA	
Digital Current		2.5		mA	
Digital Interface Current		700		µA	
DIRIN/DIROUT Current		3.5		mA	
PLL Current		900		µA	
Power Supply Rejection					
Signal at Analog Supply Pins		−70		dB	1 kHz, 300 mV p-p
		−70		dB	20 kHz, 300 mV p-p

[1] Guaranteed by design.

TIMING SPECIFICATIONS

Timing specifications are guaranteed over the full temperature and supply range.

Table 3.

Parameter		Min	Typ	Max	Unit	Comments
MASTER CLOCK AND RESET						
f_{MCLK}	MCLKI Frequency		12.288	54	MHz	
f_{XIN}	XIN Frequency		27	54	MHz	
t_{RESET}	$\overline{\text{RESET}}$ Low	20			ns	
I^2C PORT						
f_{SCL}	SCL Clock Frequency			400	kHz	
t_{SCLH}	SCL High	0.6			µs	
t_{SCLL}	SCL Low	1.3			µs	
Start Condition						
t_{SCS}	Setup Time	0.6			µs	Relevant for repeated start condition
t_{SCH}	Hold Time	0.6			µs	After this period, the first clock is generated
t_{DS}	Data Setup Time	100			ns	
t_{SCR}	SCL Rise Time			300	ns	
t_{SCF}	SCL Fall Time			300	ns	
t_{SDR}	SDA Rise Time			300	ns	
t_{SDF}	SDA Fall Time			300	ns	
Stop Condition						
t_{SCS}	Setup Time		0.6		µs	
SERIAL PORTS[1]						
Slave Mode						
t_{SBH}	xBCLK High	40			ns	
t_{SBL}	xBCLK Low	40			ns	
f_{SBF}	xBCLK Frequency	$64 \times f_S$				
t_{SLS}	xLRCLK Setup	10			ns	To xBCLK rising edge
t_{SLH}	xLRCLK Hold	10			ns	From xBCLK rising edge
t_{SDS}	xSDATA Setup	10			ns	To xBCLK rising edge
t_{SDH}	xSDATA Hold	10			ns	From xBCLK rising edge
t_{SDD}	xSDATA Delay	10			ns	From xBCLK falling edge

Parameter		Min	Typ	Max	Unit	Comments
Master Mode						
t_{MLD}	xLRCLK Delay			5	ns	From xBCLK falling edge
t_{MDD}	xSDATA Delay			10	ns	From xBCLK falling edge
t_{MDS}	xSDATA Setup	10			ns	From xBCLK rising edge
t_{MDH}	xSDATA Hold	10			ns	From xBCLK rising edge

[1] The prefix x refers to I-, O-, IAUX-, or OAUX- for the full pin name.

TEMPERATURE RANGE

Table 4.

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	−40		+85	°C
Storage	−65		+150	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
DVDD to DGND and ODVDD to DGND	0 V to 4.6 V
AVDD to AGND	0 V to 4.6 V
Digital Inputs	DGND − 0.3 V to DVDD + 0.3 V
Analog Inputs	AGND − 0.3 V to AVDD + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Reference Voltage	Indefinite short circuit to ground
Soldering (10 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

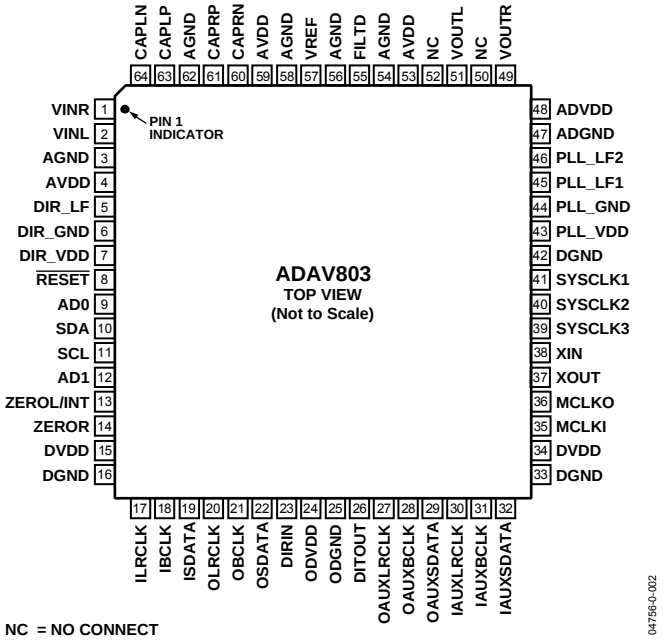

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	VINR	I	Analog Audio Input, Right Channel.
2	VINL	I	Analog Audio Input, Left Channel.
3	AGND		Analog Ground.
4	AVDD		Analog Voltage Supply.
5	DIR_LF		DIR Phase-Locked Loop (PLL) Filter Pin.
6	DIR_GND		Supply Ground for DIR Analog Section. This pin should be connected to AGND.
7	DIR_VDD		Supply for DIR Analog Section. This pin should be connected to AVDD.
8	$\overline{\text{RESET}}$	I	Asychronous Reset Input (Active Low).
9	AD0	I	I^2C Address LSB.
10	SDA	I/O	Data Input/Output of I^2C-Compatible Control Interface.
11	SCL	I	Clock Input of I^2C Compatible Control Interface.
12	AD1	I	I^2C Address MSB.
13	ZEROL/INT	O	Left Channel (Output) Zero Flag or Interrupt (Output) Flag. The function of this pin is determined by the INTRPT pin in DAC Control Register 4.
14	ZEROR	O	Right Channel (Output) Zero Flag.
15	DVDD		Digital Voltage Supply.
16	DGND		Digital Ground.
17	ILRCLK	I/O	Sampling Clock (LRCLK) of Playback Digital Input Port.
18	IBCLK	I/O	Serial Clock (BCLK) of Playback Digital Input Port.
19	ISDATA	I	Data Input of Playback Digital Input Port.
20	OLRCLK	I/O	Sampling Clock (LRCLK) of Record Digital Output Port.
21	OBCLK	I/O	Serial Clock (BCLK) of Record Digital Output Port.
22	OSDATA	O	Data Output of Record Digital Output Port.
23	DIRIN	I	Input to Digital Input Receiver (S/PDIF).
24	ODVDD		Interface Digital Voltage Supply.
25	ODGND		Interface Digital Ground.
26	DITOUT	O	S/PDIF Output from DIT.

Pin No.	Mnemonic	I/O	Description
27	OAUXLRCLK	I/O	Sampling Clock (LRCLK) of Auxiliary Digital Output Port.
28	OAUXBCLK	I/O	Serial Clock (BCLK) of Auxiliary Digital Output Port.
29	OAUXSDATA	O	Data Output of Auxiliary Digital Output Port.
30	IAUXLRCLK	I/O	Sampling Clock (LRCLK) of Auxiliary Digital Input Port.
31	IAUXBCLK	I/O	Serial (BCLK) of Auxiliary Digital Input Port.
32	IAUXSDATA	I	Data Input of Auxiliary Digital Input Port.
33	DGND		Digital Ground.
34	DVDD		Digital Supply Voltage.
35	MCLKI	I	External MCLK Input.
36	MCLKO	O	Oscillator Output.
37	XOUT	I	Crystal Input.
38	XIN	I	Crystal or External MCLK Input.
39	SYSCLK3	O	System Clock 3 (from PLL2).
40	SYSCLK2	O	System Clock 2 (from PLL2).
41	SYSCLK1	O	System Clock 1 (from PLL1).
42	DGND		Digital Ground.
43	PLL_VDD		Supply for PLL Analog Section. This pin should be connected to AVDD.
44	PLL_GND		Ground for PLL Analog Section. This pin should be connected to AGND.
45	PLL_LF1		Loop Filter for PLL1.
46	PLL_LF2		Loop Filter for PLL2.
47	ADGND		Analog Ground (Mixed Signal). This pin should be connected to AGND.
48	ADVDD		Analog Voltage Supply (Mixed Signal). This pin should be connected to AVDD.
49	VOUTR	O	Right Channel Analog Output.
50	NC		No Connect.
51	VOUTL	O	Left Channel Analog Output.
52	NC		No Connect.
53	AVDD		Analog Voltage Supply.
54	AGND		Analog Ground.
55	FILTD		Output DAC Reference Decoupling.
56	AGND		Analog Ground.
57	VREF		Voltage Reference Voltage.
58	AGND		Analog Ground.
59	AVDD		Analog Voltage Supply.
60	CAPRN		ADC Modulator Input Filter Capacitor (Right Channel, Negative).
61	CAPRP		ADC Modulator Input Filter Capacitor (Right Channel, Positive).
62	AGND		Analog Ground.
63	CAPLP		ADC Modulator Input Filter Capacitor (Left Channel, Positive).
64	CAPLN		ADC Modulator Input Filter Capacitor (Left Channel, Negative).

TYPICAL PERFORMANCE CHARACTERISTICS

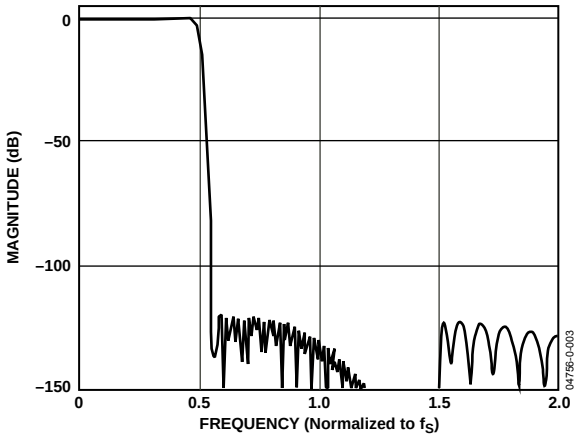

Figure 3. ADC Composite Filter Response

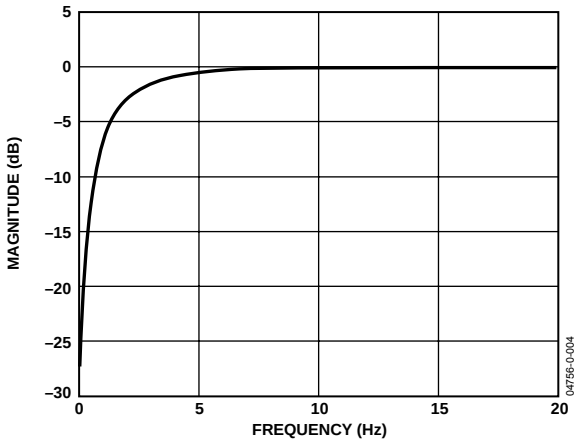

Figure 4. ADC High-Pass Filter Response, f_S = 48 kHz

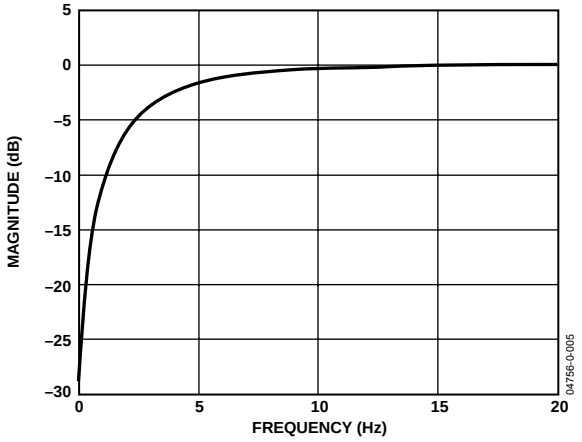

Figure 5. ADC High-Pass Filter Response, f_S = 96 kHz

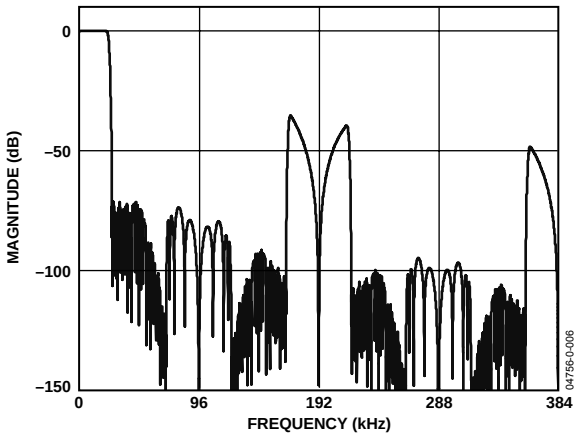

Figure 6. DAC Composite Filter Response, 48 kHz

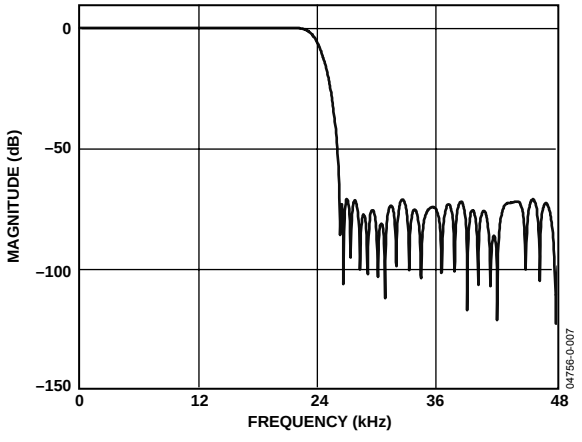

Figure 7. DAC Pass-Band Filter Response, 48 kHz

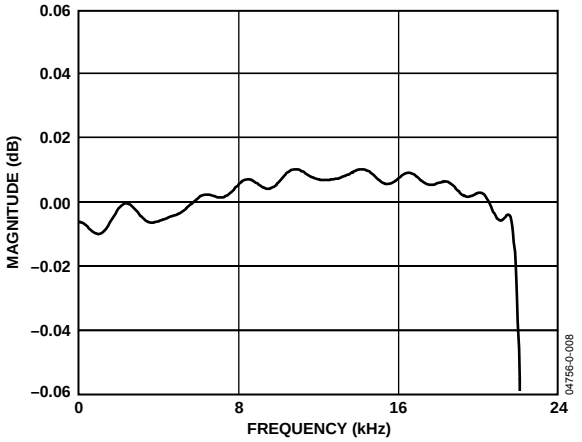

Figure 8. DAC Filter Ripple, 48 kHz

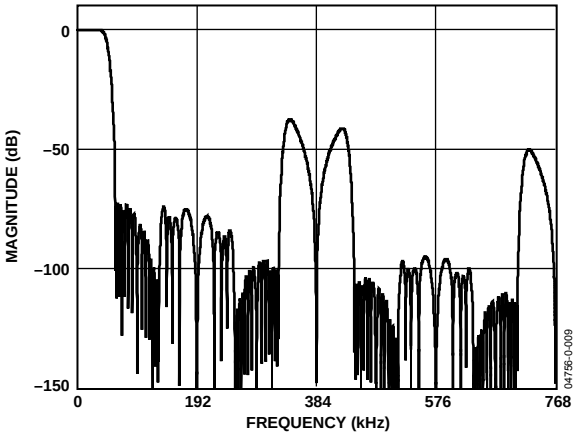

Figure 9. DAC Composite Filter Response, 96 kHz

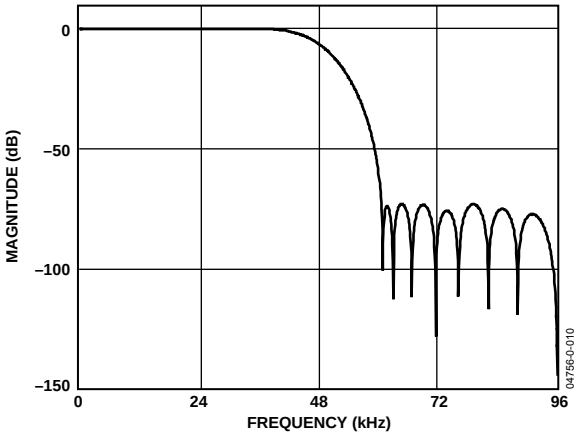

Figure 10. DAC Pass-Band Filter Response, 96 kHz

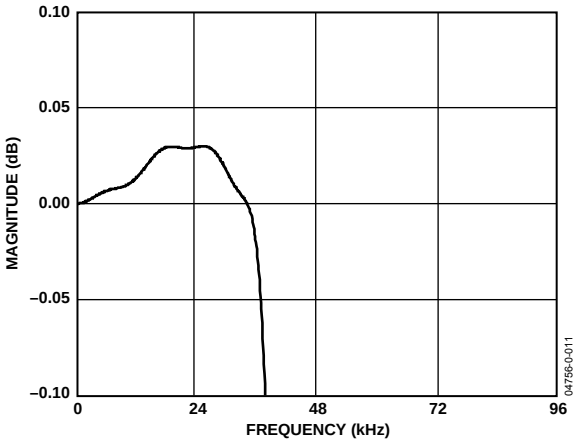

Figure 11. DAC Filter Ripple, 96 kHz

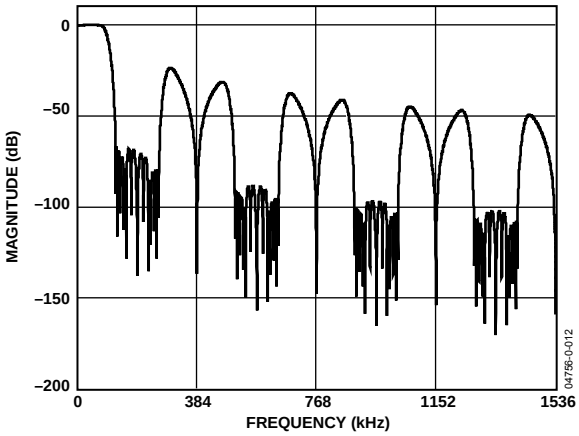

Figure 12. DAC Composite Filter Response, 192 kHz

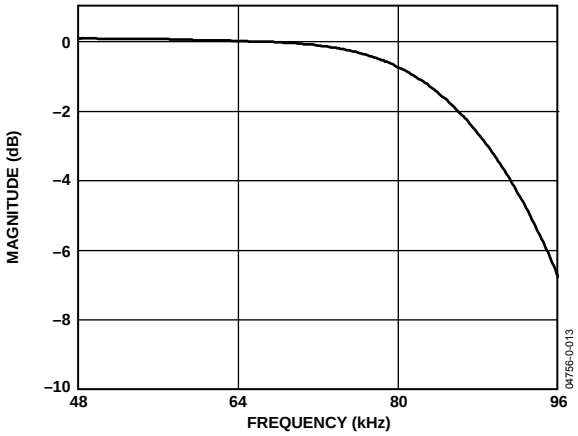

Figure 13. DAC Pass-Band Filter Response, 192 kHz

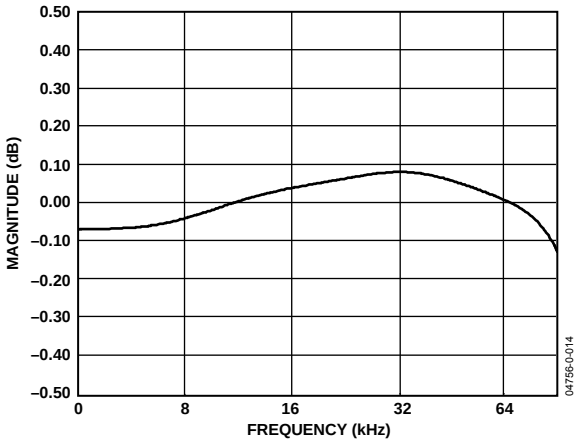

Figure 14. DAC Filter Ripple, 192 kHz

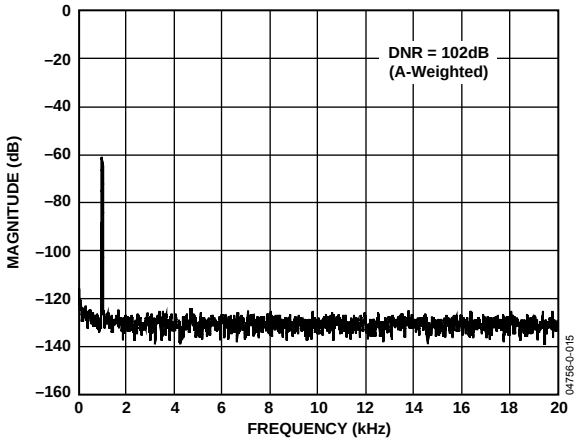

Figure 15. DAC Dynamic Range, f_S = 48 kHz

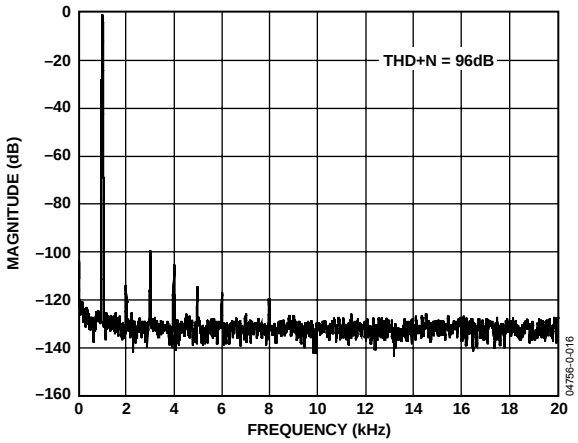

Figure 16. DAC THD + N, f_S = 48 kHz

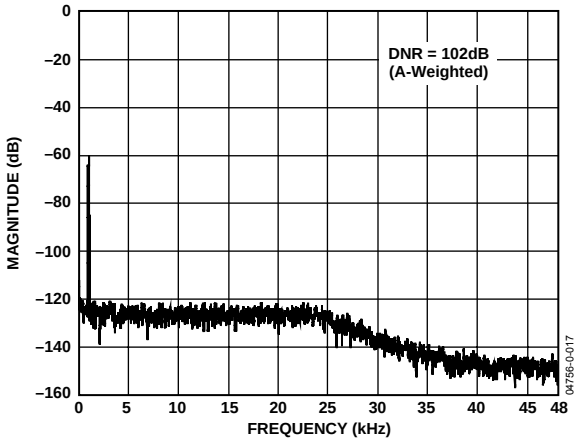

Figure 17. DAC Dynamic Range, f_S = 96 kHz

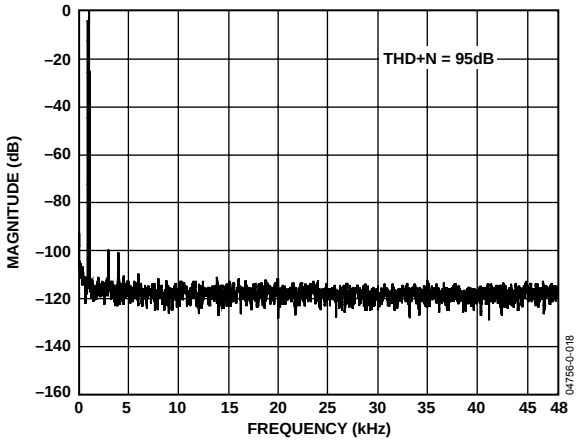

Figure 18. DAC THD + N, f_S = 96 kHz

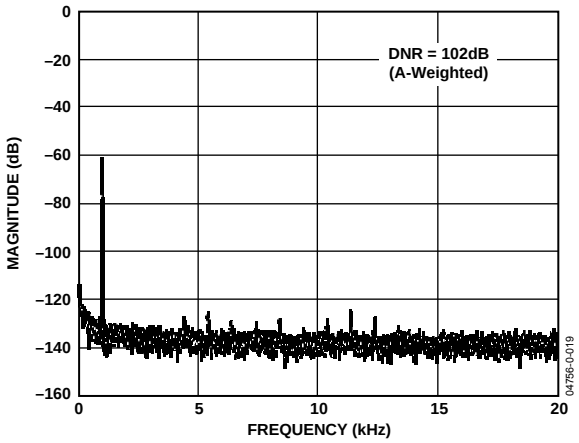

Figure 19. ADC Dynamic Range, f_S = 48 kHz

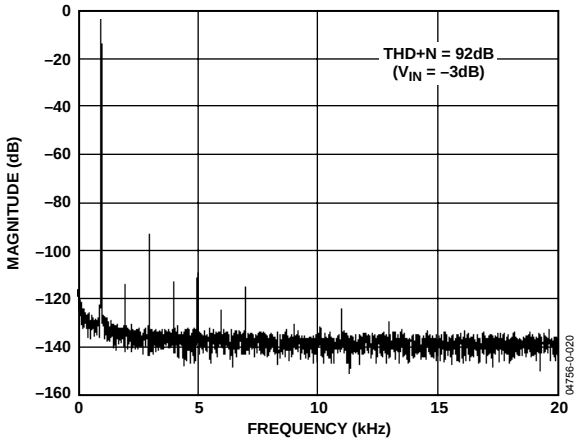

Figure 20. DAC THD + N, f_S = 48 kHz

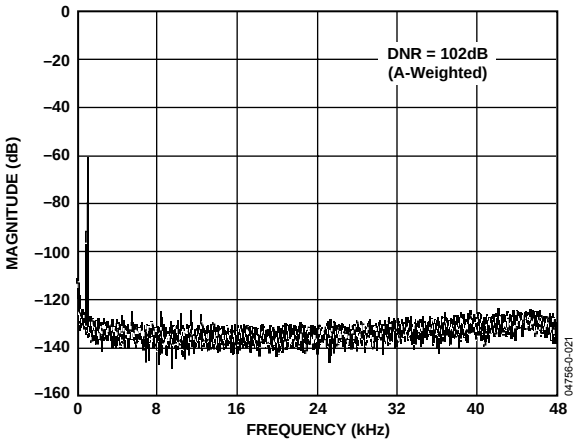

Figure 21. ADC Dynamic Range, f_S = 96 kHz

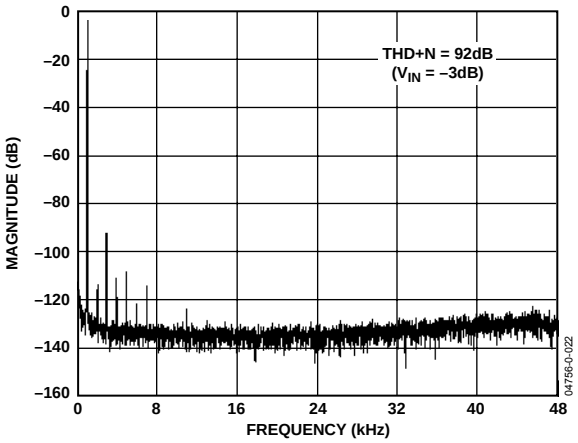

Figure 22. ADC THD + N, f_S = 96 kHz

FUNCTIONAL DESCRIPTION

ADC SECTION

The ADAV803's ADC section is implemented using a second-order multibit (5 bits) Σ-Δ modulator. The modulator is sampled at either half of the ADC MCLK rate (modulator clock = 128 × f_S) or one-quarter of the ADC MCLK rate (modulator clock = 64 × f_S). The digital decimator consists of a Sinc^5 filter followed by a cascade of three half-band FIR filters. The Sinc decimates by a factor of 16 at 48 kHz and by a factor of 8 at 96 kHz. Each of the half-band filters decimates by a factor of 2.

Figure 23 shows the details of the ADC section. The ADC can be clocked by a number of different clock sources to control the sample rate. MCLK selection for the ADC is set by Internal Clocking Control Register 1 (Address 0x76). The ADC provides an output word of up to 24 bits of resolution in twos complement format. The output word can be routed to either the output ports, the sample rate converter, or the SPDIF digital transmitter.

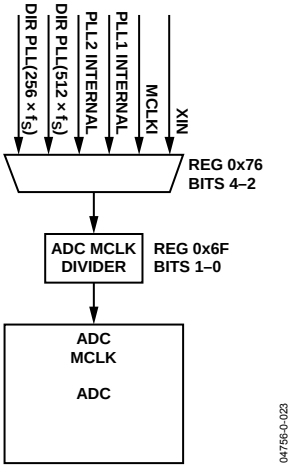

Figure 23. Clock Path Control on the ADC

Programmable Gain Amplifier (PGA)

The input of the record channel features a PGA that converts the single-ended signal to a differential signal, which is applied to the analog Σ-Δ modulator of the ADC. The PGA can be programmed to amplify a signal by up to 24 dB in 0.5 dB increments. Figure 24 shows the structure of the PGA circuit.

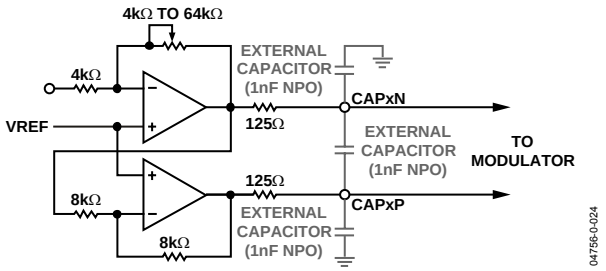

Figure 24. PGA Block Diagram

Analog Σ-Δ Modulator

The ADC features a second-order, multibit, Σ-Δ modulator. The input features two integrators in cascade followed by a flash converter. This multibit output is directed to a scrambler, followed by a DAC for loop feedback. The flash ADC output is also converted from thermometer coding to binary coding for input as a 5-bit word to the decimator. Figure 25 shows the ADC block diagram.

The ADC also features independent digital volume control for the left and right channels. The volume control consists of 256 linear steps, with each step reducing the digital output codes by 0.39%. Each channel also has a peak detector that records the peak level of the input signal. The peak detector register is cleared by reading it.

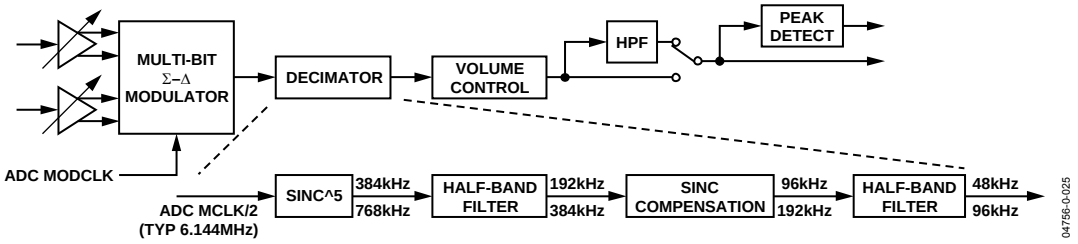

Figure 25. ADC Block Diagram

Automatic Level Control (ALC)

The ADC record channel features a programmable automatic level control block. This block monitors the level of the ADC output signal and automatically reduces the gain, if the signal at the input pins causes the ADC output to exceed a preset limit. This function can be useful to maximize the signal dynamic range when the input level is not well defined. The PGA can be used to amplify the unknown signal, and the ALC reduces the gain until the ADC output is within the preset limits. This results in maximum front end gain.

Because the ALC block monitors the output of the ADC, the volume control function should not be used. The ADC volume control scales the results from the ADC, and any distortion caused by the input signal exceeding the input range of the ADC is still present at the output of the ADC, but scaled by a value determined by the volume control register.

The ALC block has two functions, attack mode and recovery mode. Recovery mode consists of three settings: no recovery, normal recovery, and limited recovery. These modes are discussed in the following sections. Figure 26 is a flow diagram of the ALC block. When the ALC has been enabled, any changes made to the PGA or ALC settings are ignored. To change the functionality of the ALC, it must first be disabled. The settings can then be changed and the ALC re-enabled.

Attack Mode

When the absolute value of the ADC output exceeds the level set by the attack threshold bits in ALC Control Register 2, attack mode is initiated. The PGA gain for both channels is reduced by one step (0.5 dB). The ALC then waits for a time determined by the attack timer bits before sampling the ADC output value again. If the ADC output is still above the threshold, the PGA gain is reduced by a further step. This procedure continues until the ADC output is below the limit set by the attack threshold bits. The initial gains of the PGAs are defined by the ADC left PGA gain register and the ADC right PGA gain register and they can have different values. The ALC subtracts a common gain offset to these values. The ALC preserves any gain difference in dB as defined by these registers. At no time do the PGA gains exceed their initial values. The initial gain setting, therefore, also serves as a maximum value.

The limit detection mode bit in ALC Control Register 1 determines how the ALC responds to an ADC output that exceeds the set limits. If this bit is a 1, then both channels must exceed the threshold before the gain is reduced. This mode can be used to prevent unnecessary gain reduction due to spurious noise on a single channel. If the limit detection mode bit is a 0, the gain is reduced when either channel exceeds the threshold.

No Recovery Mode

By default, there is no gain recovery. Once the gain has been reduced, it is not recovered until the ALC has been reset, either by toggling the ALCEN bit in ALC Control Register 1 or by writing any value to ALC Control Register 3. The latter option is more efficient, because it requires only one write operation to reset the ALC function. No recovery mode prevents volume modulation of the signal caused by adjusting the gain, which can create undesirable artifacts in the signal. The gain can be reduced but not recovered. Therefore, care should be taken that spurious signals do not interfere with the input signal, because these might trigger a gain reduction unnecessarily.

Normal Recovery Mode

Normal recovery mode allows for the PGA gain to be recovered, provided that the input signal meets certain criteria. First, the ALC must not be in attack mode, that is, the PGA gain has been reduced sufficiently such that the input signal is below the level set by the attack threshold bits. Second, the output result from the ADC must be below the level set by the recovery threshold bits in the ALC control register. If both of these criteria are met, the gain is recovered by one step (0.5 dB). The gain is incrementally restored to its original value, assuming that the ADC output level is below the recovery threshold at intervals determined by the recovery time bits.

If the ADC output level exceeds the recovery threshold while the PGA gain is being restored, the PGA gain value is held and does not continue restoration until the ADC output level is again below the recovery threshold. Once the PGA gain is restored to its original value, it is not changed again unless the ADC output value exceeds the attack threshold and the ALC then enters attack mode. Care should be taken when using this mode to choose values for the attack and recovery thresholds that prevent excessive volume modulation caused by continuous gain adjustments.

Limited Recovery Mode

Limited recovery mode offers a compromise between no recovery and normal recovery modes. If the output level of the ADC exceeds the attack threshold, then attack mode is initiated. When attack mode has reduced the PGA gain to suitable levels, the ALC attempts to recover the gain to its original level. If the ADC output level exceeds the level set by the recovery threshold bits, a counter is incremented (GAINCNTR). This counter is incremented at intervals equal to the recovery time selection, if the ADC has any excursion above the recovery threshold. If the counter reaches its maximum value, determined by the GAINCNTR bits in ALC Control Register 1, the PGA gain is deemed suitable and no further gain recovery is attempted. Whenever the ADC output level exceeds the attack threshold, attack mode is reinitiated and the counter is reset.

Selecting a Sample Rate

The output sample rate of the ADC is always ADC MCLK/256, as shown in Figure 23. By default, the ADC modulator runs at ADC MCLK/2. When the ADC MCLK exceeds 12.288 MHz, the ADC modulator should be set to run at ADC MCLK/4. This is achieved by setting the AMC (ADC Modulator Clock) bit in the ADC Control Register 1. To compensate for the reduced modulator clock speed, a different set of filters is used in the decimator section ensuring that the sample rate remains the same.

The AMC bit can also be used to boost the THD + N performance of the ADC at the expense of dynamic range. The improvement is typically 0.5 dB to 1.0 dB and works, because selecting the lower modulator rate reduces the amount of digital noise, improving THD + N, but reduces the oversampling ratio, therefore reducing the dynamic range by a corresponding amount.

For best performance of the ADC, avoid using similar frequency clocks from separate sources in the ADAV803. For example, running the ADC from a 12.288 MHz clock connected to MCLKI and using the PLL to generate a separate 12.288 MHz clock for the DAC can reduce the performance of the ADC. This is due to the interaction of the clocks, which generate beat frequencies that can affect the charge on the switch capacitors of the analog inputs.

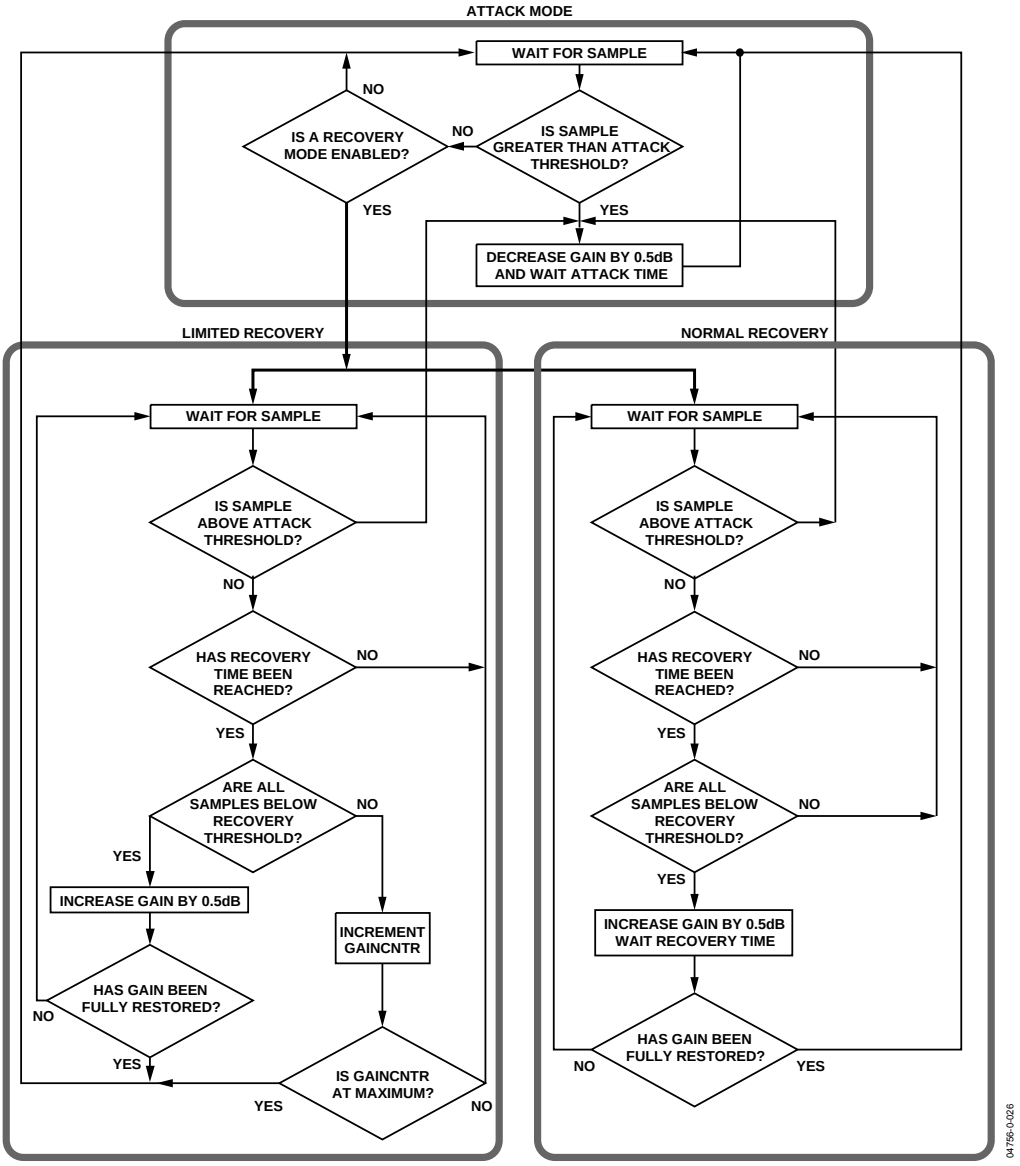

Figure 26. ALC Flow Diagram

DAC SECTION

The ADAV803 has two DAC channels arranged as a stereo pair with single-ended analog outputs. Each channel has its own independently programmable attenuator, adjustable in 128 steps of 0.375 dB per step. The DAC can receive data from the playback or auxiliary input ports, the SRC, the ADC, or the DIR. Each analog output pin sits at a dc level of VREF, and swings 1.0 V rms for a 0 dB digital input signal. A single op amp third-order external low-pass filter is recommended to remove high frequency noise present on the output pins. Note that the use of op amps with low slew rate or low bandwidth can cause high frequency noise and tones to fold down into the audio band. Care should be taken in selecting these components.

The FILTD and FILTR pins should be bypassed by external capacitors to AGND. The FILTD pin is used to reduce the noise of the internal DAC bias circuitry, thereby reducing the DAC output noise. The voltage at the VREF pin, FILTR, can be used to bias external op amps used to filter the output signals. For applications in which the FILTR is required to drive external op amps, which might draw more than 50 μA or have dynamic load changes, extra buffering should be used to preserve the quality of the ADAV803 reference.

The digital input data source for the DAC can be selected from a number of available sources by programming the appropriate bits in the datapath control register. Figure 27 shows how the digital data source and the MCLK source for the DAC are selected. Each DAC has an independent volume register giving 256 steps of control, with each step giving approximately 0.375 dB of attenuation. Note that the DACs are muted by default to prevent unwanted pops, clicks, and other noises from appearing on the outputs while the ADAV803 is being configured. Each DAC also has a peak-level register that records the peak value of the digital audio data. Reading the register clears the peak.

Selecting a Sample Rate

Correct operation of the DAC is dependent upon the data rate provided to the DAC, the master clock applied to the DAC, and the selected interpolation rate. By default, the DAC assumes that the MCLK rate is 256 times the sample rate, which requires an 8-times oversampling rate. This combination is suitable for sample rates of up to 48 kHz.

For a 96 kHz data rate that has a 24.576 MHz MCLK (256 × f_S) associated with it, the DAC MCLK divider should be set to divide the MCLK by 2. This prevents the DAC engine from running too fast. To compensate for the reduced MCLK rate, the interpolator should be selected to operate in 4 × (DAC MCLK = 128 × f_S). Similar combinations can be selected for different sample rates.

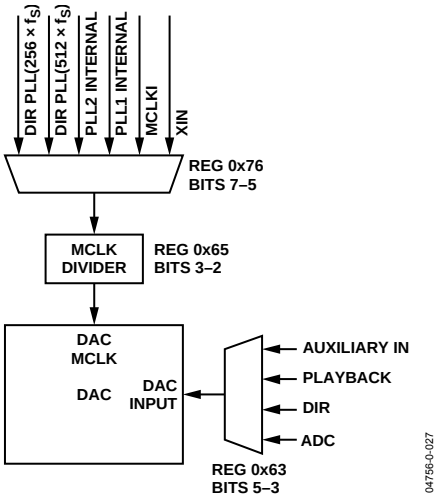

Figure 27. Clock and Datapath Control on the DAC

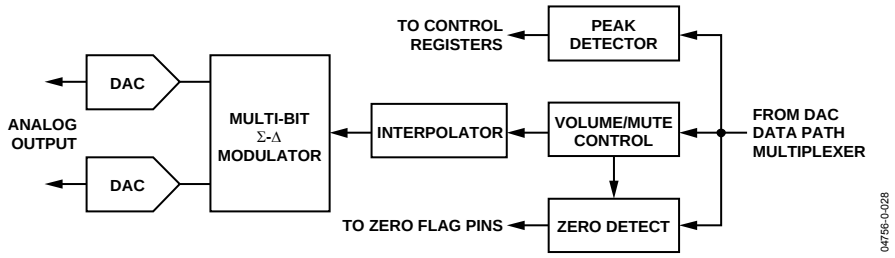

Figure 28. DAC Block Diagram

SAMPLE RATE CONVERTER (SRC) FUNCTIONAL OVERVIEW

During asynchronous sample rate conversion, data can be converted at the same sample rate or at different sample rates. The simplest approach to an asynchronous sample rate conversion is to use a zero-order hold between the two samplers, as shown in Figure 29. In an asynchronous system, T2 is never equal to T1, nor is the ratio between T2 and T1 rational. As a result, samples at f_{S_OUT} are repeated or dropped, producing an error in the resampling process.

The frequency domain shows the wide side lobes that result from this error when the sampling of f_{S_OUT} is convolved with the attenuated images from the SIN(x)/x nature of the zero-order hold. The images at f_{S_IN} (dc signal images) of the zero-order hold are infinitely attenuated. Because the ratio of T2 to T1 is an irrational number, the error resulting from the resampling at f_{S_OUT} can never be eliminated. The error can be significantly reduced, however, through interpolation of the input data at f_{S_IN}. Therefore, the sample rate converter in the ADAV803 is conceptually interpolated by a factor of 2^{20}.

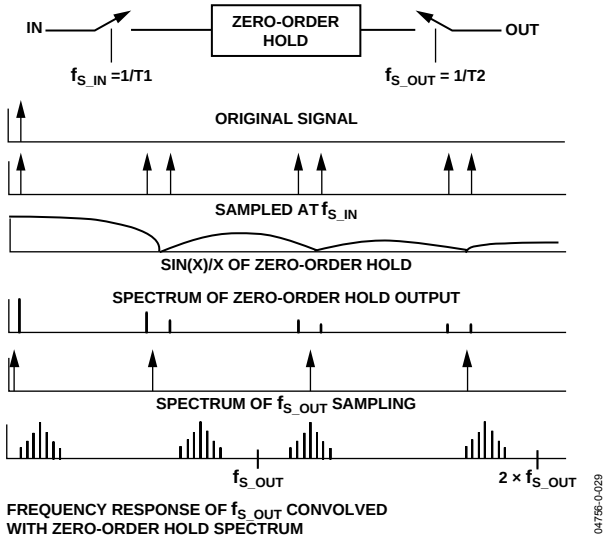

Figure 29. Zero-Order Hold Used by f_{S_OUT} to Resample Data from f_{S_IN}

Conceptual High Interpolation Model

Interpolation of the input data by a factor of 2^{20} involves placing $(2^{20} - 1)$ samples between each f_{S_IN} sample. Figure 30 shows both the time domain and the frequency domain of interpolation by a factor of 2^{20}. Conceptually, interpolation by 2^{20} involves the steps of zero-stuffing $(2^{20} - 1)$ number of samples between each f_{S_IN} sample and convolving this interpolated signal with a digital low-pass filter to suppress the images. In the time domain, it can be seen that f_{S_OUT} selects the closest $f_{S\_IN} \times 2^{20}$ sample from the zero-order hold, as opposed to the nearest f_{S_IN} sample in the case of no interpolation. This significantly reduces the resampling error.

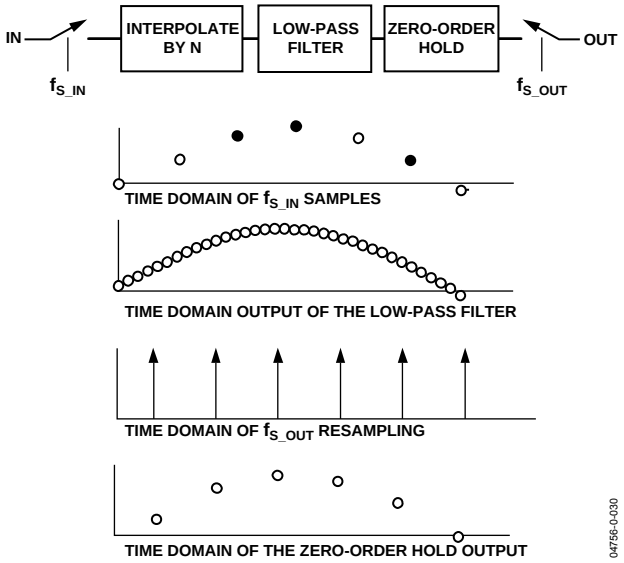

Figure 30. SRC Time Domain

In the frequency domain shown in Figure 31, the interpolation expands the frequency axis of the zero-order hold. The images from the interpolation can be sufficiently attenuated by a good low-pass filter. The images from the zero-order hold are now pushed by a factor of 2^{20} closer to the infinite attenuation point of the zero-order hold, which is $f_{S\_IN} \times 2^{20}$. The images at the zero-order hold are the determining factor for the fidelity of the output at f_{S_OUT}.

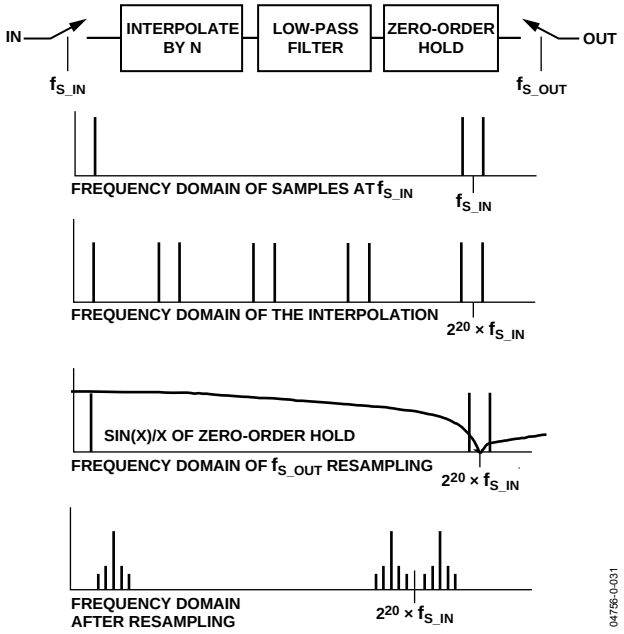

Figure 31. Frequency Domain of the Interpolation and Resampling

The worst-case images can be computed from the zero-order hold frequency response:

$$maximum\ image = \sin(\times F/f_{S\_INTERP})/(\times F/f_{S\_INTERP})$$

where:

F is the frequency of the worst-case image that would be $2^{20} \times f_{S\_IN} \pm f_{S\_IN}/2$.

f_{S_INTERP} is $f_{S\_IN} \times 2^{20}$.

The following worst-case images would appear for f_{S_IN} equal to 192 kHz:

Image at f_{S_INTERP} − 96 kHz = −125.1 dB

Image at f_{S_INTERP} + 96 kHz = −125.1 dB

Hardware Model

The output rate of the low-pass filter in Figure 30 is the interpolation rate:

$2^{20} \times 192{,}000$ kHz = 201.3 GHz

Sampling at a rate of 201.3 GHz is clearly impractical, not to mention the number of taps required to calculate each interpolated sample. However, because interpolation by 2^{20} involves zero-stuffing $2^{20}-1$ samples between each f_{S_IN} sample, most of the multiplies in the low-pass FIR filter are by zero. A further reduction can be realized, because only one interpolated sample is taken at the output at the f_{S_OUT} rate, so only one convolution needs to be performed per f_{S_OUT} period instead of 2^{20} convolutions. A 64-tap FIR filter for each f_{S_OUT} sample is sufficient to suppress the images caused by the interpolation.

One difficulty with the above approach is that the correct interpolated sample must be selected upon the arrival of f_{S_OUT}. Because there are 2^{20} possible convolutions per f_{S_OUT} period, the arrival of the f_{S_OUT} clock must be measured with an accuracy of 1/201.3 GHz = 4.96 ps. Measuring the f_{S_OUT} period with a clock of 201.3 GHz frequency is clearly impossible; instead, several coarse measurements of the f_{S_OUT} clock period are made and averaged over time.

Another difficulty with the above approach is the number of coefficients required. Because there are 2^{20} possible convolutions with a 64-tap FIR filter, there must be 2^{20} polyphase coefficients for each tap, which requires a total of 2^{26} coefficients. To reduce the number of coefficients in ROM, the SRC stores a small subset of coefficients and performs a high order interpolation between the stored coefficients.

The above approach works when $f_{S\_OUT} > f_{S\_IN}$. However, when the output sample rate, f_{S_OUT}, is less than the input sample rate, f_{S_IN}, the ROM starting address, input data, and length of the convolution must be scaled. As the input sample rate rises over the output sample rate, the antialiasing filter's cutoff frequency must be lowered, because the Nyquist frequency of the output samples is less than the Nyquist frequency of the input samples. To move the cutoff frequency of the antialiasing filter, the coefficients are dynamically altered and the length of the convolution is increased by a factor of (f_{S_IN}/f_{S_OUT}).

This technique is supported by the Fourier transform property that, if f(t) is F(ω), then f(k × t) is F(ω/k). Thus, the range of decimation is limited by the size of the RAM.

SRC Architecture

The architecture of the sample rate converter is shown in Figure 32. The sample rate converter's FIFO block adjusts the left and right input samples and stores them for the FIR filter's convolution cycle. The f_{S_IN} counter provides the write address to the FIFO block and the ramp input to the digital servo loop. The ROM stores the coefficients for the FIR filter convolution and performs a high order interpolation between the stored coefficients. The sample rate ratio block measures the sample rate for dynamically altering the ROM coefficients and scaling of the FIR filter length as well as the input data. The digital servo loop automatically tracks the f_{S_IN} and f_{S_OUT} sample rates and provides the RAM and ROM start addresses for the start of the FIR filter convolution.

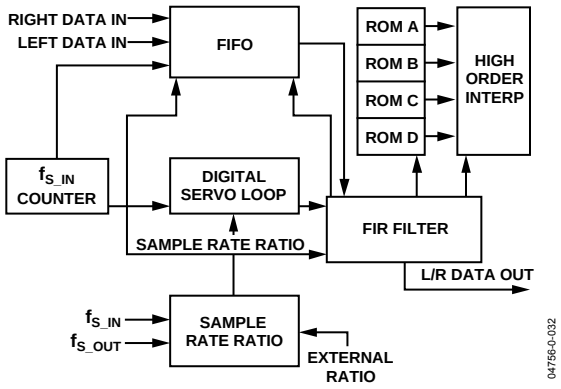

Figure 32. Architecture of the Sample Rate Converter

The FIFO receives the left and right input data and adjusts the amplitude of the data for both the soft muting of the sample rate converter and the scaling of the input data by the sample rate ratio before storing the samples in the RAM. The input data is scaled by the sample rate ratio, because, as the FIR filter length of the convolution increases, so does the amplitude of the convolution output. To keep the output of the FIR filter from saturating, the input data is scaled down by multiplying it by (f_{S_OUT}/f_{S_IN}) when $f_{S\_OUT} < f_{S\_IN}$. The FIFO also scales the input data for muting and unmuting of the SRC.

The RAM in the FIFO is 512 words deep for both left and right channels. An offset to the write address provided by the f_{S_IN} counter is added to prevent the RAM read pointer from overlapping the write address. The minimum offset on the SRC is 16 samples. However, the group delay and mute-in register can be used to increase this offset.

The number of input samples added to the write pointer of the FIFO on the SRC is 16 plus Bit 6 to Bit 0 of the group delay register. This feature is useful in varispeed applications to prevent the read pointer to the FIFO from running ahead of the write pointer. When set, Bit 7 of the group delay and mute-in register soft-mutes the sample rate. Increasing the offset of the write address pointer is useful for applications in which small changes in the sample rate ratio between f_{S_IN} and f_{S_OUT} are expected. The maximum decimation rate can be calculated from the RAM word depth and the group delay as

(512 − 16)/64 taps = 7.75

for short group delay and

(512 − 64)/64 taps = 7

for long group delay.

The digital servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter, and the ROM is the fractional part. The digital servo loop must provide excellent rejection of jitter on the f_{S_IN} and f_{S_OUT} clocks, as well as measure the arrival of the f_{S_OUT} clock within 4.97 ps. The digital servo loop also divides the fractional part of the ramp output by the ratio of f_{S_IN}/f_{S_OUT} to dynamically alter the ROM coefficients when $f_{S\_IN} > f_{S\_OUT}$.

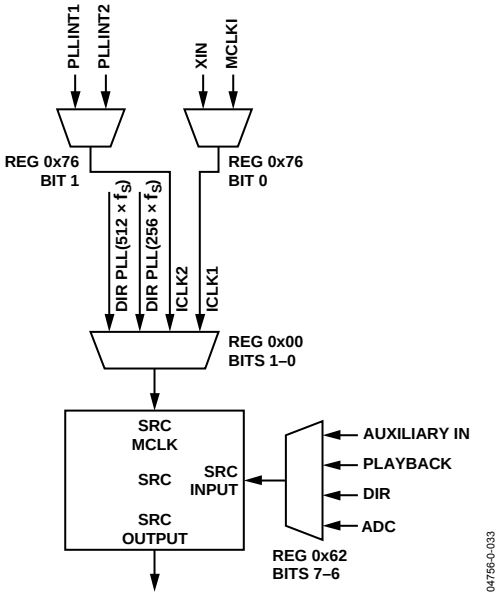

Figure 33. Clock and Datapath Control on the SCR

The digital servo loop is implemented with a multirate filter. To settle the digital servo loop filter more quickly upon startup or a change in the sample rate, a fast mode has been added to the filter. When the digital servo loop starts up or the sample rate is changed, the digital servo loop enters fast mode to adjust and settle on the new sample rate. Upon sensing that the digital servo loop is settling down to a reasonable value, the digital servo loop returns to normal (or slow) mode.

During fast mode, the MUTE_OUT bit in the sample rate error register is asserted to let the user know that clicks or pops might be present in the digital audio data. The output of the SRC can be muted by asserting Bit 7 of the group delay and mute register until the SRC has changed to slow mode. The MUTE_OUT bit can be set to generate an interrupt when the SRC changes to slow mode, indicating that the data is being sample rate converted accurately.

The frequency responses of the digital servo loop for fast mode and slow mode are shown in Figure 34. The FIR filter is a 64-tap filter when $f_{S\_OUT} \geq f_{S\_IN}$ and is $(f_{S\_IN}/f_{S\_OUT}) \times 64$ taps when $f_{S\_IN} > f_{S\_OUT}$. The FIR filter performs its convolution by loading in the starting address of the RAM address pointer and the ROM address pointer from the digital servo loop at the start of the f_{S_OUT} period. The FIR filter then steps through the RAM by decrementing its address by 1 for each tap, and the ROM pointer increments its address by the $(f_{S\_OUT}/f_{S\_IN}) \times 2^{20}$ ratio for $f_{S\_IN} > f_{S\_OUT}$ or 2^{20} for $f_{S\_OUT} \geq f_{S\_IN}$. Once the ROM address rolls over, the convolution is completed.

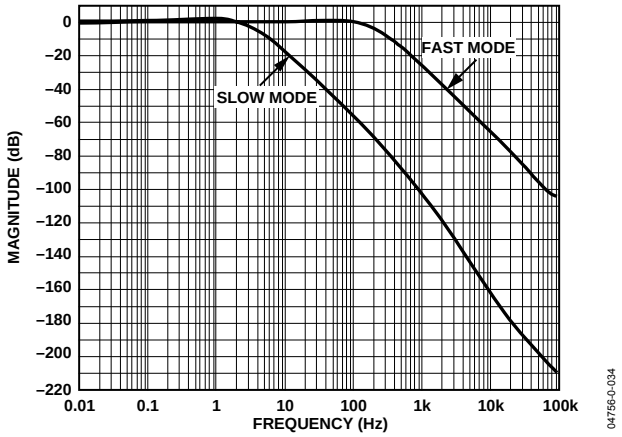

Figure 34. Frequency Response of the Digital Servo Loop. f_{S_IN} is the X-Axis, f_{S_OUT} = 192 KHz, Master Clock is 30 MHz

The convolution is performed for both the left and right channels, and the multiply accumulate circuit used for the convolution is shared between the channels. The f_{S_IN}/f_{S_OUT} sample rate ratio circuit is used to dynamically alter the coefficients in the ROM when $f_{S\_IN} > f_{S\_OUT}$. The ratio is calculated by comparing the output of an f_{S_OUT} counter to the output of an f_{S_IN} counter. If $f_{S\_OUT} > f_{S\_IN}$, the ratio is held at one. If $f_{S\_IN} > f_{S\_OUT}$, the sample rate ratio is updated, if it is different by more than two f_{S_OUT} periods from the previous f_{S_OUT} to f_{S_IN} comparison. This is done to provide some hysteresis to prevent the filter length from oscillating and causing distortion.

PLL SECTION

The ADAV803 features a dual PLL configuration to generate independent system clocks for asynchronous operation. Figure 37 shows the block diagram of the PLL section. The PLL generates the internal and system clocks from a 27 MHz clock. This clock is generated either by a crystal connected between XIN and XOUT, as shown in Figure 35, or from an external clock source connected directly to XIN. A 54 MHz clock can also be used, if the internal clock divider is used.

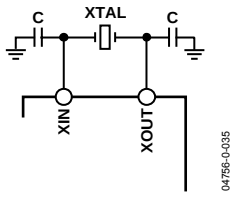

Figure 35. Crystal Connection

Both PLLs (PLL1 and PLL2) can be programmed independently and can accommodate a range of sampling rates (32/44.1/48 kHz) with selectable system clock oversampling rates of 256 and 384. Higher oversampling rates can also be selected by enabling the doubling of the sampling rate to give 512 or 768 × f_S ratios. Note that this option also allows oversampling ratios of 256 or 384 at double sample rates of 64/88.2/96 kHz.

The PLL outputs can be routed internally to act as clock sources for the other component blocks such as the ADC, DAC, and so on. The outputs of the PLLs are also available on the three SYSCLK pins. Figure 38 shows how the PLLs can be configured to provide the sampling clocks.

Table 7. PLL Frequency Selection Options

		MCLK Selection	
PLL	**Sample Rate (f_S)**	**Normal f_S**	**Double f_S**
1	32/44.1/48 kHz	256/384 × f_S	512/768 × f_S
	64/88.2/96 kHz		256/384 × f_S
2A	32/44.1/48 kHz	256/384 × f_S	512/768 × f_S
	64/88.2/96 kHz		256/384 × f_S
2B	Same as f_S selected	512 × f_S	
	For PLL 2A	512 × f_S	

The PLLs require some external components to operate correctly. These components, shown in Figure 36, form a loop filter that integrates the current pulses from a charge pump and produces a voltage that is used to tune the VCO. Good quality capacitors, such as PPS film, are recommended. Figure 37 shows a block diagram of the PLL section, including master clock selection. Figure 38 shows how the clock frequencies at the clock output pins, SYSCLK1 to SYSCLK 3, and the internal PLL clock values, PLL1 and PLL2, are selected.

The clock nodes, PLL1 and PLL2, can be used as master clocks for the other blocks in the ADAV803 such as the DAC or ADC. The PLL has separate supply and ground pins, which should be as clean as possible to prevent electrical noise from being converted into clock jitter by coupling onto the loop filter pins.

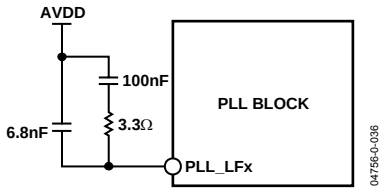

Figure 36. PLL Loop Filter

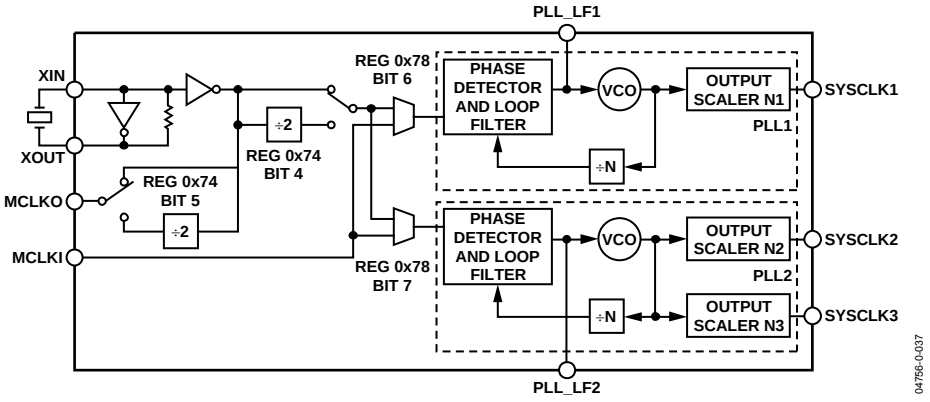

Figure 37. PLL Section Block Diagram

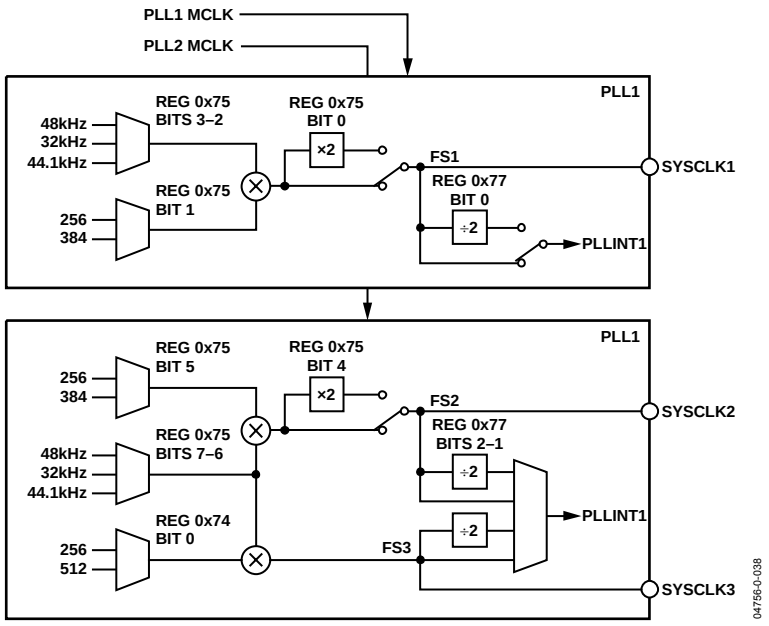

Figure 38. PLL Clocking Scheme

SPDIF TRANSMITTER AND RECEIVER

The ADAV803 contains an integrated SPDIF transmitter and receiver. The transmitter consists of a single output pin, DITOUT, on which the biphase encoded data appears. The SPDIF transmitter source can be selected from the different blocks making up the ADAV803. Additionally, the clock source for the SPDIF transmitter can be selected from the various clock sources available in the ADAV803.

The receiver uses two pins, DIRIN and DIR_LF. DIRIN accepts the SPDIF input data stream. The DIRIN pin can be configured to accept a digital input level, as defined in the Specifications section, or an input signal with a peak-to-peak level of 200 mV minimum, as defined by the IEC60958-3 specification. DIR_LF is a loop filter pin, required by the internal PLL, which is used to recover the clock from the SPDIF data stream.

The components shown in Figure 42 form a loop filter, which integrates the current pulses from a charge pump and produces a voltage that is used to tune the VCO of the clock recovery PLL. The recovered audio data and audio clock can be routed to the different blocks of the ADAV803, as required. Figure 39 shows a conceptual diagram of the DIRIN block.

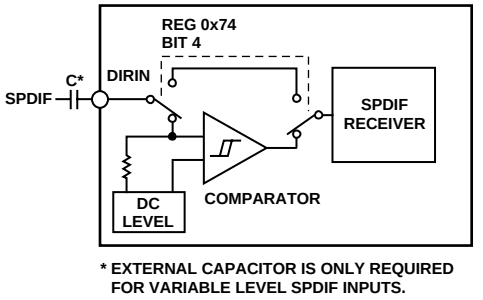

Figure 39. DIRIN Block

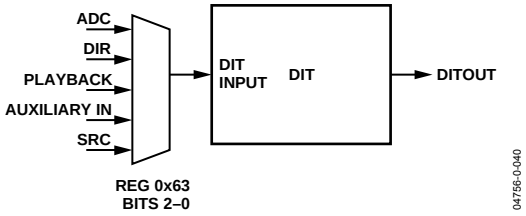

Figure 40. Digital Output Transmitter Block Diagram

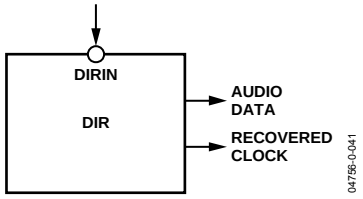

Figure 41. Digital Input Receiver Block Diagram

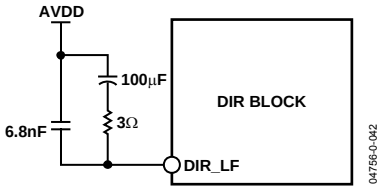

Figure 42. DIR Loop Filter Components

Serial Digital Audio Transmission Standards

The ADAV803 can receive and transmit SPDIF, AES/EBU, and IEC-958 serial streams. SPDIF is a consumer audio standard, and AES/EBU is a professional audio standard. IEC-958 has both consumer and professional definitions. This data sheet is not intended to fully define or to provide a tutorial for these standards. Contact the international standards-setting bodies for the full specifications.

All these digital audio communication schemes encode audio data and audio control information using the biphase-mark method. This encoding method minimizes the dc content of the transmitted signal. As can be seen from Figure 43, 1s in the original data end up with midcell transitions in the biphase-mark encoded data, while 0s in the original data do not. Note that the biphase-mark encoded data always has a transition between bit boundaries.

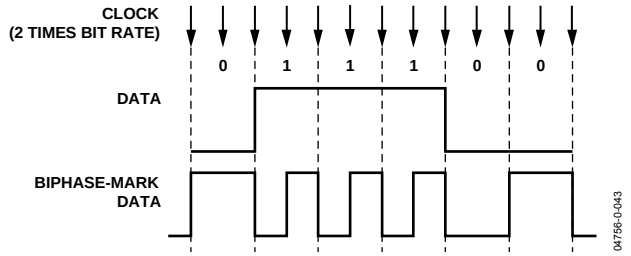

Figure 43. Biphase-Mark Encoding

Digital audio-communication schemes use preambles to distinguish among channels (called subframes) and among longer-term control information blocks (called frames). Preambles are particular biphase-mark patterns, which contain encoding violations that allow the receiver to uniquely recognize them. These patterns and their relationship to frames and subframes are shown in Table 8 and Figure 44.

Table 8. Biphase-Mark Encode Preamble

	Biphase Patterns	Channel
X	11100010 or 00011101	Left
Y	11100100 or 00011011	Right
Z	11101000 or 00010111	Left and CS block start

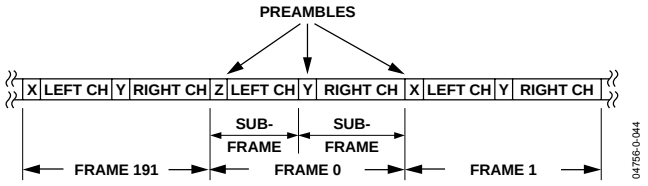

Figure 44. Preambles, Frames, and Subframes

The biphase-mark encoding violations are shown in Figure 45. Note that all three preambles include encoding violations. Ordinarily, the biphase-mark encoding method results in a polarity transition between bit boundaries.

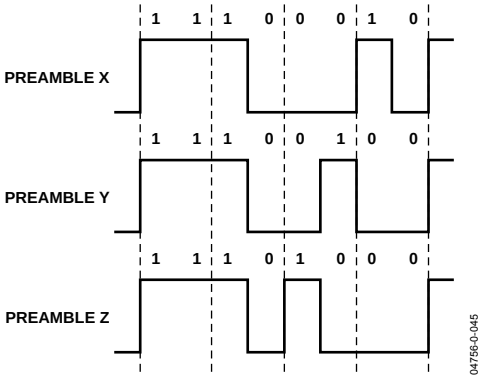

Figure 45. Preambles

The serial digital audio communication scheme is organized using a frame and subframe construction. There are two subframes per frame (ordinarily the left and right channel). Each subframe includes the appropriate 4-bit preamble, up to 24 bits of audio data, a validity (V) bit, a user (U) bit, a channel status (C) bit, and an even parity (P) bit. The channel status bits and the user bits accumulate over many frames to convey control information. The channel status bits accumulate over a 192 frame period (called a channel status block). The user bits accumulate over 1,176 frames when the interconnect is implementing the so-called subcode scheme (EIAJ CP-2401). The organization of the channel status block, frames, and subframes is shown in Table 9 and Table 10. Note that the ADAV803 supports the professional audio standard from a software point of view only. The digital interface supports only consumer mode.

Table 9. Consumer Audio Standard

	Data Bits							
Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N	Channel Status		Emphasis			Copy-right	Non-Audio	Pro/Con = 0
N + 1	Category Code							
N + 2	Channel Number					Source Number		
N + 3	Reserved		Clock Accuracy			Sampling Frequency		
N + 4	Reserved					Word Length		
N + 5 to (N + 23)	Reserved							

N = 0x20 for receiver channel status buffer.
N = 0x38 for transmitter channel status buffer.

Table 10. Professional Audio Standard

	Data Bits							
Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N	Sample Frequency		Lock	Emphasis			Non-Audio	Pro/Con = 1
N + 1	User Bit Management			Channel Mode				
N + 2	Alignment Level		Source Word Length			Use of Auxiliary Mode Sample Bits		
N + 3	Channel Identification							
N + 4	f_S Scaling	Sample Frequency (f_S)				Reserved	Digital Audio Reference Signal	
N + 5	Reserved							
N + 6	Alphanumeric Channel Origin Data—First Character							
N + 7	Alphanumeric Channel Origin Data							
N + 8	Alphanumeric Channel Origin Data							
N + 9	Alphanumeric Channel Origin Data—Last Character							
N + 10	Alphanumeric Channel Destination Data—First Character							
N + 11	Alphanumeric Channel Destination Data							
N + 12	Alphanumeric Channel Destination Data							
N + 13	Alphanumeric Channel Destination Data—Last Character							
N + 14	Local Sample Address Code—LSW							
N + 15	Local Sample Address Code							
N + 16	Local Sample Address Code							
N + 17	Local Sample Address Code—MSW							
N + 18	Time of Day Code—LSW							
N + 19	Time of Day Code							
N + 20	Time of Day Code							
N + 21	Time of Day Code—MSW							
N + 22	Reliability Flags			Reserved				
N + 23	Cyclic Redundancy Check Character (CRCC)							

N = 0x20 for receiver channel status buffer.
N = 0x38 for transmitter channel status buffer.

The standards allow the channel status bits in each subframe to be independent, but ordinarily the channel status bit in the two subframes of each frame are the same. The channel status bits are defined differently for the consumer audio standards and the professional audio standards. The 192 channel status bits are organized into 24 bytes and have the interpretations shown in Table 9 and Table 10.

The SPDIF transmitter and receiver have a comprehensive register set. The registers give the user full access to the functions of the SPDIF block, such as detecting nonaudio and validity bits, Q subcodes, preambles, and so on. The channel status bits as defined by the IEC60958 and AES3 specifications are stored in register buffers for ease of use. An autobuffering function allows channel status bits and user bits read by the receiver to be copied directly to the transmitter block, removing the need for user intervention.

Receiver Section

The ADAV803 uses a double-buffering scheme to handle reading channel status and user bit information. The channel status bits are available as a memory buffer, taking up 24 consecutive register locations. The user bits are read using an indirect memory addressing scheme, where the receiver user- bit indirect-address register is programmed with an offset to the user bit buffer, and the receiver user bit data register can be read to determine the user bits at that location. Reading the receiver user bit data register automatically updates the indirect address register to the next location in the buffer. Typically, the receiver user bit indirect-address register is programmed to zero (the start of the buffer), and the receiver user bit data register is read repeatedly until all the buffer's data has been read. Figure 46 and Figure 47 show how receiving the channel status bits and user bits is implemented.

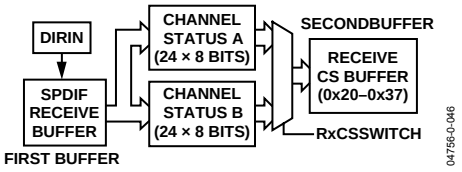

Figure 46. Channel Status Buffer

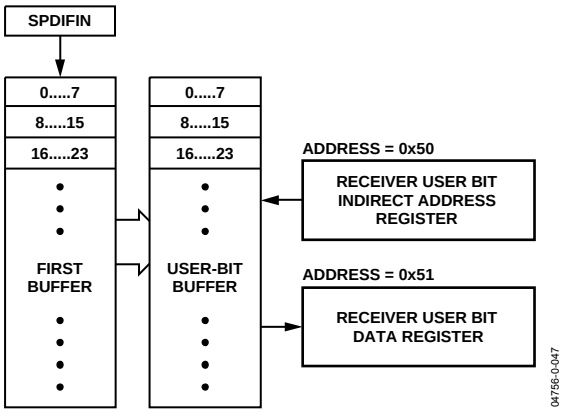

Figure 47. Receiver User Bit Buffer

The SPDIF receive buffer is updated continuously by the incoming SPDIF stream. Once all the channel status bits for the block (192 for Channel A and 192 for Channel B) are received, the bits are copied into the receiver channel status buffer. This buffer stores all 384 bits of channel status information, and the RxCSSWITCH bit in the channel status switch buffer register determines whether the Channel A or the Channel B status bits are required to be read. The receive channel status bit buffer is 24 bytes long and spans the address range from 0x20 to 0x37.

Because the channel status bits of an SPDIF stream rarely change, a software interrupt/flag bit, RxCSBINT, is provided to notify the host control that either a new block of channel status bits is available or that the first five bytes of channel status information have changed from a previous block. The function of the RxCSBINT is controlled by the RxBCONF3 bit in the receiver buffer configuration register.

The size of the user bit buffer can be set by programming the RxBCONF0 bit in the receiver buffer configuration register, as shown in Table 11.

Table 11. RxBCONF3 Functionality

RxBCONF0	Receiver User Bit Buffer Size
0	384 bits with Preamble Z as the start of the block.
1	768 bits with Preamble Z as the start of the block.

The updating of the user bit buffer is controlled by Bits RxBCONF2–1 and Bit 7 to Bit 4 of the channel status register, as shown in Table 12 and Table 13.

Table 12. RxBCONF2–1 Functionality

RxBCONF		
Bit 2	Bit 1	Receiver User Bit Buffer Configuration
0	0	User bits are ignored.
0	1	Update second buffer when first buffer is full.
1	0	Format according to Byte 1, Bit 4 to Bit 7, if PRO bit is set. Format according to IEC60958-3, if PRO bit is clear.

Table 13. Automatic User Bit Configuration

Bits				Automatic Receiver User Bit Buffer
7	6	5	4	Configuration
0	0	0	0	User bits are ignored.
0	1	0	0	AES-18 format: the user bit buffer is treated in the same way as when RxBCONF2–1 = 0b01.
1	0	0	0	User bit buffer is updated in the same way as when RxBCONF2–1 = 0b01 and RxBCONF0 = 0b00.
1	1	0	0	User-defined format: the user bit buffer is treated in the same way as when RxBCONF2–1 = 0b01.

When the user bit buffer has been filled, the RxUBINT interrupt bit in the interrupt status register is set, provided that the RxUBINT mask bit is set, to indicate that the buffer has new information and can be read.

For the special case when the user data is formatted according to the IEC60958-3 standard into messages made of information units, called IUs, the zeros stuffed between each IU and each message are removed and only the IUs are stored. Once the end of the message is sensed by more that eight zeros between IUs, the user bit buffer is updated with the complete message and the first buffer begins looking for the start of the next message.

Each IU is stored as a byte consisting of 1, Q, R, S, T, U, V, and W bits (see the IEC60958-3 specification for more information). When 96 IUs are received, the Q subcode of the IUs is stored in the Q subcode buffer, consisting of 10 bytes. The Q subcode is the Q bits taken from each of the 96 IUs. The first 10 bytes (80 bits) of the Q subcode contain information sent by CD, MD, and DAT systems. The last 16 bits of the Q subcode are used to perform a CRC check of the Q subcode. If an error occurs in the CRC check of the Q subcode, the QCRCERROR bit is set. This is a sticky bit that remains high until the register is read.

Transmitter Operation

The SPDIF transmitter has a similar buffer structure to the receive section. The transmitter channel status buffer occupies 24 bytes of the register map. This buffer is long enough to store the 192 bits required for one channel of channel status information. Setting the TxCSSWITCH bit determines if the data loaded to the transmitter channel status buffer is intended for Channel A or Channel B. In most cases, the channel status bits for Channel A and Channel B are the same, in which case setting the Tx_A/B_Same bit reads the data from the transmitter channel status buffer and transmits it on both channels.

Because the channel status information is rarely changed during transmission, the information contained in the buffer is transmitted repeatedly. The Disable_Tx_Copy bit can be used to prevent the channel status bits from being copied from the transmitter CS buffer into the SPDIF transmitter buffer until the user has finished loading the buffers. This feature is typically used, if the Channel A data and Channel B data are different. Setting the bit prevents the data from being copied. Clearing the bit allows the data to be copied and then transmitted. Figure 48 shows how the buffers are organized.

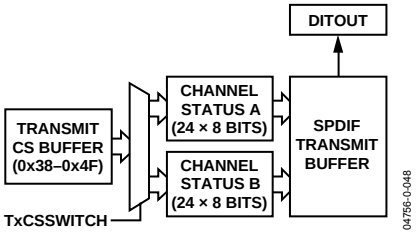

Figure 48. Transmitter Channel Status Buffer

As with the receiver section, the transmitted user bits are also double-buffered. This is required, because, unlike the channel status bits, the user bits do not necessarily repeat themselves. The user bits can be buffered in various configurations, as listed in Table 14. Transmission of the user bits is determined by the state of the BCONF3 bit. If the bit is 0, the user bits begin transmitting right away without alignment to the Z preamble. If this bit is 1, the user bits do not start transmitting until a Z preamble occurs when the TxBCONF2–1 bits are 01.

Table 14. Transmitter User Bit Buffer Configurations

TxBCONF2-1		
Bit 2	Bit 1	Transmitter User Bit Buffer Configuration
0	0	Zeros are transmitted for the user bits.
0	1	Host writes user bits to the buffer until it is full.
1	0	Writes the user bits to the buffer in IUs specified by IEC60958-3 and transmits them according to the standard.
1	1	First 10 bytes of the user-bit buffer are configured to store a Q subcode.

Table 15. Transmitter User Bit Buffer Size

TxBCONF0	Buffer Size
0	384 bits with Preamble Z as the start of the block.
1	768 bits with Preamble Z as the start of the block.

By using sticky bits and interrupts, the transmit buffers can notify the host or microcontroller when the first user bit buffer has been updated and when the second transmit user bit buffer is full. The sticky bit, TxUBINT, is set when the transmit user bit buffer has been updated and the second transmit user bit buffer is ready to accept new user bits. The sticky bit, TxFBINT, is set whenever the second transmit user bit buffer is full. Any new writes to this buffer are ignored until the first transmit buffer is updated. These two bits are located in the interrupt status register. When the host reads the interrupt status register, these bits are cleared. Interrupts for the TxUBINT and TxFBINT sticky bits can be enabled by setting the TxUBMASK and TxFBMASK bits, respectively, in the interrupt status mask register.

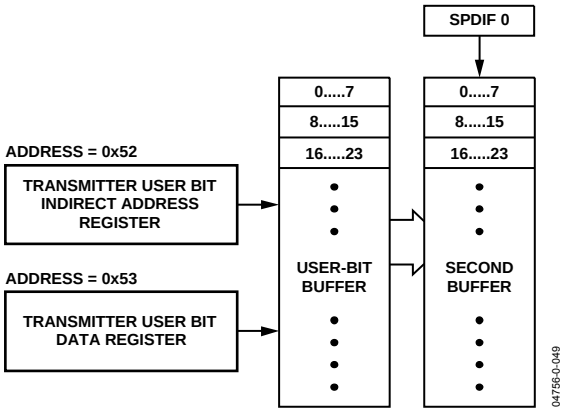

Figure 49. Transmitter User Bit Buffer

Autobuffering

The ADAV803 SPDIF receiver and transmitter sections have an autobuffering mode allowing the channel status and user bits to be copied automatically from the receiver to the transmitter without user intervention. The channel status and user bits can be independently selected for autobuffering using the Auto_CSBits and Auto_UBits bits, respectively, in the autobuffer register. When the receiver and transmitter are running at the same sample rate, the transmitted channel status and user bits are the same as the received channel-status and user bits.

In many systems, however, it is likely that the receiver and transmitter are not running at the same frequency. When the transmitter sample rate is higher than the receiver sample rate, the channel status and user bit block is sometimes repeated. When the transmitter sample rate is lower than the receiver sample rate, the channel status and user bit blocks might be dropped. Because the first five bytes of the channel status are typically constant, they can be repeated or dropped with no information loss. However, if the PRO bit in the channel status is set and the local sample address code and time-of-day code bytes contain information, these bytes might be repeated or dropped, in which case information can be lost. It is up to the user to determine how to handle this case.

When the user bits are transmitted according to the IEC60958-3 format, the messages contained in the user bits can still be sent without dropping or repeating messages. Because zero-stuffing is allowed between IUs and messages, zeros can be added or subtracted to preserve the messages. When the transmitter sample rate is greater than the receiver sample rate, extra zeros are stuffed between the messages. When the sample rate of the transmitter is less than the sample rate of the receiver, the zeros stuffed between the messages are subtracted. If there are not enough zeros between the messages to be subtracted, the zeros between IUs are subtracted as well. The Zero_Stuff_IU bit in the autobuffer register enables the adding or subtracting of zeros between messages.

Interrupts

The ADAV803 provides interrupt bits to indicate the presence of certain conditions that require attention. Reading the interrupt status register allows the user to determine if any of the interrupts have been asserted. The bits of the interrupt status register remain high, if set, until the register is read. Two bits, SRCError and RxError, indicate interrupt conditions in the sample rate converter and an SPDIF receiver error, respectively. Both these conditions require a read of the appropriate error register to determine the exact cause of the interrupt.

Each interrupt in the interrupt status register has an associated mask bit in the interrupt status mask register. The interrupt mask bit must be set for the corresponding interrupt to be generated. This feature allows the user to determine which functions should be responded to.

The dual function pin ZEROL/INT can be set to indicate the presence of no audio data on the left channel or the presence of an interrupt set in the interrupt status register. As shown in Table 16, the function of this pin is selected by the INTRPT bit in DAC Control Register 4.

Table 16. ZEROL/INT Pin Functionality

INTRPT	Pin Functionality
0	Pin functions as a ZEROL flag pin.
1	Pin functions as an interrupt pin.

SERIAL DATA PORTS

The ADAV803 contains four flexible serial ports (SPORTs) to allow data transfer to and from the codec. All four SPORTs are independent and can be configured as master or slave ports. In slave mode, the xLRCLK and xBCLK signals are inputs to the serial ports. In master mode, the serial port generates the xLRCLK and xBCLK signals. The master clock for the SPORT can be selected from a number of sources, as shown in Figure 50.

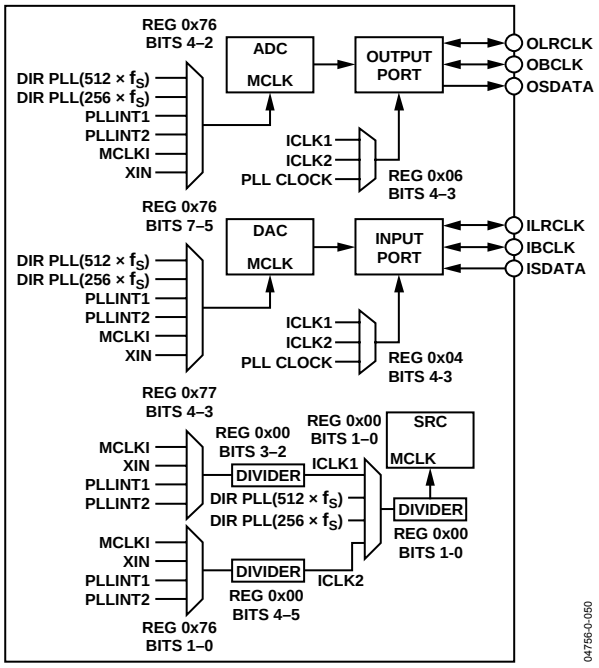

Figure 50. SPORT Clocking Scheme

Care should be taken to ensure that the clock rate is appropriate for whatever block is connected to the serial port. For example, if the ADC is running from the MCLKI input at 256 × f_S, then the master clock for the SPORT should also run from the MCLKI input to ensure that the ADC and serial port are synchronized.

The SPORTs can be set to transmit or receive data in I²S, left-justified or right-justified formats with different word lengths by programming the appropriate bits in the playback register, auxiliary input port register, record register, and auxiliary output port-control register. Figure 51 is a timing diagram of the serial data port formats.

Clocking Scheme

The ADAV803 provides a flexible choice of on-chip and off-chip clocking sources. The on-chip oscillator with dual PLLs is intended to offer complete system clocking requirements for use with available MPEG encoders, decoders, or a combination of codecs. The oscillator function is designed for generation of a 27 MHz video clock from a 27 MHz crystal connected between the XIN and XOUT pins. Capacitors must also be connected between these pins and DGND, as shown in Figure 35. The capacitor values should be specified by the crystal manufacturer. A square wave version of the crystal clock is output on the MCLKO pin. If the system has a 27 MHz clock available, this clock can be connected directly to the XIN pin.

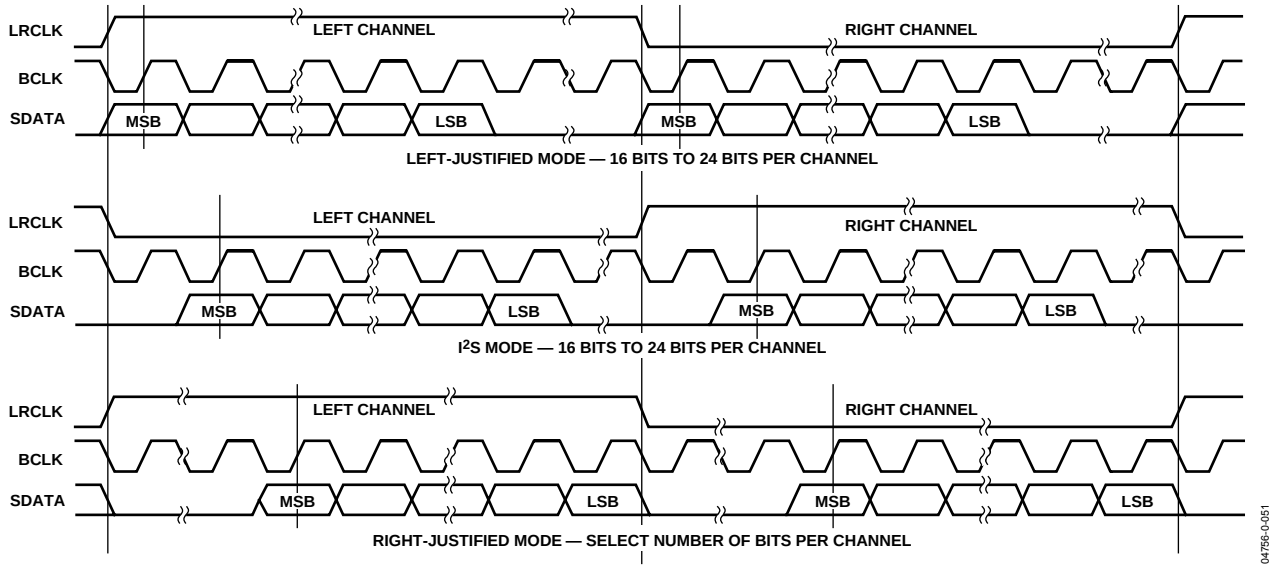

Figure 51. Serial Data Modes

Datapath

The ADAV803 features a digital input/output switching/ multiplexing matrix that gives flexibility to the range of possible input and output connections. Digital input ports include playback and auxiliary input (both 3-wire digital), and S/PDIF (single-wire to the on-chip receiver). Output ports include the record and auxiliary output ports (both 3-wire digital) and the S/PDIF port (single-wire from the on-chip transmitter). Internally, the DIR and DIT are interfaced via 3-wire interfaces. The datapath for each input and output port is selected by programming Datapath Control Registers 1 and 2. Figure 52 shows the internal datapath structure of the ADAV803.

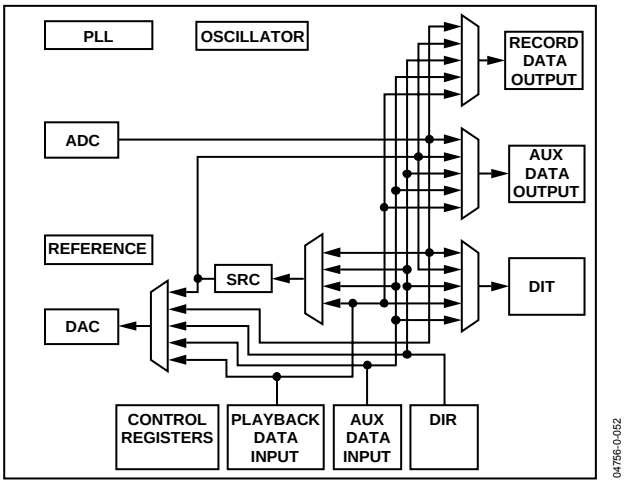

Figure 52. Datapath

INTERFACE CONTROL

The ADAV803 has a dedicated control port to allow the internal registers of the ADAV803 to be accessed. Each of the internal registers is eight bits wide. Where bits are described as reserved (RES), these bits should be programmed as zero.

I²C INTERFACE

The I²C interface of the ADAV803 is a 2-wire interface consisting of a clock line, SCL, and a data line, SDA. SDA is bidirectional; the ADAV803 drives SDA to either acknowledge the master, ACK, or send data during a read operation. The SDA pin for the I²C port is an open-drain collector that requires a 1 kΩ pull-up resistor. A write or read access occurs when the SDA line is pulled low while the SCL line is high, indicated by START in the timing diagrams. SDA is allowed to change only when SCL is low, except when a start or stop condition occurs, as shown in Figure 53 and Figure 54. The I²C interface supports both standard (100 kbps) and fast (400 kbps) modes as defined by the I²C standards.

The first eight bits of the access consist of the device address and the R/W bit. The device address consists of an internal built-in address (0b00100) and two address pins, AD1 and AD0. The two address pins allow up to four ADAV803s to be used in a system.

Initiating a write operation to the ADAV803 involves sending a start condition and then sending the device address with the R/W set low. The ADAV803 responds by issuing an ACK to indicate that it has been addressed. The user then sends a second frame telling the ADAV803 which register is required to be written to. The 7-bit register address is left-shifted to make the eight bits that the frame requires. Another ACK is issued by the ADAV803. Finally the user can send another frame with the eight data bits required to be written to the register. A third ACK is issued by the ADAV803, after which the user can send a stop condition to complete the data transfer.

A read operation requires that the user first write to the ADAV803 to point to the correct register and then read the data. This is achieved by sending a start condition followed by the device address frame, with R/W low, and then the register address frame. Following the ACK from the ADAV803, the user must issue a repeated start condition. This is identical to a start condition. The next frame is the device address with R/W set high. On the next frame, the ADAV803 outputs the register data on the SDA line. A stop condition completes the read operation. Figure 53 and Figure 54 show examples of writing to and reading from the DAC left volume register (Address 0b1101000).

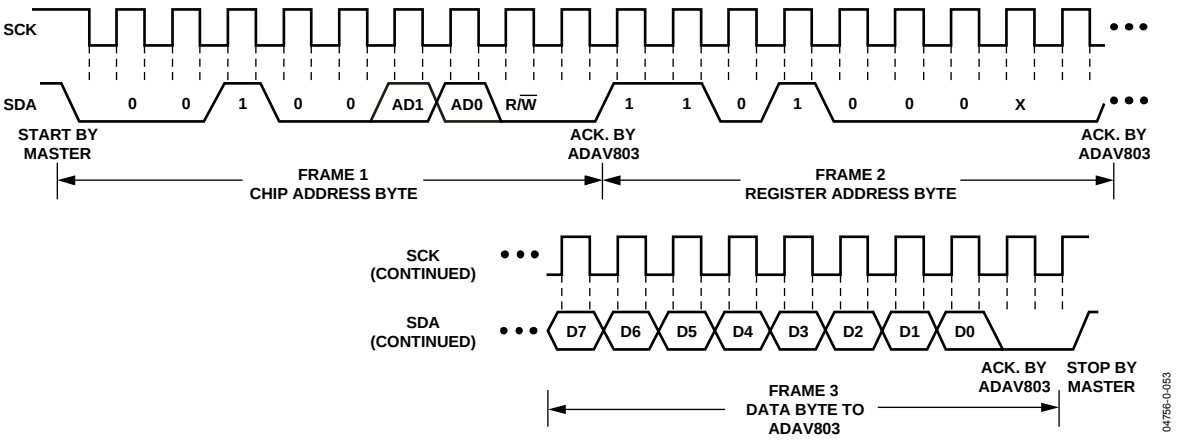

Figure 53. Writing to the DAC Left Volume Register in I²C

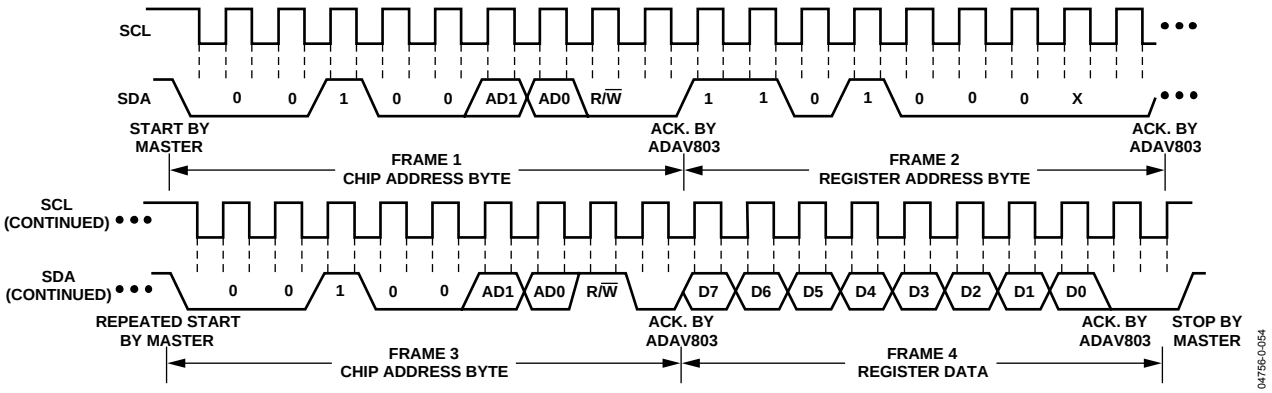

Figure 54. Reading from the DAC Left Volume Register in I²C

BLOCK READS AND WRITES

The ADAV803 provides the user with the ability to write to or read from a block of registers in one continuous operation. To use this feature, the user has to continue providing data frames before the stop condition. For a write operation, the register address is automatically incremented with each additional frame and the register data is written to that register address. For a read operation, the register address is automatically incremented with each additional frame, and the register data is clocked out on that frame.

Care should be exercised when using the block read or block write modes. For most cases, block reading or writing to a register automatically increments the register address to point to the next register. The exceptions to this case are the indirect memory address registers, transmitter user bit and receiver user bit data buffers. Using a block read or write to access these registers does not update the absolute register address, but instead updates the buffer address to provide the next value in the buffer.

REGISTER DESCRIPTIONS

Table 17. SRC and Clock Control Register

	SRCDIV1	SRCDIV0	CLK2DIV1	CLK2DIV0	CLK1DIV1	CLK1DIV0	MCLKSEL1	MCLKSEL0
	7	6	5	4	3	2	1	0
ADDRESS = 0000000 (0x00)								
SRCDIV1–0	Divides the SRC master clock. 00 = SRC master clock is not divided. 01 = SRC master clock is divided by 1.5. 10 = SRC master clock is divided by 2. 11= SRC master clock is divided by 3.							
CLK2DIV1–0	Clock divider for Internal Clock 2 (ICLK2). 00 = Divide by 1. 01 = Divide by 1.5. 10 = Divide by 2. 11 = Divide by 3.							
CLK1DIV1–0	Clock divider for Internal Clock 1 (ICLK1). 00 = Divide by 1. 01 = Divide by 1.5. 10 = Divide by 2. 11 = Divide by 3.							
MCLKSEL1–0	Clock selection for the SRC master clock. 00 = Internal Clock 1. 01 = Internal Clock 2. 10 = PLL recovered clock ($512 \times f_S$). 11 = PLL recovered clock ($256 \times f_S$).							

Table 18. SPDIF Loopback Control Register

	RES	RES	RES	RES	RES	RES	RES	TxMUX
	7	6	5	4	3	2	1	0
ADDRESS = 0000011 (0x03)								
TxMUX	Selects the source for SPDIF output (DITOUT). 0 = SPDIF transmitter, normal mode. 1 = DIRIN, loopback mode.							

Table 19. Playback Port Control Register

	RES	RES	RES	CLKSRC1	CLKSRC0	SPMODE2	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000100 (0x04)								
CLKSRC1–0	Selects the clock source for generating the ILRCLK and IBCLK. 00 = Input port is a slave. 01 = Recovered PLL clock. 10 = Internal Clock 1. 11 = Internal Clock 2.							
SPMODE2–0	Selects the serial format of the playback port. 000 = Left-justified. 001 = I^2S. 100 = 24-bit, right-justified. 101 = 20-bit, right-justified. 110 = 18-bit, right-justified. 111 = 16-bit, right-justified.							

Table 20. Auxiliary Input Port Register

	RES	RES	RES	CLKSRC1	CLKSRC0	SPMODE2	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000101 (0x05)								
CLKSRC1–0	Selects the clock source for generating the IAUXLRCLK and IAUXBCLK. 00 = Input port is a slave. 01 = Recovered PLL cock. 10 = Internal Clock 1. 11 = Internal Clock 2.							
SPMODE2–0	Selects the serial format of auxiliary input port. 000 = Left-justified. 001 = I²S. 100 = 24-bit, right-justified. 101 = 20-bit, right-justified. 110 = 18-bit, right-justified. 111 = 16-bit, right-justified.							

Table 21. Record Port Control Register

	RES	RES	CLKSRC1	CLKSRC0	WLEN1	WLEN0	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000110 (0x06)								
CLKSRC1–0	Selects the clock source for generating the OLRCLK and OBCLK. 00 = Record port is a slave. 01 = Recovered PLL clock. 10 = Internal Clock 1. 11 = Internal Clock 2.							
WLEN1–0	Selects the serial output word length. 00 = 24 bits. 01 = 20 bits. 10 = 18 bits. 11 = 16 bits.							
SPMODE1–0	Selects the serial format of the record port. 00 = Left-justified. 01 = I²S. 10 = Reserved. 11 = Right-justified.							

Table 22. Auxiliary Output Port Register

	RES	RES	CLKSRC1	CLKSRC0	WLEN1	WLEN0	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000111 (0x07)								
CLKSRC1–0	Selects the clock source for generating the OAUXLRCLK and OAUXBCLK. 00 = Auxiliary record port is a slave. 01 = Recovered PLL clock. 10 = Internal Clock 1. 11 = Internal Clock 2.							
WLEN1–0	Selects the serial output word length. 00 = 24 bits. 01 = 20 bits. 10 = 18 bits. 11 = 16 bits.							
SPMODE1–0	Selects the serial format of the auxiliary record port. 00 = Left-justified. 01 = I^2S. 10 = Reserved. 11 = Right-justified.							

Table 23. Group Delay and Mute Register

	MUTE_SRC	GRPDLY6–0
	7	6, 5, 4, 3, 2, 1, 0
ADDRESS = 0001000 (0x08)		
MUTE_SRC	Soft-mutes the output of the sample rate converter. 0 = No mute. 1 = Soft-mute.	
GRPDLY6–0	Adds delay to the sample rate converter FIR filter by GRPDLY6–0 input samples. 0000000 = No delay. 0000001 = 1 sample delay. 0000010 = 2 sample delay. 1111110 = 126 sample delay. 1111111 = 127 sample delay.	

Table 24. Receiver Configuration 1 Register

	NOCLOCK	RxCLK1–0	AUTO_ DEEMPH	ERR1–0	LOCK1–0
	7	6, 5	4	3, 2	1, 0
ADDRESS = 0001001 (0x09)					
NOCLOCK	Selects the source of the receiver clock when the PLL is not locked. 0 = Recovered PLL clock is used. 1 = ICLK1 is used.				
RxCLK1–0	Determines the oversampling ratio of the recovered receiver clock. 00 = RxCLK is a 128 × f_S recovered clock. 01 = RxCLK is a 256 × f_S recovered clock. 10 = RxCLK is a 512 × f_S recovered clock. 11 = Reserved.				
AUTO_DEEMPH	Automatically de-emphasizes the data from the receiver based on the channel status information. 0 = Automatic de-emphasis is disabled. 1 = Automatic de-emphasis is enabled.				
ERR1–0	Defines what action the receiver should take, if the receiver detects a parity or biphase error. 00 = No action is taken. 01 = Last valid sample is held. 10 = Invalid sample is replaced with zeros. 11 = Reserved.				
LOCK1–0	Defines what action the receiver should take, if the PLL loses lock. 00 = No action is taken. 01 = Last valid sample is held. 10 = Zeros are sent out after the last valid sample. 11 = Soft-mute of the last valid audio sample.				

Table 25. Receiver Configuration 2 Register

	RxMUTE	SP_PLL	SP_PLL_ SEL1–0	RES	RES	NO NONAUDIO	NO_VALIDITY
	7	6	5, 4	3	2	1	0
ADDRESS = 0001010 (0x0A)							
RxMUTE	Hard-mutes the audio output for the AES3/SPDIF receiver. 0 = AES3/SPDIF receiver is not muted. 1 = AES3/SPDIF receiver is muted.						
SP_PLL	AES3/SPDIF receiver PLL accepts a left/right clock from one of the four serial ports as the PLL reference clock. 0 = Left/right clock generated from the AES3/SPDIF preambles is the reference clock to the PLL. 1 = Left/right clock from one of the serial ports is the reference clock to the PLL.						
SP_PLL_SEL1–0	Selects one of the four serial ports as the reference clock to the PLL when SP_PLL is set. 00 = Playback port is selected. 01 = Auxiliary input port is selected. 10 = Record port is selected. 11 = Auxiliary output port is selected.						
NO NONAUDIO	When the NONAUDIO bit is set, data from the AES3/SPDIF receiver is not allowed into the sample rate converter (SRC). If the NONAUDIO data is due to DTS, AAC, and so on, as defined by the IEC61937 standard, then the data from the AES3/SPDIF receiver is not allowed into the SRC regardless of the state of this bit. 0 = AES3/SPDIF receiver data is sent to the SRC. 1 = Data from the AES3/SPDIF receiver is not allowed into the SRC, if the NONAUDIO bit is set.						
NO_VALIDITY	When the VALIDITY bit is set, data from the AES3/SPDIF receiver is not allowed into the SRC. 0 = AES3/SPDIF receiver data is sent to the SRC. 1 = Data from the AES3/SPDIF receiver is not allowed into the SRC, if the VALIDITY bit is set.						

Table 26. Receiver Buffer Configuration Register

	RES	RES	RxBCONF5	RxBCONF4	RxBCONF3	RxBCONF2–1	RxBCONF0
	7	6	5	4	3	2, 1	0
ADDRESS = 0001011 (0x0B)							
RxBCONF5	If the user bits are formatted according to the IEC60958-3 standard and the DAT category is detected, the user bit interrupt is enabled only when there is a change in the start (ID) bit. 0 = User bit interrupt is enabled in normal mode. 1 = If the DAT category is detected, the user bit interrupt is enabled only if there is a change in the start (ID) bit.						
RxBCONF4	This bit determines whether Channel A and Channel B user bits are stored in the buffer together or separated between A and B. 0 = User bits are stored together. 1 = User bits are stored separately.						
RxBCONF3	Defines the function of RxCSBINT. 0 = RxCSBINT are set when a new block of receiver channel status is read, which is 192 audio frames. 1 = RxCSBINT is set only if the first five bytes of the receiver channel status block changes from the previous channel status block.						
RxBCONF2–1	Defines the user bit buffer. 00 = User bits are ignored. 01 = Updates the second user bit buffer when the first user bit buffer is full. 10 = Formats the received user bits according to Byte 1, Bit 4 to Bit 7, of the channel status, if the PRO bit is set. If the PRO bit is not set, formats the user bits according to the IEC60958-3 standard. 11 = Reserved.						
RxBCONF0	Defines the user bit buffer size, if RxBCONF2–1 = 01. 0 = 384 bits with Preamble Z as the start of the buffer. 1 = 768 bits with Preamble Z as the start of the buffer.						

Table 27. Transmitter Control Register

	RES	TxVALIDITY	TxRATIO2–0	TxCLKSEL1–0	TxENABLE
	7	6	5, 4, 3	2, 1	0
ADDRESS = 0001100 (0x0C)					
TxVALIDITY	This bit is used to set or clear the VALIDITY bit in the AES3/SPDIF transmit stream. 0 = Audio is suitable for D/A conversion. 1 = Audio is not suitable for D/A conversion.				
TxRATIO2–0	Determines the AES3/SPDIF transmitter to AES3/SPDIF receiver ratio. 000 = Transmitter to receiver ratio is 1:1. 001 = Transmitter to receiver ratio is 1:2. 010 = Transmitter to receiver ratio is 1:4. 101 = Transmitter to receiver ratio is 2:1. 110 = Transmitter to receiver ratio is 4:1.				
TxCLKSEL1–0	Selects the clock source for the AES3/SPDIF transmitter. 00 = Internal Clock 1 is the clock source for the transmitter. 01 = Internal Clock 2 is the clock source for the transmitter. 10 = Recovered PLL clock is the clock source for the transmitter. 11 = Reserved.				
TxENABLE	Enables the AES3/SPDIF transmitter. 0 = AES3/SPDIF transmitter is disabled. 1 = AES3/SPDIF transmitter is enabled.				

Table 28. Transmitter Buffer Configuration Register

	IU_Zeros3–0	TxBCONF3	TxBCONF2–1	TxBCONF0
	7, 6, 5, 4	3	2, 1	0
ADDRESS = 0001101 (0x0D)				
IU_Zeros3–0	Determines the number of zeros to be stuffed between IUs in a message up to a maximum of 8. 0000 = 0. 0001 = 1. … 0111 = 7. 1000 = 8.			
TxBCONF3	Transmitter user bits can be stored in separate buffers or stored together. 0 = User bits are stored together. 1 = User bits are stored separately.			
TxBCONF2–1	Configures the transmitter user bit buffer. 00 = Zeros are transmitted for the user bits. 01 = Transmitter user bit buffer size is configured according to TxBCONF0. 10 = User bits are written to the transmit buffer in IUs specified by the IEC60958-3 standard. 11 = Reserved.			
TxBCONF0	Determines the buffer size of the transmitter user bits when TxBCONF2–1 is 01. 0 = 384 bits with Preamble Z as the start of the buffer. 1 = 768 bits with Preamble Z as the start of the buffer.			

Table 29. Channel Status Switch Buffer and Transmitter

	RES	RES	Tx_A/B_Same	Disable_Tx_Copy	RES	RES	TxCSSWITCH	RxCSSWITCH
	7	6	5	4	3	2	1	0
ADDRESS = 0001110 (0x0E)								
Tx_A/B_Same	Transmitter Channel Status A and B are the same. The transmitter reads only from the Channel Status A buffer and places the data into the Channel Status B buffer. 0 = Channel status for A and B are separate. 1 = Channel status for A and B are the same.							
Disable_Tx_Copy	Disables the copying of the channel status bits from the transmitter channel status buffer to the SPDIF transmitter buffer. 0 = Copying transmitter channel status is enabled. 1 = Copying transmitter channel status is disabled.							
TxCSSWITCH	Toggle switch for the transmit channel status buffer. 0 = 24-byte Transmitter Channel Status A buffer can be accessed at address locations 0x38 through 0x4F. 1 = 24-byte Transmitter Channel Status B buffer can be accessed at address locations 0x38 through 0x4F.							
RxCSSWITCH	Toggle switch for the receive channel status buffer. 0 = 24-byte Receiver Channel Status A buffer can be accessed at address locations 0x20 through 0x37. 1 = 24-byte Receiver Channel Status B buffer can be accessed at address locations 0x20 through 0x37.							

Table 30. Transmitter Message Zeros Most Significant Byte

	MSBZeros7–0
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0001111 (0x0F)	
MSBZeros7–0	Most significant byte of the number of zeros to be stuffed between IEC60958-3 messages (packets). Default = 0x00.

Table 31. Transmitter Message Zeros Least Significant Byte

	LSBZeros7–0
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010000 (0x10)	
LSBZeros7–0	Least significant byte of the number of zeros to be stuffed between IEC60958-3 messages (packets). Default = 0x09.

Table 32. Autobuffer Register

	RES	Zero_Stuff_IU	Auto_UBits	Auto_CSBits	IU_Zeros3–0
	7	6	5	4	3, 2, 1, 0
ADDRESS = 0010001 (0x11)					
Zero_Stuff_IU	Enables the addition or subtraction of zeros between IUs during autobuffering of the user bits in IEC60958-3 format. 0 = No zeros added or subtracted. 1 = Zeros can be added or subtracted between IUs.				
Auto_UBits	Enables the user bits to be autobuffered between the AES3/SPDIF receiver and transmitter. 0 = User bits are not autobuffered. 1 = User bits are autobuffered.				
Auto_CSBits	Enables the channel status bits to be autobuffered between the AES3/SPDIF receiver and transmitter. 0 = Channel status bits are not autobuffered. 1 = Channel status bits are autobuffered.				
IU_Zeros3–0	Sets the maximum number of zero-stuffing to be added between IUs while autobuffering up to a maximum of 8. 0000 = 0. 0001 = 1. … 0111 = 7. 1000 = 8.				

Table 33. Sample Rate Ratio MSB Register (Read Only)

	RES	SRCRATIO14–SRCRATIO08
	7	6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010010 (0x12)		
SRCRATIO14–08	Seven most significant bits of the15-bit sample rate ratio.	

Table 34. Sample Rate Ratio LSB Register (Read Only)

	SRCRATIO07–SRCRATIO00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010011 (0x13)	
SRCRATIO07–00	Eight least significant bits of the15-bit sample rate ratio.

Table 35. Preamble-C MSB Register (Read Only)

	PRE_C15–PRE_C08
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010100 (0x14)	
PRE_C15–08	Eight most significant bits of the 16-bit Preamble-C, when nonaudio data is detected according to the IEC60937 standard; otherwise, bits show zeros.

Table 36. Preamble-C LSB Register (Read Only)

	PRE_C07–PRE_C00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010101 (0x15)	
PRE_C07–00	Eight least significant bits of the 16-bit Preamble-C, when nonaudio data is detected according to the IEC60937 standard; otherwise, bits show zeros.

Table 37. Preamble-D MSB Register (Read Only)

	PRE_D15–PRE_D08
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010110 (0x16)	
PRE_D15–08	Eight most significant bits of the 16-bit Preamble-D, when nonaudio data is detected according to the IEC60937 standard; otherwise, bits show zeros. When subframe nonaudio is used, this becomes the eight most significant bits of the 16-bit Preamble-C of Channel B.

Table 38. Preamble-D LSB Register (Read Only)

	PRE_D07–PRE_D00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0010111 (0x17)	
PRE_D07–00	Eight least significant bits of the 16-bit Preamble-D, when nonaudio data is detected according to the IEC60937 standard; otherwise, bits show zeros. When subframe nonaudio is used, this becomes the eight most significant bits of the 16-bit Preamble-C of Channel B.

Table 39. Receiver Error Register (Read Only)

	RxValidity	Emphasis	NonAudio	NonAudio Preamble	CRCError	NoStream	BiPhase/ Parity	Lock
	7	6	5	4	3	2	1	0
ADDRESS = 0011000 (0x18)								
RxValidity	This is the VALIDITY bit in the AES3 received stream.							
Emphasis	This bit is set, if the audio data is pre-emphasized. Once it has been read, it remains high and does not generate an interrupt unless it changes state.							
NonAudio	This bit is set, when Channel Status Bit 1 (nonaudio) is set. Once it has been read, it does not generate another interrupt unless the data becomes audio or the type of nonaudio data changes.							
NonAudio Preamble	This bit is set, if the audio data is nonaudio due to the detection of a preamble. The nonaudio preamble type register indicates what type of preamble was detected. Once read, it remains in its state and does not generate an interrupt unless it changes state.							
CRCError	This bit is the error flag for the channel status CRCError check. This bit does not clear until the receiver error register is read.							
NoStream	This bit is set, if there is no AES3/SPDIF stream present at the AES3/SPDIF receiver. Once read, it remains high and does not generate an interrupt unless it changes state.							
BiPhase/Parity	This bit is set, if a biphase or parity error occurred in the AES3/SPDIF stream. This bit is not cleared until the register is read.							
Lock	This bit is set, if the PLL has locked or cleared when the PLL loses lock. Once read, it remains in its state and does not generate an interrupt unless it changes state.							

Table 40. Receiver Error Mask Register

	RxValidity Mask	Emphasis Mask	NonAudio Mask	NonAudio Preamble Mask	CRCError Mask	NoStream Mask	BiPhase/ Parity Mask	Lock Mask
	7	6	5	4	3	2	1	0
ADDRESS = 0011001 (0x19)								

RxValidity Mask	Masks the RxValidity bit from generating an interrupt. 0 = RxValidity bit does not generate an interrupt. 1 = RxValidity bit generates an interrupt.
Emphasis Mask	Masks the emphasis bit from generating an interrupt. 0 = Emphasis bit does not generate an interrupt. 1 = Emphasis bit generates an interrupt.
NonAudio Mask	Masks the NonAudio bit from generating an interrupt. 0 = NonAudio bit does not generate an interrupt. 1 = NonAudio bit generates an interrupt.
NonAudio Preamble Mask	Masks the NonAudio preamble bit from generating an interrupt. 0 = NonAudio preamble bit does not generate an interrupt. 1 = NonAudio preamble bit generates an interrupt.
CRCError Mask	Masks the CRCError bit from generating an interrupt. 0 = CRCError bit does not generate an interrupt. 1 = CRCError bit generates an interrupt.
NoStream Mask	Masks the NoStream bit from generating an interrupt. 0 = NoStream bit does not generate an interrupt. 1 = NoStream bit generates an interrupt.
BiPhase/Parity Mask	Masks the BiPhase/Parity bit from generating an interrupt. 0 = BiPhase/Parity bit does not generate an interrupt. 1 = BiPhase/Parity bit generates an interrupt.
Lock Mask	Masks the Lock bit from generating an interrupt. 0 = Lock bit does not generate an interrupt. 1 = Lock bit generates an interrupt.

Table 41. Sample Rate Converter Error Register (Read Only)

	RES	RES	RES	RES	TOO_SLOW	OVRL	OVRR	MUTE_IND
	7	6	5	4	3	2	1	0
ADDRESS = 0011010 (0x1A)								

TOO_SLOW	This bit is set, when the clock to the SRC is too slow, that is, there are not enough clock cycles to complete the internal convolution.
OVRL	This bit is set, when the left output data of the sample rate converter has gone over the full-scale range and has been clipped. This bit is not cleared until the register is read.
OVRR	This bit is set, when the right output data of the sample rate converter has gone over the full-scale range and has been clipped. This bit is not cleared until the register is read.
MUTE_IND	Mute indicated. This bit is set, when the SRC is in fast mode and clicks or pops can be heard in the SRC output data. The output of the SRC can be muted, if required, until the SRC is in slow mode. Once read, this bit remains in its state and does not generate an interrupt until it has changed state.

Table 42. Sample Rate Converter Error Mask Register

	RES	RES	RES	RES	RES	OVRL Mask	OVRR Mask	MUTE_IND MASK
	7	6	5	4	3	2	1	0
ADDRESS = 0011011 (0x1B)								
OVRL Mask	Masks the OVRL from generating an interrupt. 0 = OVRL bit does not generate an interrupt. 1 = OVRL bit generates an interrupt.							
OVRR Mask	Masks the OVRR from generating an interrupt. 0 = OVRR bit does not generate an interrupt. 1 = OVRR bit generates an interrupt. Reserved.							
MUTE_IND MASK	Masks the MUTE_IND from generating an interrupt. 0 = MUTE_IND bit does not generate an interrupt. 1 = MUTE_IND bit generates an interrupt.							

Table 43. Interrupt Status Register

	SRCError	TxCSTINT	TxUBINT	TxCSINT	RxCSDIFF	RxUBINT	RxCSBINT	RxERROR
	7	6	5	4	3	2	1	0
ADDRESS = 0011100 (0x1C)								
SRCError	This bit is set, if one of the sample rate converter interrupts is asserted, and the host should immediately read the sample rate converter error register. This bit remains high until the interrupt status register is read.							
TxCSTINT	This bit is set, if a write to the transmitter channel status buffer was made while transmitter channel status bits were being copied from the transmitter CS buffer to the SPDIF transmit buffer.							
TxUBINT	This bit is set, if the SPDIF transmit buffer is empty. This bit remains high until the interrupt status register is read.							
TxCSINT	This bit is set, if the transmitter channel status bit buffer has transmitted its block of channel status. This bit remains high until the interrupt status register is read.							
RxCSDIFF	This bit is set, if the receiver Channel Status A block is different from the receiver Channel Status B clock. This bit remains high until read, but does not generate an interrupt.							
RxUBINT	This bit is set, if the receiver user bit buffer has a new block or message. This bit remains high until the interrupt status register is read.							
RxCSBINT	This bit is set, if a new block of channel status is read when RxBCONF3 = 0, or if the channel status has changed when RxBCONF3 = 1. This bit remains high until the interrupt status register is read.							
RxERROR	This bit is set, if one of the AES3/SPDIF receiver interrupts is asserted, and the host should immediately read the receiver error register. This bit remains high until the interrupt status register is read.							

Table 44. Interrupt Status Mask Register

	SRCError Mask	TxCSTINT Mask	TxUBINT Mask	TxCSBINT Mask	RES	RxUBINT Mask	RxCSBINT Mask	RxError Mask
	7	6	5	4	3	2	1	0
ADDRESS = 0011101 (0x1D)								
SRCError Mask	Masks the SRCError bit from generating an interrupt. 0 = SRCError bit does not generate an interrupt. 1 = SRCError bit generates an interrupt.							
TxCSTINT Mask	Masks the TxCSTINT bit from generating an interrupt. 0 = TxCSTINT bit does not generate an interrupt. 1 = TxCSTINT bit generates an interrupt.							
TxUBINT Mask	Masks the TxUBINT bit from generating an interrupt. 0 = TxUBINT bit does not generate an interrupt. 1 = TxUBINT bit generates an interrupt.							
TxCSBINT Mask	Masks the TxCSBINT bit from generating an interrupt. 0 = TxCSBINT bit does not generate an interrupt. 1 = TxCSBINT bit generates an interrupt.							
RxUBINT Mask	Masks the RxUBINT bit from generating an interrupt. 0 = RxUBINT bit does not generate an interrupt. 1 = RxUBINT bit generates an interrupt.							
RxCSBINT Mask	Masks the RxCSBINT bit from generating an interrupt. 0 = RxCSBINT bit does not generate an interrupt. 1 = RxCSBINT bit generates an interrupt.							
RxError Mask	Masks the RxError bit from generating an interrupt. 0 = RxError bit does not generate an interrupt. 1 = RxError bit generates an interrupt.							

Table 45. Mute and De-Emphasis Register

	RES	RES	TxMUTE	RES	RES	SRC_DEEM1–0	RES
	7	6	5	4	3	2, 1	0
ADDRESS = 0011110 (0x1E)							
TxMUTE	Mutes the AES3/SPDIF transmitter. 0 = Transmitter is not muted. 1 = Transmitter is muted.						
SRC_DEEM1–0	Selects the de-emphasis filter for the input data to the sample rate converter. 00 = No de-emphasis. 01 = 32 kHz de-emphasis. 10 = 44.1 kHz de-emphasis. 11 = 48 kHz de-emphasis.						

Table 46. NonAudio Preamble Type Register (Read Only)

	RES	RES	RES	RES	DTS-CD Preamble	NonAudio Frame	NonAudio Subframe_A	NonAudio Subframe_B
	7	6	5	4	3	2	1	0
ADDRESS = 0011111 (0x1F)								
DTS-CD Preamble	This bit is set, if the DTS-CD preamble is detected.							
NonAudio Frame	This bit is set, if the data received through the AES3/SPDIF receiver is nonaudio data according to the IEC61937 standard or nonaudio data according to SMPTE337M.							
NonAudio Subframe_A	This bit is set, if the data received through Channel A of the AES3/SPDIF receiver is subframe nonaudio data according to SMPTE337M.							
NonAudio Subframe_B	This bit is set, if the data received through Channel B of the AES3/SPDIF receiver is subframe nonaudio data according to SMPTE337M.							

Table 47. Receiver Channel Status Buffer

	RCSB7–RCSB0
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0100000 to 0110111 (0x20 to 0x37)	
RCSB7–0	The 24-byte receiver channel status buffer. The PRO bit is stored at address location 0x20, Bit 0. This buffer is read only if the channel status is not autobuffered between the receiver and transmitter.

Table 48. Transmitter Channel Status Buffer

	TCSB7–TCSB0
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 0111000 to 1001111 (0x38 to 0x4F)	
TCSB7–0	The 24-byte transmitter channel status buffer. The PRO bit is stored at address location 0x38, Bit 0. This buffer is disabled when autobuffering between the receiver and transmitter is enabled.

Table 49. Receiver User Bit Buffer Indirect Address Register

	RxUBADDR07–RxUBADDR00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 1010000 (0x50)	
RxUBADDR07–00	Indirect address pointing to the address location in the receiver user bit buffer.

Table 50. Receiver User Bit Buffer Data Register

	RxUBDATA07–RxUBDATA00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 1010001 (0x51)	
RxUBDATA07–00	A read from this register reads eight bits of user data from the receiver user bit buffer pointed to by RxUBADDR07–00. This buffer can be written to when autobuffering of the user bits is enabled; otherwise, it is a read-only buffer.

Table 51. Transmitter User Bit Buffer Indirect Address Register

	TxUBADDR07–TxUBADDR00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 1010010 (0x52)	
TxUBADDR07–00	Indirect address pointing to the address location in the transmitter user bit buffer.

Table 52. Transmitter User Bit Buffer Data Register

	TxUBDATA07–TxUBDATA00
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 1010011 (0x53)	
TxUBDATA07–00	A write to this register writes eight bits of user data to the transmit user bit buffer pointed to by TxUBADDR07–00. When user bit autobuffering is enabled, this buffer is disabled.

Table 53. Q Subcode CRCError Status Register (Read-Only)

	RES	RES	RES	RES	RES	RES	QCRCERROR	QSUB
	7	6	5	4	3	2	1	0
ADDRESS = 1010100 (0x54)								
QCRCERROR	This bit is set, if the CRC check of the Q subcode fails. This bit remains high, but does not generate an interrupt. This bit is cleared once the register is read.							
QSUB	This bit is set, if a Q subcode has been read into the Q subcode buffer (see Table 54).							

Table 54. Q Subcode Buffer

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x55	Address	Address	Address	Address	Control	Control	Control	Control
0x56	Track number	Track number	Track number	Track number	Track number	Track number	Track number	Track number
0x57	Index	Index	Index	Index	Index	Index	Index	Index
0x58	Minute	Minute	Minute	Minute	Minute	Minute	Minute	Minute
0x59	Second	Second	Second	Second	Second	Second	Second	Second
0x5A	Frame	Frame	Frame	Frame	Frame	Frame	Frame	Frame
0x5B	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
0x5C	Absolute minute	Absolute minute	Absolute minute	Absolute minute	Absolute minute	Absolute minute	Absolute minute	Absolute minute
0x5D	Absolute second	Absolute second	Absolute second	Absolute second	Absolute second	Absolute second	Absolute second	Absolute second
0x5E	Absolute frame	Absolute frame	Absolute frame	Absolute frame	Absolute frame	Absolute frame	Absolute frame	Absolute frame

Table 55. Datapath Control Register 1

	SRC1	SRC0	REC2	REC1	REC0	AUXO2	AUXO1	AUXO0
	7	6	5	4	3	2	1	0
ADDRESS = 1100010 (0x62)								
SRC1–0	Datapath source select for sample rate converter (SRC). 00 = ADC. 01 = DIR. 10 = Playback. 11 = Auxiliary in.							
REC2–0	Datapath source select for record output port. 000 = ADC. 001 = DIR. 010 = Playback. 011 = Auxiliary in. 100 = SRC.							
AUXO2–0	Datapath source select for auxiliary output port. 000 = ADC. 001 = DIR. 010 = Playback. 011 = Auxiliary in. 100 = SRC.							

Table 56. Datapath Control Register 2

	RES	RES	DAC2	DAC1	DAC0	DIT2	DIT1	DIT0
	7	6	5	4	3	2	1	0
ADDRESS = 1100011 (0x63)								
DAC2–0	Datapath source select for DAC. 00 = ADC. 01 = DIR. 10 = Playback. 11 = Auxiliary in. 100 = SRC.							
DIT2–0	Datapath source select for DIT. 000 = ADC. 001 = DIR. 010 = Playback. 011 = Auxiliary in. 100 = SRC.							

Table 57. DAC Control Register 1

	DR_ALL	DR_DIG	CHSEL1	CHSEL0	POL1	POL0	MUTER	MUTEL
	7	6	5	4	3	2	1	0
ADDRESS = 1100100 (0x64)								
DR_ALL	Hard reset and power-down. 0 = Normal, output pins go to V_{REF} level. 1 = Hard reset and low power, output pins go to AGND.							
DR_DIG	DAC digital reset. 0 = Normal. 1 = Reset all except registers.							
CHSEL1–0	DAC channel select. 00 = Normal, left-right. 01 = Both right. 10 = Both left. 11 = Swapped, right-left.							
POL1–0	DAC channel polarity. 00 = Both positive. 01 = Left negative. 10 = Right negative. 11 = Both negative.							
MUTER	Mute right channel. 0 = Normal. 1 = Mute.							
MUTEL	Mute left channel. 0 = Normal. 1 = Mute.							

Table 58. DAC Control Register 2

	RES	RES	DMCLK1	DMCLK0	DFS1	DFS0	DEEM1	DEEM0
	7	6	5	4	3	2	1	0
ADDRESS = 1100101 (0x65)								
DMCLK1–0	DAC MCLK divider. 00 = MCLK. 01 = MCLK/1.5. 10 = MCLK/2. 11 = MCLK/3.							
DFS1–0	DAC interpolator select. 00 = 8 × (MCLK = 256 × f_S). 01 = 4 × (MCLK = 128 × f_S). 10 = 2 × (MCLK = 64 × f_S). 11 = Reserved.							
DEEM1–0	DAC de-emphasis select. 00 = None. 01 = 44.1 kHz. 10 = 32 kHz. 11 = 48 kHz.							

Table 59. DAC Control Register 3

	RES	RES	RES	RES	RES	ZFVOL	ZFDATA	ZFPOL
	7	6	5	4	3	2	1	0
ADDRESS = 1100110 (0x66)								
ZFVOL	DAC zero flag on mute and zero volume. 0 = Enabled. 1 = Disabled.							
ZFDATA	DAC zero flag on zero data disable. 0 = Enabled. 1 = Disabled.							
ZFPOL	DAC zero flag polarity. 0 = Active high. 1 = Active low.							

Table 60. DAC Control Register 4

	RES	INTRPT	ZEROSEL1	ZEROSEL0	RES	RES	RES	RES
	7	6	5	4	3	2	1	0
ADDRESS = 1100111 (0x67)								
INTRPT	This bit selects the functionality of the ZEROL/INT pin. 0 = Pin functions as a ZEROL flag pin. 1 = Pin functions as an interrupt pin.							
ZEROSEL1–0	These bits control the functionality of the ZEROR pin when the ZEROL/INT pin is used as an interrupt. 00 = Pin functions as a ZEROR flag pin. 01 = Pin functions as a ZEROL flag pin. 10 = Pin is asserted when either the left or right channel is zero. 11 = Pin is asserted when both the left and right channels are zero.							

Table 61. DAC Left Volume Register

	DVOLL7	DVOLL6	DVOLL5	DVOLL4	DVOLL3	DVOLL2	DVOLL1	DVOLL0
	7	6	5	4	3	2	1	0
ADDRESS = 1101000 (0x68)								
DVOLL7–0	DAC left channel volume control. 1111111 = 0 dBFS. 1111110 = −0.375 dBFS. 0000000 = −95.625 dBFS.							

Table 62. DAC Right Volume Register

	DVOLR7	DVOLR6	DVOLR5	DVOLR4	DVOLR3	DVOLR2	DVOLR1	DVOLR0
	7	6	5	4	3	2	1	0
ADDRESS = 1101001 (0x69)								
DVOLR7–0	DAC right channel volume control. 1111111 = 0 dBFS. 1111110 = −0.375 dBFS. 0000000 = −95.625 dBFS.							

Table 63. DAC Left Peak Volume Register

	RES	RES	DLP5	DLP4	DLP3	DLP2	DLP1	DLP0
	7	6	5	4	3	2	1	0
ADDRESS = 1101010 (0x6A)								
DLP5–0	DAC left channel peak volume detection. 000000 = 0 dBFS. 000001 = −1 dBFS. 111111 = −63 dBFS.							

Table 64. DAC Right Peak Volume Register

	RES	RES	DRP5	DRP4	DRP3	DRP2	DRP1	DRP0
	7	6	5	4	3	2	1	0
ADDRESS = 1101011 (0x6B)								
DRP5–0	DAC right channel peak volume detection. 000000 = 0 dBFS. 000001 = −1 dBFS. 111111 = −63 dBFS.							

Table 65. ADC Left Channel PGA Gain Register

	RES	RES	AGL5	AGL4	AGL3	AGL2	AGL1	AGL0
	7	6	5	4	3	2	1	0
ADDRESS = 1101100 (0x6C)								
AGL5–0	PGA left channel gain control. 000000 = 0 dB. 000001 = 0.5 dB. … 101111 = 23.5 dB. 110000 = 24 dB. … 111111 = 24 dB.							

Table 66. ADC Right Channel PGA Gain Register

	RES	RES	AGR5	AGR4	AGR3	AGR2	AGR1	AGR0
	7	6	5	4	3	2	1	0
ADDRESS = 1101101 (0x6D)								
AGR5–0	PGA right channel gain control. 000000 = 0 dB. 000001 = 0.5 dB. … 101111 = 23.5 dB. 110000 = 24 dB. … 111111 = 24 dB.							

Table 67. ADC Control Register 1

	AMC	HPF	PWRDWN	ANA_PD	MUTER	MUTEL	PLPD	PRPD
	7	6	5	4	3	2	1	0
ADDRESS = 1101110 (0x6E)								
AMC	ADC modulator clock. 0 = ADC MCLK/2 (128 × f_S). 1 = ADC MCLK/4 (64 × f_S).							
HPF	High-pass filter enable. 0 = Normal. 1 = HPF enabled.							
PWRDWN	ADC power-down. 0 = Normal. 1 = Power-down.							
ANA_PD	ADC analog section power-down. 0 = Normal. 1 = Power-down.							
MUTER	Mute ADC right channel. 0 = Normal. 1 = Muted.							
MUTEL	Mute ADC left channel. 0 = Normal. 1 = Muted.							
PLPD	PGA left power-down. 0 = Normal. 1 = Power-down.							
PRPD	PGA right power-down. 0 = Normal. 1 = Power-down.							

Table 68. ADC Control Register 2

	RES	RES	RES	BUF_PD	RES	RES	MCD1	MCD0
	7	6	5	4	3	2	1	0
ADDRESS = 1101111 (0x6F)								
BUF_PD	Reference buffer power-down control. 0 = Normal. 1 = Power-down.							
MCD1–0	ADC master clock divider. 00 = Divide by 1. 01 = Divide by 2. 10 = Divide by 3. 11 = Divide by 1.							

Table 69. ADC Left Volume Register

	AVOLL7	AVOLL6	AVOLL5	AVOLL4	AVOLL3	AVOLL2	AVOLL1	AVOLL0
	7	6	5	4	3	2	1	0
ADDRESS = 1110000 (0x70)								
AVOLL7–0	ADC left channel volume control. 1111111 = 1.0 (0 dBFS). 1111110 = 0.996 (−0.00348 dBFS). 1000000 = 0.5 (−6 dBFS). 0111111 = 0.496 (−6.09 dBFS). 0000000 = 0.0039 (−48.18 dBFS).							

Table 70. ADC Right Volume Register

	AVOLR7	AVOLR6	AVOLR5	AVOLR4	AVOLR3	AVOLR2	AVOLR1	AVOLR0
	7	6	5	4	3	2	1	0
ADDRESS = 1110001 (0x71)								
AVOLR7–0	ADC right channel volume control. 1111111 = 1.0 (0 dBFS). 1111110 = 0.996 (−0.00348 dBFS). 1000000 = 0.5 (−6 dBFS). 0111111 = 0.496 (−6.09 dBFS). 0000000 = 0.0039 (−48.18 dBFS).							

Table 71. ADC Left Peak Volume Register

	RES	RES	ALP5	ALP4	ALP3	ALP2	ALP1	ALP0
	7	6	5	4	3	2	1	0
ADDRESS = 1110010 (0x72)								
ALP5–0	ADC left channel peak volume detection. 000000 = 0 dBFS. 000001 = −1 dBFS. 111111 = −63 dBFS.							

Table 72. ADC Right Peak Volume Register

	RES	RES	ARP5	ARP4	ARP3	ARP2	ARP1	ARP0
	7	6	5	4	3	2	1	0
ADDRESS = 1110011 (0x73)								
ARP5–0	ADC right channel peak volume detection. 000000 = 0 dBFS. 000001 = −1 dBFS. 111111 = −63 dBFS.							

Table 73. PLL Control Register 1

	DIRIN_CLK1	DIRIN_CLK0	MCLKODIV	PLLDIV	PLL2PD	PLL1PD	XTLPD	SYSCLK3
	7	6	5	4	3	2	1	0
ADDRESS = 1110100 (0x74)								
DIRIN_CLK1-0	Recovered SPDIF clock sent to SYSCLK3. 00 = SYSCLK3 comes from PLL block. 01 = Reserved. 10 = Reserved. 11 = SYSCLK3 is the recovered SPDIF clock from DIRIN.							
MCLKODIV	Divide input MCLK by 2 to generate MCLKO. 0 = Disabled. 1 = Enabled.							
PLLDIV	Divide XIN by 2 to generate the PLL master clock. 0 = Disabled. 1 = Enabled.							
PLL2PD	Power-down PLL2. 0 = Normal. 1 = Power-down.							
PLL1PD	Power-down PLL1. 0 = Normal. 1 = Power-down.							
XTLPD	Power-down XTAL oscillator. 0 = Normal. 1 = Power-down.							
SYSCLK3	Clock output for SYSCLK3. 0 = 512 × f_S. 1 = 256 × f_S.							

Table 74. PLL Control Register 2

	FS2_1	FS2_0	SEL2	DOUB2	FS1	FS0	SEL1	DOUB1
	7	6	5	4	3	2	1	0
ADDRESS = 1110101 (0x75)								
FS2_1–0	Sample rate select for PLL2. 00 = 48 kHz. 01 = Reserved. 10 = 32 kHz. 11 = 44.1 kHz.							
SEL2	Oversample ratio select for PLL2. 0 = 256 × f_S. 1 = 384 × f_S.							
DOUB2	Double-selected sample rate on PLL2. 0 = Disabled. 1 = Enabled.							
FS1–0	Sample rate select for PLL1. 00 = 48 kHz. 01 = Reserved. 10 = 32 kHz. 11 = 44.1 kHz.							
SEL1	Oversample ratio select for PLL1. 0 = 256 × f_S. 1 = 384 × f_S.							
DOUB1	Double-selected sample rate on PLL1. 0 = Disabled. 1 = Enabled.							

Table 75. Internal Clocking Control Register 1

	DCLK2	DCLK1	DCLK0	ACLK2	ACLK1	ACLK0	ICLK2_1	ICLK2_0
	7	6	5	4	3	2	1	0
ADDRESS = 1110110 (0x76)								
DCLK2–0	DAC clock source select. 000 = XIN. 001 = MCLKI. 010 = PLLINT1. 011 = PLLINT2. 100 = DIR PLL (512 × f_S). 101 = DIR PLL (256 × f_S). 110 = XIN. 111 = XIN.							
ACLK2–0	ADC clock source select. 000 = XIN. 001 = MCLKI. 010 = PLLINT1. 011 = PLLINT2. 100 = DIR PLL (512 × f_S). 101 = DIR PLL (256 × f_S). 110 = XIN. 111 = XIN.							
ICLK2_1–0	Source selector for internal clock ICLK2. 00 = XIN. 01 = MCLKI. 10 = PLLINT1. 11 = PLLINT2.							

Table 76. Internal Clocking Control Register 2

	RES	RES	RES	ICLK1_1	ICLK1_0	PLL2INT1	PLL2INT0	PLL1INT
	7	6	5	4	3	2	1	0
ADDRESS = 1110111 (0x77)								
ICLK1_1–0	Source selector for internal clock ICLK1. 00 = XIN. 01 = MCLKI. 10 = PLLINT1. 11 = PLLINT2.							
PLL2INT1–0	PLL2 internal selector (see Figure 38). 00 = FS2. 01 = FS2/2. 10 = FS3. 11 = FS3/2.							
PLL1INT	PLL1 internal selector. 0 = FS1. 1 = FS1/2.							

Table 77. PLL Clock Source Register

	PLL1_Source	PLL2_Source	RES	RES	RES	RES	RES	RES
	7	6	5	4	3	2	1	0
ADDRESS = 1111000 (0x78)								
PLL1_Source	Selects the clock source for PLL1.							
	0 = XIN.							
	1 = MCLKI.							
PLL2_Source	Selects the clock source for PLL2.							
	0 = XIN.							
	1 = MCLKI.							

Table 78. PLL Output Enable Register

	RES	RES	DIRINPD	DIRIN_PIN	RES	SYSCLK1	SYSCLK2	SYSCLK3
	7	6	5	4	3	2	1	0
ADDRESS = 1111010 (0x7A)								
DIRINPD	This bit powers down the SPDIF receiver.							
	0 = Normal.							
	1 = Power-down.							
DIRIN_PIN	This bit determines the input levels of the DIRIN pin.							
	0 = DIRIN accepts input signals down to 200 mV according to AES3 requirements.							
	1 = DIRIN accepts input signals as defined in the Specifications section.							
SYSCLK1	Enables the SYSCLK1 output.							
	0 = Enabled.							
	1 = Disabled.							
SYSCLK2	Enables the SYSCLK2 output.							
	0 = Enabled.							
	1 = Disabled.							
SYSCLK3	Enables the SYSCLK3 output.							
	0 = Enabled.							
	1 = Disabled.							

Table 79. ALC Control Register 1

	FSSEL1–0	GAINCNTR1–0	RECMODE1–0	LIMDET	ALCEN
	7, 6	5, 4	3, 2	1	0
ADDRESS = 1111011 (0x7B)					
FSSEL1–0	These bits should equal the sample rate of the ADC. 00 = 96 kHz. 01 = 48 kHz. 10 = 32 kHz. 11 = Reserved.				
GAINCNTR1–0	These bits determine the limit of the counter used in limited recovery mode. 00 = 3. 01 = 7. 10 = 15. 11 = 31.				
RECMODE1–0	These bits determine which recovery mode is used by the ALC section. 00 = No recovery. 01 = Normal recovery. 10 = Limited recovery. 11 = Reserved.				
LIMDET	These bits limit detect mode. 0 = ALC is used when either channel exceeds the set limit. 1 = ALC is used only when both channels exceed the set limit.				
ALCEN	These bits enable ALC. 0 = Disable ALC. 1 = Enable ALC.				

Table 80. ALC Control Register 2

	RES	RECTH1–0	ATKTH1–0	RECTIME1–0	ATKTIME
	7	6, 5	4, 3	2, 1	0
ADDRESS = 1111100 (0x7C)					
RECTH1–0	Recovery threshold. 00 = −2 dB. 01 = −3 dB. 10 = −4 dB. 11 = −6 dB.				
ATKTH1–0	Attack threshold. 00 = 0 dB. 01 = −1 dB. 10 = −2 dB. 11 = −4 dB.				
RECTIME1–0	Recovery time selection. 00 = 32 ms. 01 = 64 ms. 10 = 128 ms. 11 = 256 ms.				
ATKTIME	Attack timer selection. 0 = 1 ms. 1 = 4 ms.				

Table 81. ALC Control Register 3

	ALC RESET
	7, 6, 5, 4, 3, 2, 1, 0
ADDRESS = 1111101 (0x7D)	
ALC RESET	A write to this register restarts the ALC operation. The value written to this register is irrelevant. A read from this register gives the gain reduction factor.

LAYOUT CONSIDERATIONS

Getting the best performance from the ADAV803 requires a careful layout of the printed circuit board (PCB). Using separate analog and digital ground planes is recommended, because these give the currents a low resistance path back to the power supplies. The ground planes should be connected in only one place, usually under the ADAV803, to prevent ground loops.

The analog and digital supply pins should be decoupled to their respective ground pins with a 10 µF to 47 µF tantalum capacitor and a 0.1 µF ceramic capacitor. These capacitors should be placed as close as possible to the supply pins.

ADC

The ADC uses a switch capacitor input stage and is, therefore, particularly sensitive to digital noise. Sources of noise, such as PLLs or clocks, should not be routed close to the ADC section. The CAPxN and CAPxP pins form a charge reservoir for the switched capacitor section of the ADC, so keeping these nodes electrically quiet is a key factor in ensuring good performance. The capacitors connected to these pins should be of good quality, either NPO or COG, and should be placed as close as possible to CAPxN and CAPxP.

DAC

The DAC requires an analog filter to filter out-of-band noise from the analog output. A third-order Bessel filter is recommended, although the filter to use depends on the requirements of the application.

PLL

The PLL can be used to generate digital clocks, either for use internally or to clock external circuitry. Because every clock is a potential source of noise, care should be taken when using the PLL. The ADAV803's PLL outputs can be enabled or disabled, as required. If the PLL clocks are not required by external circuitry, it is recommended that the outputs be disabled. To reduce cross-coupling between clocks, a digital ground trace can be routed on either side of the PLL clock signal, if required.

The PLL has its own power supply pins. To get the best performance from the PLL and from the rest of the ADAV803, it is recommended that a separate analog supply be used. Where this is not possible, the user must decide whether to connect the PLL supply to the analog (AV_{DD}) or digital (DV_{DD}) supply. Connecting the PLL supply to AV_{DD} gives the best jitter performance, but can degrade the performance of the ADC and DAC sections slightly due to the increased digital noise created on the AV_{DD} by the PLL. Connecting the PLL supply to DV_{DD} keeps digital noise away from the analog supply, but the jitter specifications might be reduced depending on the quality of the digital supply. Using the layout recommendations described in this section helps to reduce these effects.

RESET AND POWER-DOWN CONSIDERATIONS

When the ADAV803 is held in reset by bringing the $\overline{\text{RESET}}$ pin low, a number of circuit blocks remain powered up. For example, the crystal oscillator circuit based around the XIN and XOUT pins is still active, so that a stable clock source is available when the ADAV803 is taken out of reset. Also, the VCO associated with the SPDIF receiver is active so that the receiver locks to the incoming SPDIF stream in the shortest possible time. Where power consumption is a concern, the individual blocks of the ADAV803 can be powered down via the control registers to gain significant power savings. Table 82 shows typical power savings when using the power-down bits in the control registers.

Table 82. Typical Power Requirements

Operating Mode	AV_{DD} (mA)	DV_{DD} (mA)	ODV_{DD} (mA)	DIR_V_{DD} (mA)	Power (mW)
Normal	50	25	5	5	280.5
Reset low	30	4	2.5	1	123.75
Power-down bits	12	0.1	1.3	0.7	46.53

OUTLINE DIMENSIONS

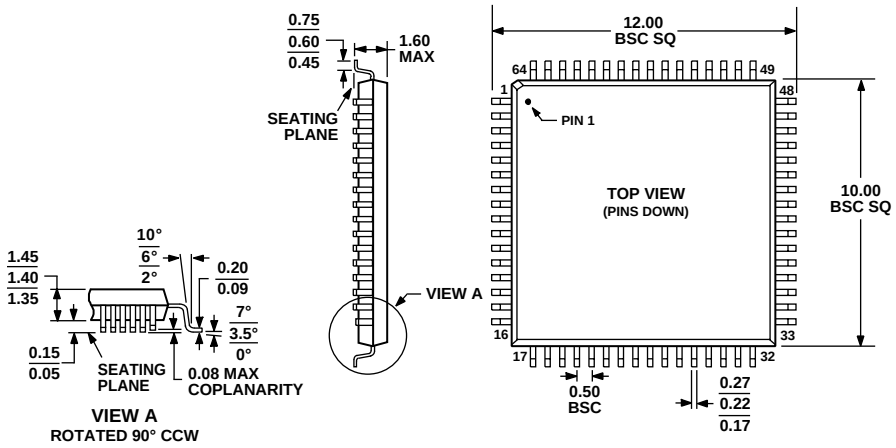

Figure 55. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Control Interface	DAC Outputs	Package Description	Package Option
ADAV803ASTZ[1]	−40°C to +85°C	SPI	Single-Ended	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADAV803ASTZ-REEL[1]	−40°C to +85°C	SPI	Single-Ended	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2

[1] Z = Pb free part.

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