

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC1677C

### 5 V-BIAS, +19.5 dBm OUTPUT, 1.8 GHz WIDE BAND SiMMIC AMPLIFIER

#### DESCRIPTION

The  $\mu$ PC1677C is a silicon monolithic integrated circuit designed as medium output power amplifier for Ultra high frequency system applications. Due to +17 dBm output at 1 GHz, this IC is recommendable for transmitter stage amplifier of L Band wireless communication systems. This IC is packaged in 8 pin plastic DIP.

#### FEATURES

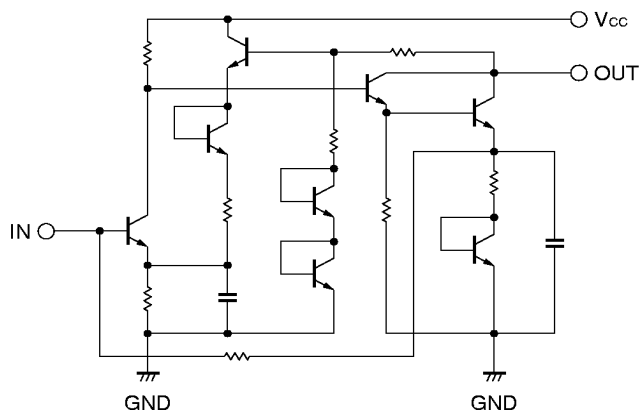
- Supply voltage : 5 V  $\pm$ 0.5 V
- High saturated output power : +19.5 dBm @ 0.5 GHz
- Excellent frequency response: 1.8 GHz TYP.  
@ 3 dB down below the gain at 0.1 GHz.
- High power gain : 24 dB TYP. @ 0.5 GHz
- Excellent isolation : 34 dBm TYP. @ 0.5 GHz

#### ORDERING INFORMATION

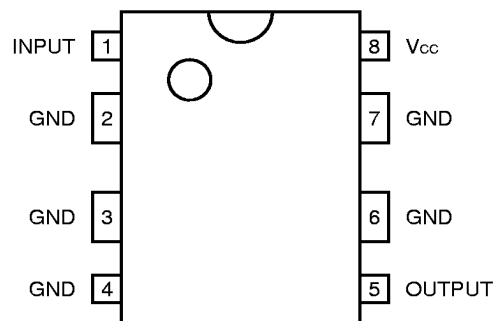
PART NUMBER	PACKAGE	SUPPLYING FORM
$\mu$ PC1677C	8 pin plastic DIP (300 mil)	Plastic magazine case.

\* For evaluation sample order, please contact your local NEC sales office. (Part number:  $\mu$ PC1677C)

#### EQUIVALENT CIRCUIT



#### PIN CONNECTION (Top View)



**Caution: Electro-static sensitive devices.**

**ABSOLUTE MAXIMUM RATINGS (TA = +25 °C)**

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITIONS
Supply Voltage	V <sub>CC</sub>	6	V	TA = +25 °C, 5 pin, 8 pin
Power Dissipation	P <sub>D</sub>	750	mW	Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass PWB TA = +85 °C
Operating Temperature	T <sub>opt</sub>	-45 to +85	°C	
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C	
Input Power	P <sub>in</sub>	+10	dBm	TA = +25 °C

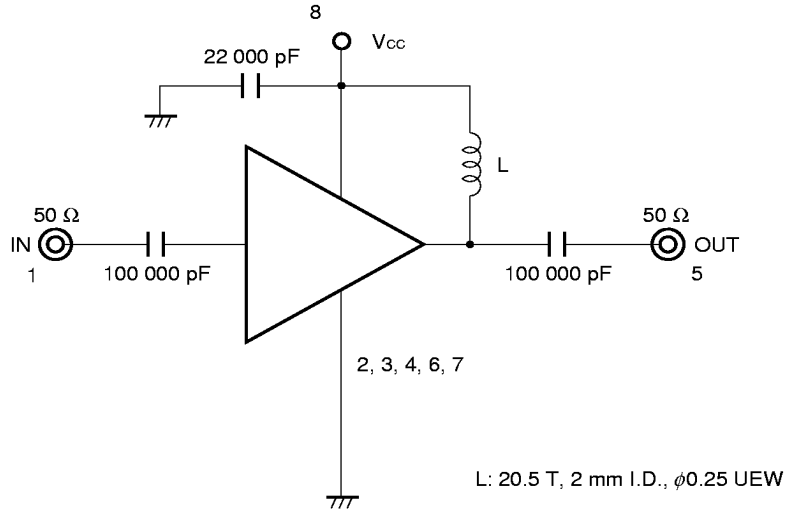
**RECOMMENDED OPERATING RANGE**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Operating Temperature	T <sub>opt</sub>	-45	+25	+85	°C

**ELECTRICAL CHARACTERISTICS (TA = +25 °C, V<sub>CC</sub> = 5 V, Z<sub>S</sub> = Z<sub>L</sub> = 50 Ω)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I <sub>CC</sub>	63	77	93	mA	No input signal
Power Gain	G <sub>P</sub>	22	24	26	dB	f = 0.5 GHz
Noise Figure	NF		6.0	8.0	dB	f = 0.5 GHz
Upper Limit Operating Frequency	f <sub>u</sub>	1.5	1.8		GHz	3 dB down below the gain at 0.1 GHz
Isolation	ISL	29	34		dB	f = 0.5 GHz
Input Return Loss	RL <sub>in</sub>	10	13		dB	f = 0.5 GHz
Output Return Loss	RL <sub>out</sub>	1	4		dB	f = 0.5 GHz
Saturated Output Power	P <sub>O(sat)</sub>	+17.5	+19.5		dBm	f = 0.5 GHz, P <sub>in</sub> = +3 dBm

TEST CIRCUIT



**Inductance for Vcc and output pin**

Due to 50 mA consuming internal output stage transistor, this IC outputs medium power. This 50 mA current should be supplied into output pin (pin No. 5) through inductance. So, please connect inductance (e.g. 300 nH) between Vcc (pin 8) and output pin (pin 5).

Inductance is intended to DC and AC effects. As for DC effect, this inductance make internal-output-transistor maximum biased to output maximum +19.5 dBm. As for AC effect, this inductance make output-port-impedance higher to get enough gain.

For above reason, large inductance value make operation wide band. 300 nH inductance is recommendable because of specified circuit.

**Capacitors for Vcc, input and output pins**

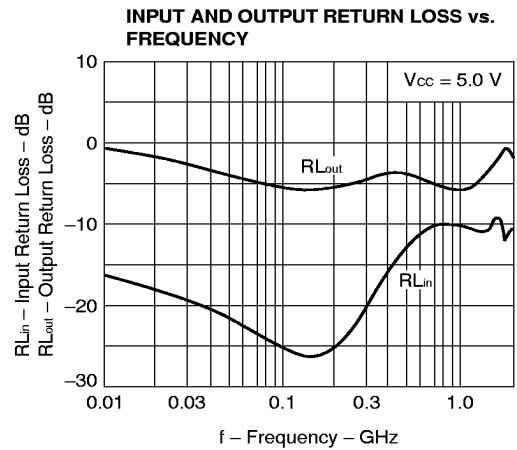
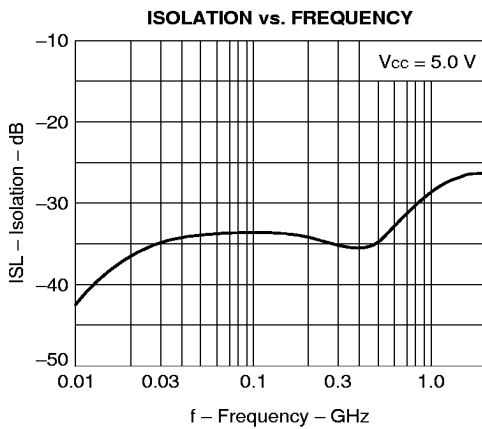
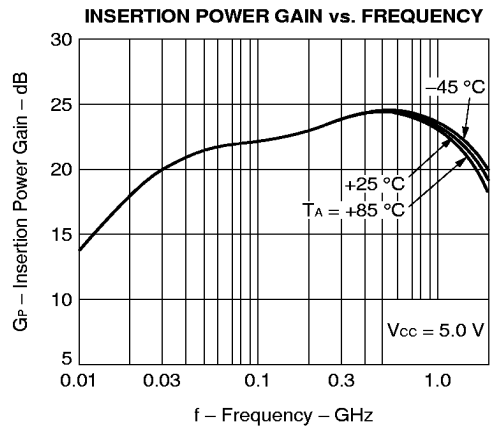
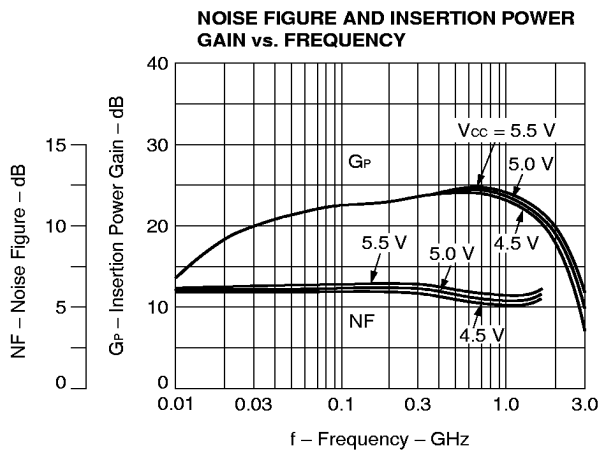
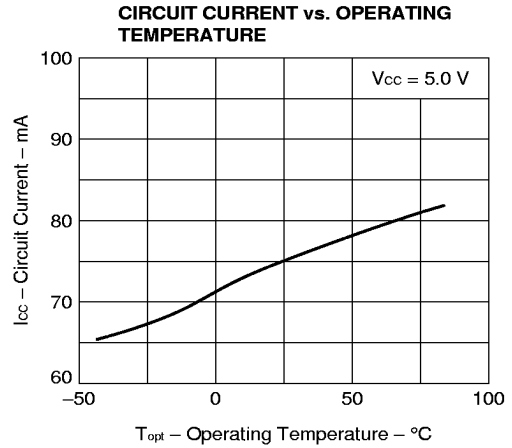
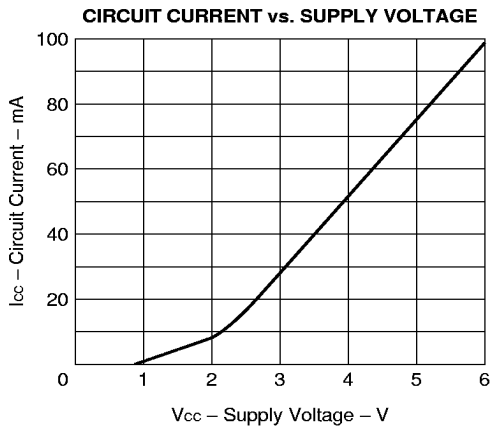
22 000 pF and 100 000 pF capacitors are recommendable as bypass capacitor for Vcc pin and coupling capacitors for input/output pins.

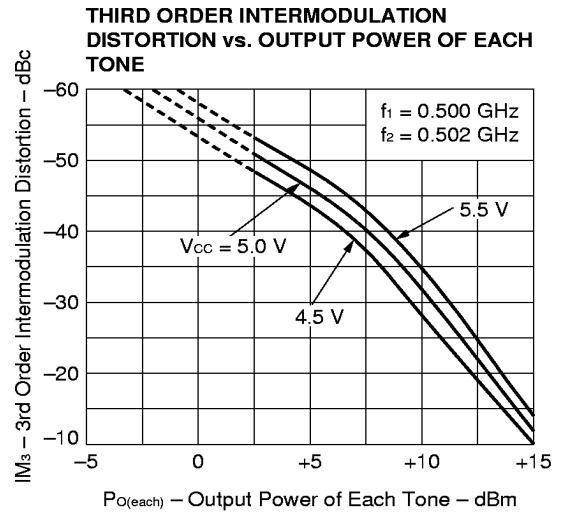
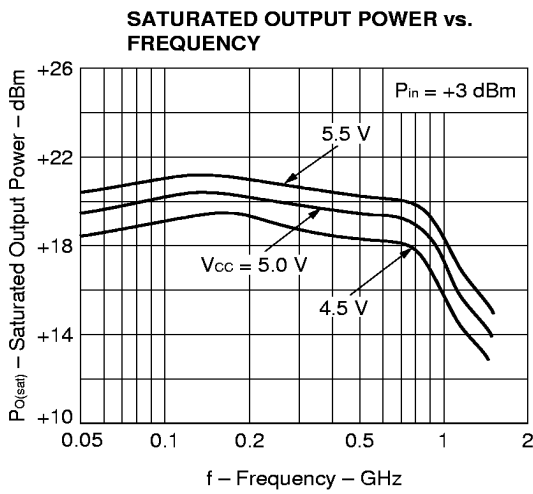
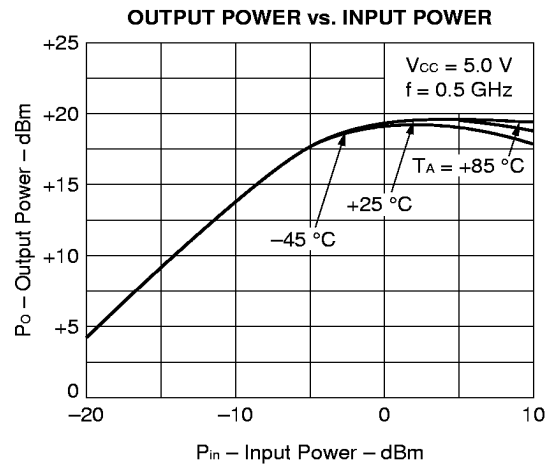
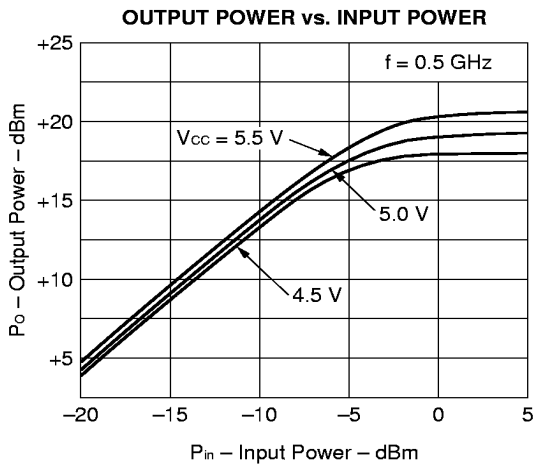
Bypass capacitor for Vcc pin is intended to minimize Vcc pin's ground impedance. Therefore, stable bias can be supplied against Vcc fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

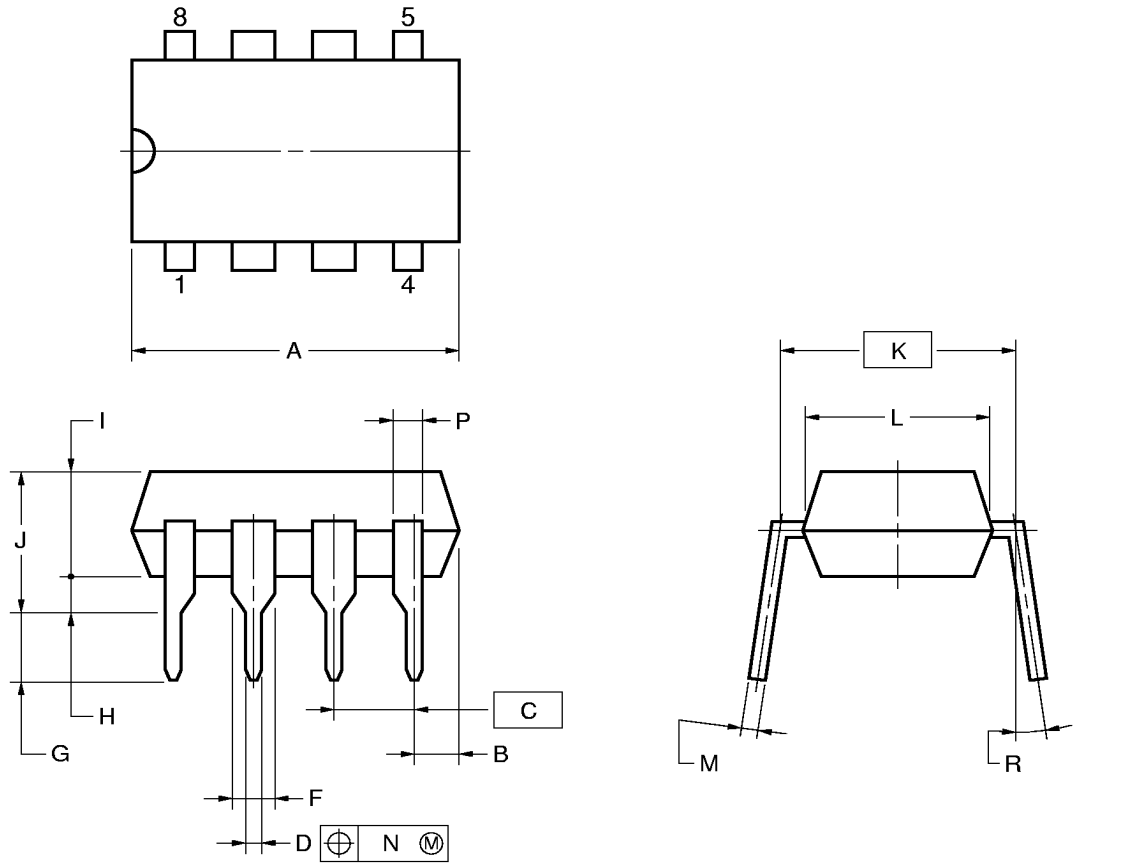
To get flat gain from 100 MHz up, 100 000 pF capacitors are assembled on the test circuit. [In the case of under 100 MHz operation, increase the value of coupling capacitor such as 1 μF. Because the coupling capacitors are determined by the equation of  $C = 1/(2 \pi fZ_s)$ .]

TYPICAL CHARACTERISTICS (T<sub>A</sub> = +25 °C)





8 PIN PLASTIC DIP (300 mil)



NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	1.4 MIN.	0.055 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P8C-100-300B,C-1

**NOTE ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired operation).
- (3) Keep the wiring length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.g. 22 000 pF) to the V<sub>CC</sub> pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

**TYPES OF THROUGH HOLE MOUNT DEVICE**

μPC1677C

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).