VFL/LED DYNAMIC DRIVERS

The TC9190N and TC9191P are VFL(Fluorescent display) and LED dynamic drivers for output extension of NEW-DTS series.

TC9190N

- . Connected with a controller by 4 serial lines.
- . 8-segment output and 7-digit output allows indication of maximum $8 \times 7=56$ segments.
- ¹. Built-in high breakdown-voltage driver allows VFL to directly drive. (P-ch open drain type where output pull-down resistance is built-in)
- . 4 built-in input ports.
- Package with shrink DIP-28 pins.

TC9191P

- . Connected with a controller by 3 serial lines.
- . 8-segment output and 5-digit output allows indication of maximum 8×5 =40 segments.
- Built-in large-current driver allows LED to directly drive.
- . Package with DIP-20pins.
- . C^2MOS construction and low power dissipation.

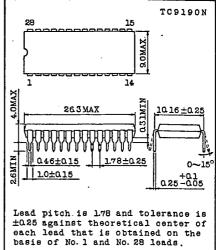
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{DD}	-0.3~7.0	v
Input Voltage	VIN	-0.3~V _{DD} +0.3	v
Output Voltage	VOL	V _{DD} -35 (Note 1)	v
Output Current	Іон	50 (Note 2)	mA
Power Dissipation	PD	350	mW
Operating Temperature	Topr	-30~75	°C
Storage Temperature	Tstg	-55~125	°C

Note 1. TC9190N only is assured.

Note 2. TC9191P only is assured.

7.50-/3.07 Unit in mm



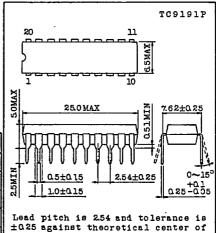
Weight: 2.2g

JEDEC

TOSHIBA

Unit in mm

4D28A-P



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 20 leads.

JEDEC —

JEDEC -TOSHIBA 3D20A-P

Weight: 1.2g

TOSHIBA, ELECTRONIC D2

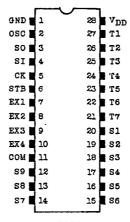
TC9190N, TC9191P



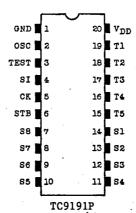
T.52.13.07

LC - 61 - 75 - 2

TERMINAL CONNECTION DIAGRAM



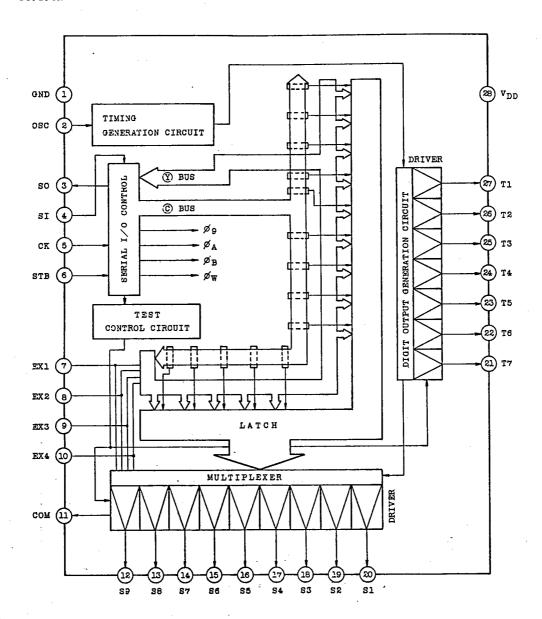
TC9190N



BLOCK DIAGRAM

TC9190N

T.52-13-07

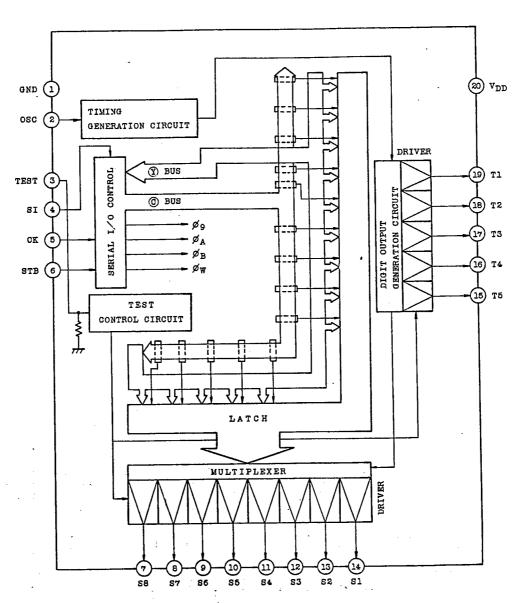


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TC9191P



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T-52-13-09

I/O MAP		Tra 12 02
1/U PIAF		T.52-13-07

	<u> </u>											/ 50	<i>x - 1 - 2</i>	<i>-</i>
	1/0		SEG 1				SEG 2				SEG 3			
i	CODE		Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
		0	OPTIO	N OUTP	UT* (ø	900)					\mathbb{I}			
		<u> </u>	EX1	EX2	EX3	EX4								
		1					$\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$					\	•	
		2		·		,		$\overline{}$	•	-		$\overline{}$		
			<u> </u>	/										
	PORT	. 3												
	INPUT PORT	4			\									
		5												
		6												
		7		-										
		8										· .		
	Ī	9	•	Γ1 (ø	99 (Y))			Γ4 (φ.	49 (Ý))			* T7	(øB9 (Y))
.			S1	S2	53	S4	S1	S2	S 3	S4	S1	S2	S3	54
1		A	•	r1 (ø	9A (Ý))			Γ4 (φ	AA (Ŷ))		;	* T7	(øba (Y))
			S 5	S6	S7	S8	85	S6	S7	S8	S5	S6	S7	S8
)RT	В			9B (Ŷ)	,		r5 (ø/	AB (V)			_		
	I P		S1_	S2	S3	S4	S1	S2	S3	S4	ļ			
	OUTPUT PORT	С			oc (Y))		·	,	(Y)					_
	8		S5	S6	S7	S8	85	Ş6	S7	58				
		D			9D (Y)		* 1		(X) (V)	, 				(øBD(Y))
			S1	S2	S3	S4_	S1	S2	S3	S4	EN		DIM ON	DIM OFF
		E			E (Y))		* 1		YE (Å)		TM (ø			_ !
	-		S5	S6	S7	S8	S5	S6	S7	S8	TEST1			
		F				ATA"9"	CHIP S						CODE DA	
L			1	0,	0	1	0	1	0	1	1	1	0	1

^{*} Option outputs T6 and T7 are built in TC9190N only.

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, VDD=5.0V)

CHARACTER	ISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
Power Supply V	oltage	v _{DD}	ļ		*	4.0	5.0	6.0	v	
Power Supply C	urrent	IDD		Non-load f _{OSC} =50kHz		-	0.2	1.0	mA	
Input Voltage	"H" Level	V _{IH1}		SI,CK,STB		$V_{DD} \times 0.7$	-	v_{DD}	v	
	"L" Level	V _{IL1}		SI,CK,STB		0	_	$v_{DD} \times 0.3$		
Input Current	"H" Level	IIHI		SI,CK,STB V _{IH} =5.0V		ı	-	±1.0	μΑ	
Input ourrent	"L" Level	IIL1		SI,CK,STB VIL=0.OV		•	•	±1.0	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
Timing Input F	requency	fopr		SI,CK,STB	*	-	300	500	kHz	
Oscillation Fr	equency	fosc		$R_X=22k\Omega$ $C_X=1500pF$	*	-	. 50	500	kHz	
Auto-Initializ	VAI				-	2.4	2.6	v		
Input Voltage	"H" Level	V _{IH2}		EX1~EX4		$v_{DD} \times 0.7$	-	$v_{ m DD}$	v	
input voituge	"L" Level	V _{IL2}		EX1~EX4		0	-	V _{DD} ×0.3		
Input Current	"H" Level	I _{IH2}		EX1~EX4 V _{IH} =5.0V		-	-	±1.0	μΛ	
Imput Current	"L" Level	IIL2		EX1~EX4 V _{IL} =0.0V		-	1	±1.0	411	
	Output Current			so v _{OH} =4.0v		-	-2.0	-1.0	mA	
Output Current				T1~T7 V _{OH} =3.0V			-15.0	-10.0		
		10Н3		S1~S9 VOH=3.0V		1	-5.0	-3.0		
Output Off-Leal	IOFF		T1~T7, S1~S9 V _{OL} =-27.0V		-	ı	±10.0	μA		
	IOFF1		so v _{OL} =0.0v		-	•	±1.0			
Load Resistanc	e .	RL		Com=-27.0V		50	100	200	kΩ	
Output Current	IOH		T1~T5, S1~S8 V _{OH} =4.0V		-	-30	-20	mA		
output Current	IOL		T1~T5, S1~S8 V _{OL} =1.0V		0.5	1.0	-			
Pull-Down Resi	stance	R _{Down}		TEST		22	47	68	kΩ	

Note: Items marked with * are assured when $V_{DD}=4.0-6.0V$, Ta=-30-75°C.

Note 1. TC9190N only is assured.

Note 2. TC9191P only is assured.

TOSHIRA

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FUNCTIONAL DESCRIPTION OF EACH TERMINAL

FUNCI	TONAL	DE2CKIALI	ON OF EACH TERM	INAL	
PIN 20 PIN	No. 28 PIN	SYMBOL	TERMINAL NAME	FUNCTIONAL & OPERATIONAL DESCRIPTION	REMARKS
1	1	GND	Power Supply Application		, .
20	28	v_{DD}	Terminal		
2	2	osc	l Terminal Oscillation Terminal	I terminal type oscillation circuit oscillating a clock necessary for the system by an external C·R.	
3	-	TEST		Pull-down resistance is built-in.	
-	31	SO	Serial Output	Serial I/O port Sending and receiving of segment	V _{DD}
4	4	SI	Serial Input	output data are performed between controllers.	
5	5	CK	Clock Signal	SO is Pch open drain output and SI,CK,STG are Schmitt trigger inputs.	2 -
6	6	STB	Strobe Signal		SI, CK, STB
_	7 ₹ 10	EX1~EX2	Option Input Terminal	Option input terminal.	C-MOS input
_	11	СОМ	VFL Power Supply Terminal	VFL driving minus power supply is applied. VDD-VFL≤33V	
-	12	S 9	Segment Output	Segment output is generated in synchronism with digit output.	V _{DD} TC9190N
7 ? 14	13 { 20	S8	Terminal	. TC9190N Pch open drain output . TC9191P Bipolar output	о
-	21 22	T7 T6	Digit Output	Dynamic indication is performed together with segment output.	V _{DD} TC9191F
15	23 1 27	T5	Terminal	. TC9190N Pch open drain output . TC9191P Bipolar output	



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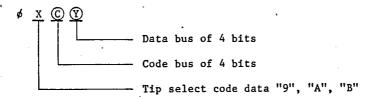
DESCRIPTION OF OPERATION

As shown in the block diagram, the TC9190N and the TC9191P are controlled by accessing port groups connected with the data bus Y and the code bus C having 4-bit function. Each data on the data bus and the code bus is sent to and recevied from the controller side by 4 terminals of SI, SO, CK, and STB (in TC9191P, 3 terminals of SI, CK, and STB) through the serial port.

As described above, all is controlled on a port basis, and description is made with the function of each port below.

These ports are constituted on 4-bit basis and each of them is selected by a code data of 4 bits. A list of code assignment to each port is desceibed as an I/O map before. As a whole, codes "OH~7H" are assigned to the input ports and codes "8H~FH" to the output ports.

- (Note 1) The meaning of "input port" and "output port" is always used with the controller side as reference. Therefore, a port to be accessed at outputting data from the controller side to the driver side is called an output port and a port to be accessed at taking in data from the driver side to the controller side is called an input port.
- (Note 2) In the sentence and the drawing, code assignment to each port is expressed with it coded as follows.



(Example) 69A9: Set S5, S8 of digit T1.

ØACF : Set S5, S6, S7, S8 of digit T2.

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O SERIAL I/O PORT

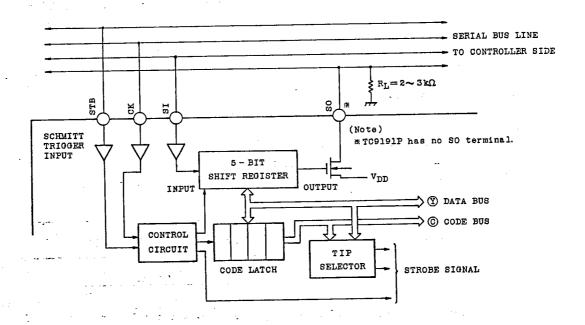
T.52-13-07

As described above, control of each port is pergormed by serial bus lines through the serial port. The serial port controls sending and receiving of data on the serial bus line and the code bus and the data bus line inside the IC.

The I/O terminals of the serial port are 4 terminals of SO, SI, CK, and STB in TC9190N since it has an input port and 3 terminals of SI, CK, and STB in TC9191F since it has no input port.

In the SI, CK, and STB terminals, schmitt trigger input is built and the SO terminal is of Pch FET open drain output construction.

(Note) For the SO terminal, an external load resistance is required. (RL=2~3k Ω)



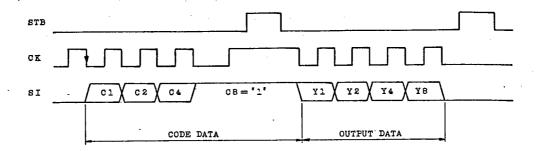
AUDIO DIGITAL IC



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1. DATA TRANSFER FORMAT

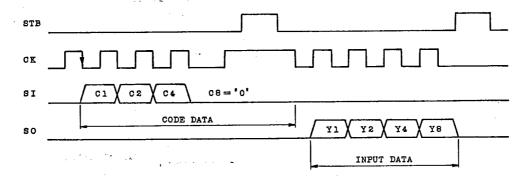
1) At outputting data (access of output port)



At the timing shown in the above drawing, input the 4-bit code data (C1~C8) of the output port and the 4-bit data (Y_1 ~ Y_8) to be output are serially input in the SI terminal. The SI data is read in at rising of CK.

(Note) At specifying the output port, the code data "C8" becomes always "1".

2) At inputting data (access of input data)



At the timing shown in the above drawing, input the 4-bit code data (C1~C8) of the input port in the SI terminal, and the data of the specified port is output to the SO terminal with 4-bit Y1~Y8 serial. The SI data is read in at rising of CK and the SO data is swept away at rising of CK.

(Note) At specifying the input port, the code data "C8" becomes always "0".

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2. SPECIFICATION OF CHIP SELECT

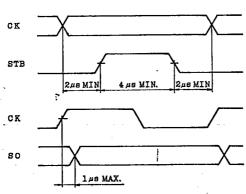
T-52-13-07

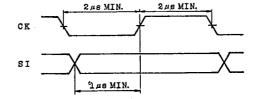
Various peripheral option IC other than a driver can be connected to serial bus lines. Therefore, it is necessary to specify as to whether a data is sent and received between the controller side and any of the ICs connected by the bus lines. For specifying the IC which is the object of control on the bus lines, a chip select code is provided.

Chip select codes for specifying TC9190N and TC9191P are the following three kinds:

- * Digit Chip select code for specifying the output ports T1~T3 and the input ports (TC9190N)
- * Digit Chip select code for specifying the output ports T4~T6 (in TC9191P, T4~T5)
- * Digit Chip select code for specifying the output port T7 (in TC9191P, no) and modes :B
- 1) The select code is set at the data output port of the chip select code(code "FH").
- 2) The select code must be set first at inputting or outputting data.
- 3) The select code once set is held unless specified again, and it is unnecessary to specify the select code everytime the data is input or output.

3. SERIAL TIMING PULSE WIDTH





4. SETTING OF MODE

In the TC9190N and the TC9191P, an auto-blanking circuit is built and the output indication at time of power on is in blanking state.

EXAMPLE AUDIO DIGITAL ICHIES



T-52-13-09.

In usual operation, it is necessary to set as follows.

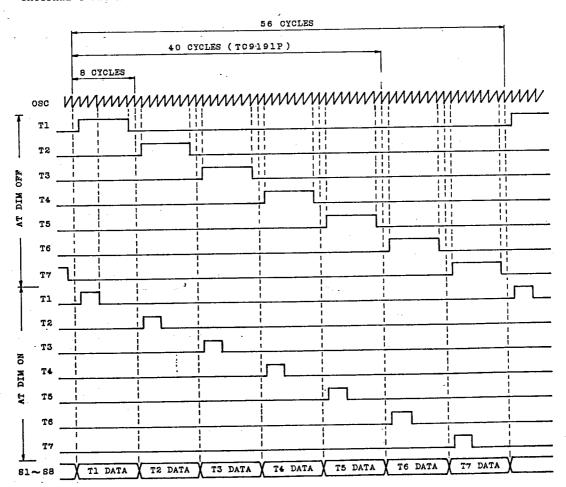
EN="1", DIS="0", TEST1="0", and TEST2="0"

When set to others, the circuits become in blanking state.

Also, these circuits have indication dimmer function. When set to DIM ON="1" and DIM OFF="0", the circuits become in DIM ON state and the brightness of indication is reduced by half or so. When set to others, DIM OFF state is indicated.

5. TIMING CHART OF OUTPUT INDICATION

The frequency of T_1 - T_7 (in TC9191P, T_1 - T_5) is determined by the constant of external C and R of OSC terminal.



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Note 1. For preventing dimming of indication at DIM OFF, T1~T7(T5) has the blanking period of two cycles.

Note 2. Renewal of indication data is executed during the blanking period described above.

© EXTERNAL INPUT PORT

The TC9190N has 4 external input ports of EX1~EX4.

EX1: T1 sync

EX2 : T2 sync

Controls S9 output

EX3 : T3 sync

EX4: T4 sync

Data of EX1~EX4 are taken in on the controller side by $\phi 900.$

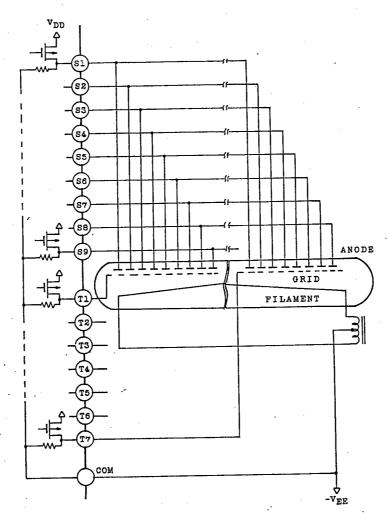
T-52-13-09 T-52-13-07 02E 18369 D

9097247 TOSHIBA. ELECTRONIC

O OUTPUT CIRCUIT

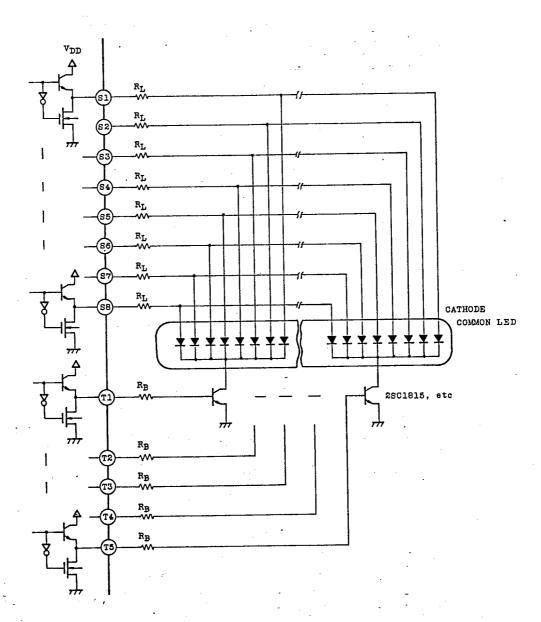
In the TC9190N, high breakdown-voltage transistor is built and VFL (fluorescent display) can be directly driven.

In the TC9191P, large-current transistor is built and LED can be directly driven. Application of TC9190N indication (for VFL)



APPLICATION OF TC9191P INDICATION (For LED)

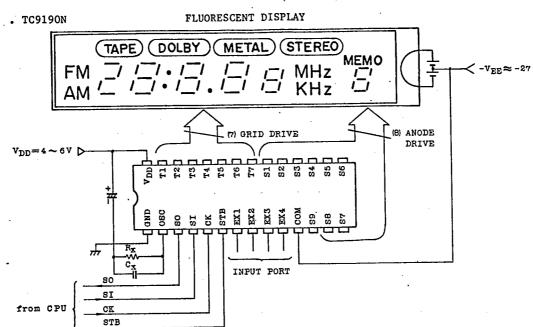
* Bipolar output



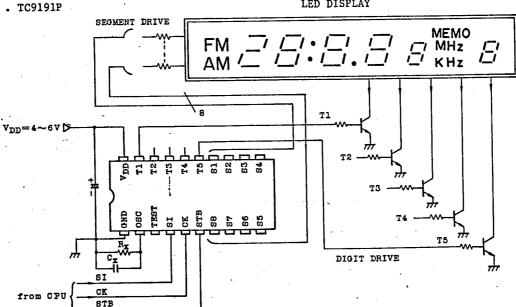


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APPLICATION CIRCUIT



LED DISPLAY



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