LR4087B/LR4087BN

Tone Dialer LSI

DESCRIPTION

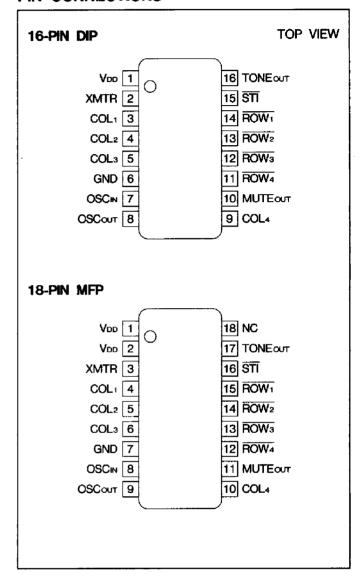
The LR4087B/LR4087BN is monolithic tone dialer LSI which uses an inexpensive crystal reference to provide eight audio sinusoidal frequencies. Dual-Tone Multi-Frequency signals are obtained by mixing these frequencies.

FEATURES

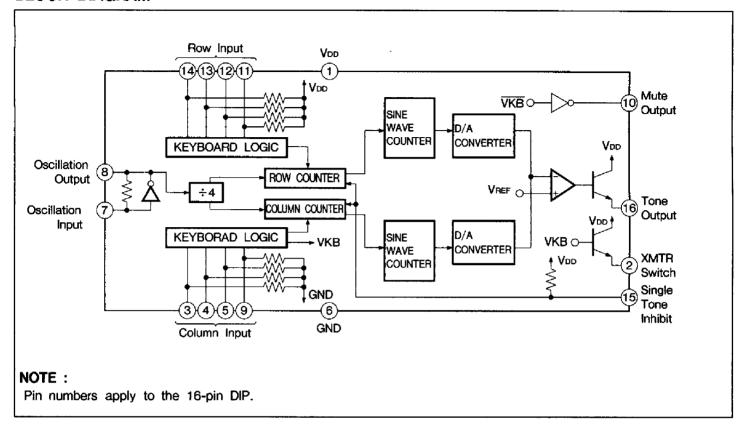
- Tone output : bipolar
- Mute output : complementary
- Uses either a standard 2-of-8 matrix keyboard or a single contact keyboard
- Uses a 3.579 545 MHz color-burst crystal oscillator as a frequency reference
- Direct telephone-line operation
- Standard Dual-Tone-Multi-Frequency (DTMF) telephone dialing
- Generates signal tones
- On-chip regulation of dual and single tone amplitudes
- Packages :

LR4087B : 16-pin DIP(DIP016-P-300B) LR4087BN : 18-pin MFP(MFP018-P)

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	Voo	/oo −0.3 to +6.2		1
Operating temperature	Topr	Topr -30 to +60		
Storage temperature	Tstg	-55 to +150	°C	
Power dissipation	Po	500	mW	2
Dia voltoro	VIN1	-0.3 V		3
Pin voltage	ViN2	+0.3 V		4

NOTES:

- 1. Referenced to GND.
- 2. Ta=25°C
- 3. The maximum applicable voltage on any pin with respect to GND.
- 4. The maximum applicable voltage on any pin with respect to Voo.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Voo	2.5 to 6.0	٧

ELECTRICAL CHARACTERISTICS

(All voltages referenced to GND, Ta = -30 to +60°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE	
STI input voltage		VIH1		0,7Vpb		Vbb	٧	1	
		VIL1		0.0		0.3Vpp	٧		
COL input voltage		VIH2		0.7Vpo		VDD	٧	2	
		VIL2		0.0	•	0.1Vpp	٧		
<u> </u>		Vінз		0.9Vpp		VDD	٧	3	
ROW output voltage		VIL3		0.0		0.3Vpp	٧	3	
Output	ROW TONE	Vor	DI 1 1: O	150	230	330	mVms	4	
voltage	COL TONE	Voc	RL=1 kΩ	190	290	420	mV⊪s		
XMTR output current,		Юнх	VDD=3.5 V, VOHX=2.5 V	-15	-25		mA	6	
XMTR output current, during key input		İXLEAX	Vpb=6.0 V, Vour=0 V		0.1	10.0	μA	6	
MUTE output current, no key input		lo _L	VDD=3.5 V, VOL=0.5 V	0.5	2.0		mA	7	
MUTE output current, during key input		Юн	VDD=3.5 V, VOH=3.0 V	0.5	2.0		mA	7	
Standby current		ISB1	V00=2.5 V		0.1	50	μΑ	- 5	
		ISB2	VDD=6.0 V		0.5	100	μA		
Operating ·current		(OP1	Vpo=2.5 V		0.7	1.5	mA	mA 5, 9	
		IOP2	VD0=6.0 V		3.0	6.0	mA		
Input resistance		Rin		20		450	kΩ	1, 4	
Tone output (no key input)						-80	dBm		
Output rise time		tr			3.0	5.0	ms	8, 9	
Pre-emphasis				1.0	2.0	3.0	dB	10	
Tone output distortion			2.5 V≤V∞≤6.0 V			-20	dB	11	

NOTES:

- 1. Applies to STI pin.
- 2. Applies to COL input pin.
- 3. Applies to ROW input pin.
- 4. Ta=25°C
- 5. All output pins open.
- 6. Applies to XMTR output pin.
- 7. Applies to MUTE output pin.

- 8. Rise time for tone output to reach 90% of maximum amplitude after key input.
- 9. Crystal resonator parameters : Rs=100 Ω , LM=96 mH, CM=0.02 pF, Ch=5 pF, f=3.579 545 MHz.
- 10. Level ratio of high group tone to low group tone.
- 11. Unnecessary frequency components against total power of basic tone signal of ROW and COL.

FUNCTIONAL DESCRIPTION

The Sharp LR4087B/LR4087BN are monolithic integrated circuit fabricated using the CMOS process. The LR4087B/LR4087BN use an inexpensive crystal reference oscillator to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing. The LR4087B/LR4087BN are designed specifically for integrated tone-dialer applications that require the

following:

- Wide-supply operation with regulated output
- Opposite-polarity logic outputs (one with a push-pull output and one with an open emitter output)
- Single contact static input
- Single tone inhibit operation

Keyboard entries select the ratios needed to divide the 3.579 545 MHz oscillator reference in order to obtain the required audio frequencies. These digital signals are then processed by a conventional R-2R ladder network. The tone output is a stair-step approximation of a sine wave, and requires little or no filtering for lowdistortion applications. The on-chip operational amplifier, that provides the current-to-voltage transformation for D/A conversion, also sums the high and low group signals to obtain the required dual tone. The accuracy of this type of tone generator is such that no frequency adjustment is needed to meet standard DTMF specifications.

Output Waveforms

The row and column output waveforms are shown in Fig. 1 and 2. These waveforms are digitally synthesized using on-chip D/A converters. Distortion measurements of these unfiltered waveforms shows a typical distortion of 7% or less. The onchip operational amplifier of the LR4087B/LR4087BN mixes the row and column tones to form a dualtone waveform. Frequency analysis of this waveform shows harmonic and intermodulation distortion components to be typically -30 dB with respect to the strongest fundamental (column) tone.

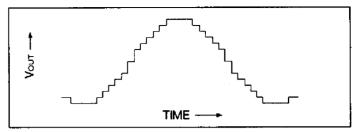


Fig. 1 Typical Sine Wave Output-Row Tones

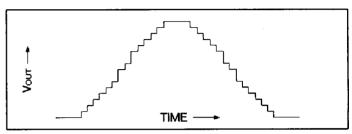


Fig. 2 Typical Sine Wave Output-Column Tones

Distortion Measurement

Total Harmonic Distortion for a single tone is given by the following expression.

THD=
$$\sqrt{\frac{V_{2t}^2 + V_{3t}^2 + V_{4t}^2 \cdots V_{nt}^2}{V_{\text{fundmental}}}} \times 100\%$$

where V2f···Vnf are the various Fourier components of the waveform being measured.

Total Harmonic Distortion for the dual tone case is defined by :

THD =
$$\sqrt{\frac{V_{2r}^2 + V_{3r}^2 + \cdots V_{rr}^2 + V_{2c}^2 + V_{3c}^2 + \cdots V_{rc}^2 + V_{IMD}^2}{\sqrt{V_{row}^2 + V_{col}^2}}} \times 100\%$$

where $\ensuremath{\mathbf{V}}_{\ensuremath{\mathbf{row}}}$ is the row fundamental amplitude,

Vcol is the column fundamental amplitude, V2r···Vnr are the amplitudes of all the Fourier components of the column frequencies, and

VIMD is the sum of all the intermodulation components.

A commonly used method of dual tone distortion measurement is the comparison of the total power of the unwanted components with the total power of the two fundamentals. For the LR4087B/LR4087BN dual tone waveforms, THD are -20 dB maximum. A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The LR4087B/LR4087BN dual tone spectrums show that individual harmonic and IMD components are typically at least -30 dB with respect to the column tone.

PIN DESCRIPTIONS (Applied to LR4087B)

ROW and COLUMN Inputs

(Pins 11, 12, 13, 14 and Pins 3, 4, 5, 9)

The LR4087B inputs are compatible with standard 2-of-8 keyboards, inexpensive single contact keyboards, and electronic input. Fig. 3 shows how to connect to the two keyboard types, and Fig. 4 shows the waveforms for electronic input. The inputs are static. i.e., noise generation does not occur as with scanned or dynamic inputs.

The internal structure of the LR4087B inputs is shown in Fig. 5. RR1 and Rc1 pull in opposite directions and hold their respective input sensing circuits off. When one or more row or column inputs are tied together however, the input sensing circuits detect the "1/2 level" and deliver a logic signal to the internal circuitry of the LR4087B, thereby causing the proper tone or tones to be generated.

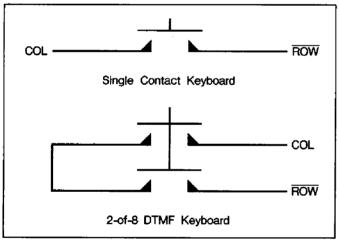


Fig. 3 Keyboard Configuration

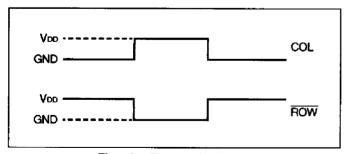


Fig. 4 Electronic Input

When used with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone generation when one or more buttons in the same row or column is pushed.

Activation of diagonal buttons will result in no tones being generaed.

When the inputs to the LR4087B are electronically activated, per Fig. 4, input to a particular row and column pair will result in the generation of that digit's dual tone. Input to a single column will generate that column tone. Input to multiple columns will result in no tone being generated. Activation of a single row is not sensed by the internal circuitry of the LR4087B. If a single row tone is desired, two columns must be activated along with the desired row.

XMTR Switch (Pin 2)

This pin is connected to the emitter of an onchip bipolar transistor whose collector is connected to VDD. With no keyboard input, this transistor is turned on and pulls pin 2 up to the VDD supply.

When a keyboard entry is sensed, this output goes open circuit (high impedance). The XMTR switch output switches regardless of the state of the Single Tone Inhibit input.

Mute Output (Pin 10)

The Mute Output is a conventional CMOS gate that pulls to GND with no keyboard input and pulls to the VDD supply when a keyboard entry is sensed.

This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The mute output switches regaedless of the state of the Single Tone Inhibit input.

Single Tone Inhibit Input (Pin 15)

The Single Tone Inhibit input is used to inhibit the generation of tones other than dual tones. It is pulled up to the VDD supply. When left floating or tied to VDD, single or dual-tones may be generated as described in the paragraph un-

der row-column inputs. When forced to the GND supply, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

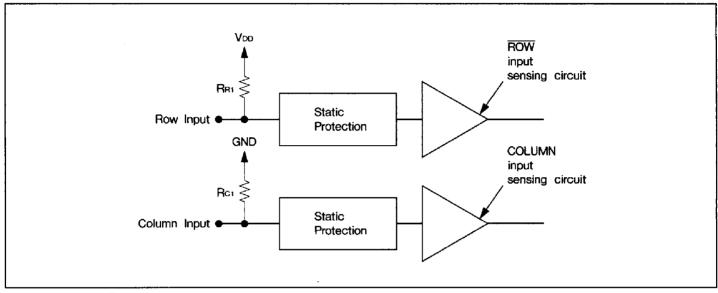


Fig. 5 Row and Column Inputs

Oscillator (Pins 7 and 8)

The network contains an on-board inverter with sufficient loop-gain to provide oscillation when used with a low-cost television color-burst crystal. The inverter's input is OSCIN (pin 7) and output is OSCOUT (pin 8). The circuit, designed to work with a 3.579 545 MHz crystal, produces the frequencies shown in Table 1.

Crystal frequency deviations will be reflected in the tone output frequency.

Tone Output (Pin 16)

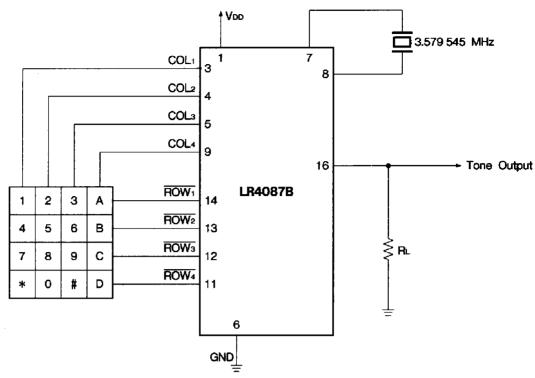
The Tone Output pin is connected internally in the LR4087B to the emitter of an NPN transistor whose collector is tied to VDD.

The on-chip operational amplifier, which mixes the row and column tones together and provides output level regulation, supplies the input to this transistor.

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ł	STANDARD DTMF (Hz)	LR4087B TONE OUTPUT FREQUENCY USING A 3.579 545 MHz CRYSTAL	STANDARD DEVIATION (%)
f1	697	701.3	+0.62
f2	770	771.4	+0.19
fз	852	857.2	+0.61
f4	941	935.1	-0.63
f5	1209	1215.9	+ 0.57
fe	1336	1331.7	-0.32
f7	1477	1471.9	0.35
f8	1633	1645.0	+0.73

TEST CIRCUIT



SYSTEM CONFIGURATION EXAMPLE

